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12th Annual Electronics Manufacturing Seminar Proceedings

Sponsored by
Electronics Manufacturing Productivity Facility
and
Soldering Technology Branch

17-19 February 1988

**NAVAL WEAPONS CENTER
CHINA LAKE, CA 93555-6001**



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FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Weapons Center, as supporting documentation for the 12th Annual Electronics Manufacturing Seminar to be held on 17-19 February 1988 at NWC, China Lake, Calif. This document is a compilation of information that was provided by both non-government and government sources.

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28 January 1988

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Released for publication by
G. R. SCHIEFER
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High-density components
High lead-count components
Hot solder coating
Integrated circuit package solderability
Intermetallic compound growth
Ionic contamination testing
Leadless chip carriers
Manual soldering
Printed wiring boards
Solderability
Solder fatigue
Soldering requirements
Stratospheric ozone
Surface insulation resistance
Surface mount technology
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Wave soldering
Wetting balance

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INTRODUCTION

The ever-changing, fast-paced technological advances being made today in electronics manufacturing present a challenge to us all. To help meet this challenge, we must work together. This Seminar – the 12th Annual Electronics Manufacturing Seminar – gives us an excellent opportunity to do just that. This Seminar promotes an open exchange of information on all issues of electronics manufacturing. It provides a forum for all persons involved in this technology, whether from government, industry, or academia. Here we can openly discuss these issues and share our ideas. Here we can work together toward our common goal: to improve the U.S. electronics industrial base.

To help make this improvement we must continue to work toward the goals of productivity, producibility, and quality. We must maintain a concerted effort to resolve production-line problems. Then, we must develop process controls and methods to solve them. Because productivity, producibility, and quality are inseparable, it is critical that our designers learn from past problems and that they design for ease of manufacturing. The Navy is continuing to work with industry through the efforts of the Electronics Manufacturing Productivity Facility (EMPF) and the Naval Weapons Center Soldering Technology Branch.

The Soldering Technology Branch is continually working to ensure that we meet the goals of producibility and quality. We evaluate soldering requirements and provide these evaluations to government and industry facilities. The Navy's work to consolidate its soldering requirements has resulted in WS-6536E, and we are continuing to work with DOD-STD-2000.

Another approach to improve our electronics industrial base is coordinated by the EMPF. The EMPF is leading the cooperative effort between electronic equipment manufacturers, product manufacturers, and government agencies to research, develop, and demonstrate electronics manufacturing processes and materials. The EMPF coordinates the cooperative work of these groups to develop high-quality processes and to demonstrate manufacturing disciplines in a production environment. The EMPF documents this cooperative work and develops an accessible information source for electronics manufacturing productivity. Our goal is to gain information, share information, and use information to help produce high-quality products at lower cost in less time.

We are indeed looking forward to working with you to improve our electronics industrial base.

We appreciate your interest in electronics manufacturing and thank you for joining us at this Seminar.

Chris Peterson
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OPTIMIZING THE HOT SOLDER COATING PROCESS FOR COMPONENT LEADS

by

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ABSTRACT

This paper will review the solder coating process for microcircuits and discrete components and how Taguchi Design of experiments was used for process development and optimization. Later discussions will go into the Taguchi concept and its impact on experimentation.

The object of the study was to achieve uniform and increased thickness of solder coating, which according to the industry experts increases shelf life and improves the integrity of the solder joint at the assembly level.

This paper will discuss what the Taguchi Design of experiments is all about and how it was applied, to achieve the objective. By reducing the process variables to key variables only, and by designing the Taguchi experiment, the actual experimental iterations were dramatically reduced. The data was analyzed and the key process variables were then adjusted to optimize the process. A confirmation experiment was conducted to verify the new levels of the key process variables. When the confirmation experiment was performed at the optimized levels, the improvements achieved in solder coating process were dramatic. It was also very revealing how certain variables had greater impact than others, on the overall result.

INTRODUCTION

During the past year or so, the wave flow soldering process had come in critical review and greater visibility at the AIL Division.

An SPC team was formed, drawing representatives from various groups to study the process, identify the critical variables and monitor the defects, and prepare control charts. It was later realized that a more viable solution to reduce assembly defects may lie in reviewing the elements which formed the assembly, rather than the finished assembly itself. One of the key elements of the assembly, was of course the components, both microcircuits and discrete. Instantly, the finish of the component leads came into focus. The problem was further compounded by the absence of first-in first-out storage. Thickness verification and measurement was a major issue. The cost factor of conducting a

major experiment was also considered. It was, in this environment, that the decision to design and conduct an experiment, based on the Taguchi techniques was made.

TAGUCHI PHILOSOPHY

According to Dr. Genichi Taguchi, the quality of a product is the minimum loss imparted by product to the society from the time product is shipped. He associates loss with every product that is used by the consumer. The loss includes, among other things, consumer dissatisfaction, added warranty costs, and loss in sales due to a bad reputation of the company.

From a technical angle, the losses of concern, are the losses which cause the products' functional characteristic to deviate from the target value. In terms of Taguchi Philosophy, it is just not enough to be within the engineering specifications. The key is to reduce the variation from the target value. The loss occurs not when the product is outside the specifications, as shown in Figure 1, but also when it falls within specifications. It is also reasonable to believe that the loss continually increases, as the product deviates further from the target value, as shown by the parabola in Figure 2.

The factors which effect the products' functional characteristics are of two types: Controllable factors and noise factors. The controllable factors are those factors, which can be controlled, such as temperature and conveyor speed. The noise factors, are those variables which are either uncontrollable or very expensive to control, like storage conditions, lead finish, and incoming part solderability variations. Since, controlling noise factors is generally out of the process engineers immediate control, Taguchi's technique is to select values for the controllable factors, such that the process is less sensitive to the changes in noise, rather than try to eliminate the noise.

PARAMETER DESIGN

While we, in the USA tend to jump from system design to tolerance design to reach the target performance levels, the Japanese emphasize the use of "parameter design", a step which is rewarding, in terms of cost and quality. The strategy of the parameter design is to recognize controllable factors and noise factors and to treat them separately. With the use of Taguchi Design of experiment, the engineer can pinpoint which variables have the strongest functional relationship to product requirement. The effect of manufacturing variables can be isolated and controlled by doing a small number of experiments as compared to conventional techniques. The processes engineer can also determine what effects the uncontrollable factors in the manufacturing process, have on the quality of the product.

When multiple variables, each with a certain number of levels are involved, the experiment can become very complicated. When using conventional experimental techniques. The size of the experiment can, however, be drastically reduced by appropriately fractionalizing its design. The use of fractional design is the main premise of Dr. Taguchi's experimental design methods.

The typical steps in the experimental design are, as shown, in Appendix A. It is very imperative that only the key variables are used in the experiment. The levels of factors are generally based on the experimenter's knowledge of the process and the equipment. While traditional analysis involves the study of the mean response, Dr. Taguchi stresses additionally the importance of the study of the variation of the response and has introduced the concept of signal to noise (S/N) ratio. The signal to noise ratio is the ratio of the mean (signal) to the standard deviation (noise) and is tied directly to the loss function. There are three standard formulas for computing S/N ratio: Higher the better, lower the better, nominal the best. The particular form of S/N ratio depends upon the functional characteristic and is tied directly to the loss function. Regardless of the type of formula used, higher performance, as measured by a high S/N ratio implies smaller loss as measured by the corresponding loss function.

As stated earlier, the main thrust of this paper is to show how the Taguchi Design of experiment was applied to improve the solder coating thickness for IC's [Dual In-line Packages (DIPS) in particular] and discrete components. In view of the fact that DIPS and discrete components were being soldered using different equipment, it became necessary to design two experiments, each with different key process variables and levels. The experimenter also decided to make the process robust to different noise factors. The functional characteristic of the S/N ratio was the same and the formula for the bigger, the better type of S/N ratio was used.

It is proposed to discuss the design and analysis of each experiment separately and independently.

DIP PRETINNING EXPERIMENT

The DIP pretinning experiment was conducted on a horizontal type wave flow solder equipment. Tooling used for the experiment consisted of two types: Indigenous tooling and commercial tooling. The equipment was equipped with preheaters. Types of solder and flux used were SN63 and RA respectively. All parts used for the experiment were manufactured by one vendor.

The experimenter identified five controllable factors and two noise factors, as shown in Figure 3. The next step was to recognize the

levels of each controllable factor. It was decided to test each controllable factor at two levels and keep the noise factors at one level. The complete list of factors and levels are shown in Figure 4.

The L8 orthogonal array was selected as it is considered the most appropriate design for this experiment. The ones and twos in the array denote the first and second levels of a factor, respectively. For example, the first test condition is run at the low levels of each factor, as shown in Table 1. The experimenter also decided to determine the effects of interactions between factors A and B; and C and E. The columns for each of the interactions were included in the orthogonal array.

The L8 array represents a total of eight treatments for each noise factor resulting in a total of 16 experimental runs. If the same experiment was conducted on the basis of factorial design instead of fractional factorial design, the number of experimental runs would be $2 \times 2^5 = 64$.

THE ANALYSIS

Table 2 shows the observations obtained after the experiment was conducted for each iteration. Each observation represents the average of solder thickness, in tenths of a mil on each side of the lead, four leads per DIP. The signal to noise ratio, based on "the bigger, the better formula", were computed for each iteration. The response table for S/N ratio was prepared by calculating the average of each factor at a particular level (see Table 3).

The average S/N ratios for each level of the five factors are plotted in Figure 5. The graphs reveal that B is more significant than other factors. It is also clear that factor levels B2, C2, D2, and E1 are obviously superior than other levels because of higher significant S/N ratio and therefore are the appropriate choice, as for factor A, although A2 provides a slightly higher S/N ratio yet it is not significantly better than A1. In this case, the experimenter decided to examine the mean response in Table 4 and the linear graphs as shown in Figure 6. The mean response table is not helpful either. The variation in the mean, for A2 appears to be slightly less than mean for A1. It was decided that since A2 provides a higher S/N ratio and more consistent means, it would be the right choice.

The interaction tables for A*B and C*E are shown in Table 5 and Table 6, and the graphs are plotted in Figure 7. The analysis of the graphs reveals that C*E interaction is clearly stronger than A*B interaction. This is also apparent from the departure from parallelism of the lines E1 and E2 in the graph.

A closer look at C*E graph shows that the slope of the line E2 is less severe than the slope of E1. This means that E2 is less sensitive to preheat temperature than E1. The choice of tooling, which gives the higher solder thickness is obviously E1, so long as the preheat level is at level C2. Therefore, the best combination of factors selected is A2, B2, C2, D2, and E1 (see Table 7).

CONFIRMATION EXPERIMENT

After the optimum combination of levels for each factor had been decided upon, a confirmation experiment was conducted, using a sample size of 8 DIPS. All the eight experimental runs were made under the best conditions determined earlier (see Table 8). The S/N ratio of 4.68 is very close to the highest ratio obtained in the experimental run. The improvement in the overall mean value was nearly 33 percent.

DISCRETE COMPONENTS PRETINNING EXPERIMENT

The second experiment is related to the discrete components pretinning operation. Unlike the ICS, which have Military Specification guidelines for solder finish, there is no reference to solder thickness requirements in the military standards for the discrete components. MIL-STD-202 method 208 provides for 95 percent minimum solder coverage area of the lead and no greater than 5 percent for pinholes, voids and porosity. MIL-M-38510 requires a minimum solder coating of 60 micro-inches for round leads. Taking these as the base line criteria, and to make the experiment objective, it was decided that the solder thickness on the leads should be measured.

As in the case of the DIP lead thickness experiment, a Taguchi design of the experiment was performed. The objective was once again to maximize solder thickness. The experiment was designed to include four controllable factors, which were identified as critical to solder thickness. Two noise factors were considered relevant to the experiment objective, as it was desired that the product i.e., solder thickness should be least sensitive to the type of component.

The four controllable factors specific to the type of equipment are described in Table 9. Type of components i.e., resistor and capacitor were recognized as noise factors, because the process has to be robust to each of the class of components. It was also decided that each controllable factor will be tested at three levels, each level having been decided arbitrarily. The ones, twos, and threes in the array denotes the first, second and third levels of the factors respectively, as shown in Table 10.

The L9 orthogonal array, as shown in Table 11, was selected for the controllable factors, since this array was found to be the most efficient for an experiment of this type. Under the traditional approach, $3^4 = 81$ experimental runs are required for each type of component to determine the best condition. The purpose of the L9 orthogonal array is to find the best combination in nine experimental runs.

THE ANALYSIS

The layout and table as shown in Table 12 shows the measure of the solder thickness for each experimental run, in tenth of a mil. The readings under the columns, N1 and N2 represent the solder thickness for a resistor and a capacitor, respectively under identical conditions. Since the intent of the experiment is to maximize solder thickness, the response characteristic of "the higher the better" was used and the applicable S/N ratio formula used is given below:

$$S/N \text{ (in dB)} = -10 \log [1/n (1/y_1^2 + 1/y_2^2 \dots 1/y_n^2)]$$

where y_1, y_2, \dots, y_n , refer to the observations within an experimental condition of a controlled factor.

The far right column in Table 12, represents the S/N ratios computed for each experimental run. As in the previous experiment, the larger the S/N ratio, the better.

The response table was prepared by computing the average of the S/N ratio for each level at each factor (see Table 13).

The average of the S/N ratios are plotted graphically in Figure 8. The graphs reveal that factor B, i.e. dwell time, has the greatest impact on solder thickness. The factors C and D, i.e., rates of ascent and descent, closely follow in their order of significance. It is obvious that B3, C3, and D3 offer the best choice of levels, because the S/N ratios for these levels are significantly higher than other levels. A2 offers a better choice than A1 and A3, but the difference in S/N ratio is not significant. Hence, the choice of the level for A is not obvious. It is for this reason, that a response table for the mean was prepared and the average of the means for each factor at various levels was computed (see Table 14). The mean was then plotted in the graphs, shown in Figure 9. A is again the better choice but not very significant. An analysis of the mean column (y) in the Table 12, shows that observations corresponding to A2, are generally consistent and have very small variations, where as the observations corresponding to A1 and A3 are not quite consistent and show greater variations. Therefore the experimenter decided to use level 2 for Factor A. Hence, the best combination for the factors was: A2, B3, C3, D3.

CONFIRMATION OF EXPERIMENT

Running the confirmation experiment is an important aspect of the Taguchi design. In this case, nine components of each type were tested at the levels which provided the best combination. Mean and S/N ratio for all the observations were computed and shown in Table 15.

The S/N ratio of 4.86 for the confirmation experiment compares very favorable with the highest S/N ratio of the experiment, which was 4.98 (see Tables 12 and 16). This shows that the combination of the levels for the factors arrived at was quite correct.

The mean of the confirmation experiment, when compared to the mean of the experiment shows 62 percent improvement. This experiment thus made it possible for the solder thickness coverage to be within the specifications in terms of MIL-M-38510, and created greater awareness of the concept of process control.

CONCLUSION

We have continued to collect data on solder thickness of the DIPS, ever since the experiment was conducted. Out of 127 data points, there have been three failures, when the solder thickness measured less than two tenths of a mil. The acceptability rate of 97.6 percent is very significant. Realizing the significance of statistical process control in product quality, our management has embarked on a bold initiative of controlling and monitoring the process parameters at the optimized levels rather than monitoring the product itself. Thus, the pretinning process parameters for both the DIPS and the discrete components are verified as opposed to inspecting each lot of parts. A sample of the product processed at the optimized levels is inspected at fixed intervals. All the components processed during the given interval and under the given conditions are accepted on the basis of sample acceptance and the control of the key process variables, thus reducing costly individual inspection. The data, based on this initiative, is not yet available, but the significance and potential of the concept has created great excitement and many more processes will be brought under statistical process control in the near future.

In short, statistical methods and Taguchi experimental design represent powerful tools to aid the process engineer in designing processes which conform to the demanding requirements of the new high quality and reliability specifications.

APPENDIX A
TYPICAL STEPS IN EXPERIMENT

- (a) Identify key process variables/factors
- (b) Identify the levels of each process factor
- (c) Identify the noise factor
- (d) Construct the most efficient orthogonal design array
- (e) Collect data
- (f) Classify the quality characteristic for computing S/N ratio
- (g) Compute S/N ratio
- (h) Construct response tables
- (i) Plot linear graphs
- (j) Pick the best combination of factors and levels
- (k) Conduct a confirmation experiment
- (l) Establish process controls

GLOSSARY OF TERMS

Bigger the better characteristic	It is a type of performance parameter that gives improved performance as the value of the parameter increases.
Confirmation experiment	The designed experiment defines improved conditions of process design. A confirmation experiment intended to verify the experiment predictions is run at the optimum conditions computed from the analysis of the designed experiment.
Control factors	Factors whose values can be selected and controlled by the engineer.

Factors	Parameters of variables that impact process performance.
Linear graphs	The linear graph is a series of lines plotted on a graph which have one to one correspondence value in the response table.
Noise	<p>Any uncontrollable factor that causes a product's quality characteristic to vary is called "noise".</p> <p>Examples of noise are: Temperature, humidity, vendor type, etc.</p>
Orthogonal Array	An orthogonal array is a matrix of numbers arranged in rows and columns. Each row represents the state of factors in a given experiment. Each column represents a specific factor or a condition that can be changed from experiment to experiment. The array is called orthogonal because the effects of the various factor in the experimental result can be separated from the other.
Parameter Design	The design stage where the nominal values of the critical dimensions and characteristics are established to optimize performance.
Robust	Used to describe product/process that has limited or reduced functional variation even in the presence of noise.
Signal factors	Factors which control response in a designed manner.

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Signal to Noise Ratio (S/N)

S/N is used to project field quality performance from experiment results. It is generally in decibels and depends on the type of characteristic being considered.

REFERENCES

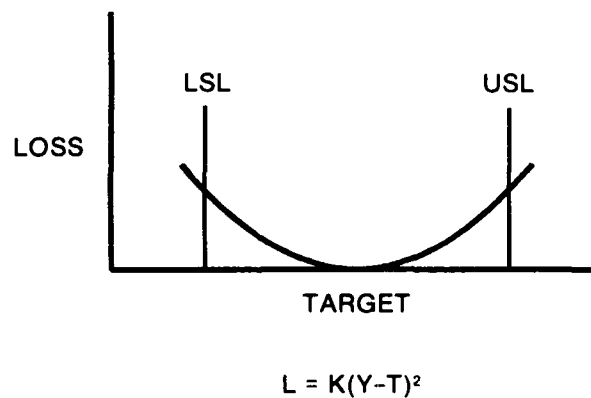
Byrne, Diane M.; Taguchi, Shin. "The Taguchi Approach to Parameter Design," ASQC Quality Congress Transaction - Anaheim, 1986.

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FIGURE 1. Pass/Fail Interpretation of Loss



L = Loss in Dollars
K = Cost coefficient
Y = Value of quality characteristic
T = Target value

FIGURE 2. Pass/Fail Interpretation of Loss

CONTROLLABLE FACTORS

- A. SOLDER TEMPERATURE
- B. CONVEYOR SPEED
- C. PREHEAT TEMPERATURE
- D. WAVE HEIGHT
- E. TOOLING TYPE

NOISE FACTORS

- N1: CLEANED COMPONENTS
- N2: NOT-CLEANED COMPONENTS

FIGURE 3. DIPS Pretinning Experiment

DESIGN FACTORS AND LEVELS

NO.	CONTROLLABLE FACTOR	LEVEL 1	LEVEL 2
A	SOLDER TEMPERATURE (°F)	450	500
B	CONVEYOR SPEED (f.p.m.)	3	6
C	PREHEAT TEMPERATURE	Low	High
D	WAVE HEIGHT	Low	High
E	TOOLING TYPE	Type 1	Type 2

NO.	NOISE FACTORS
N1	CLEANED COMPONENTS
N2	NOT-CLEANED COMPONENTS

FIGURE 4. DIPS Pretinning Experiment – Design Factors and Levels

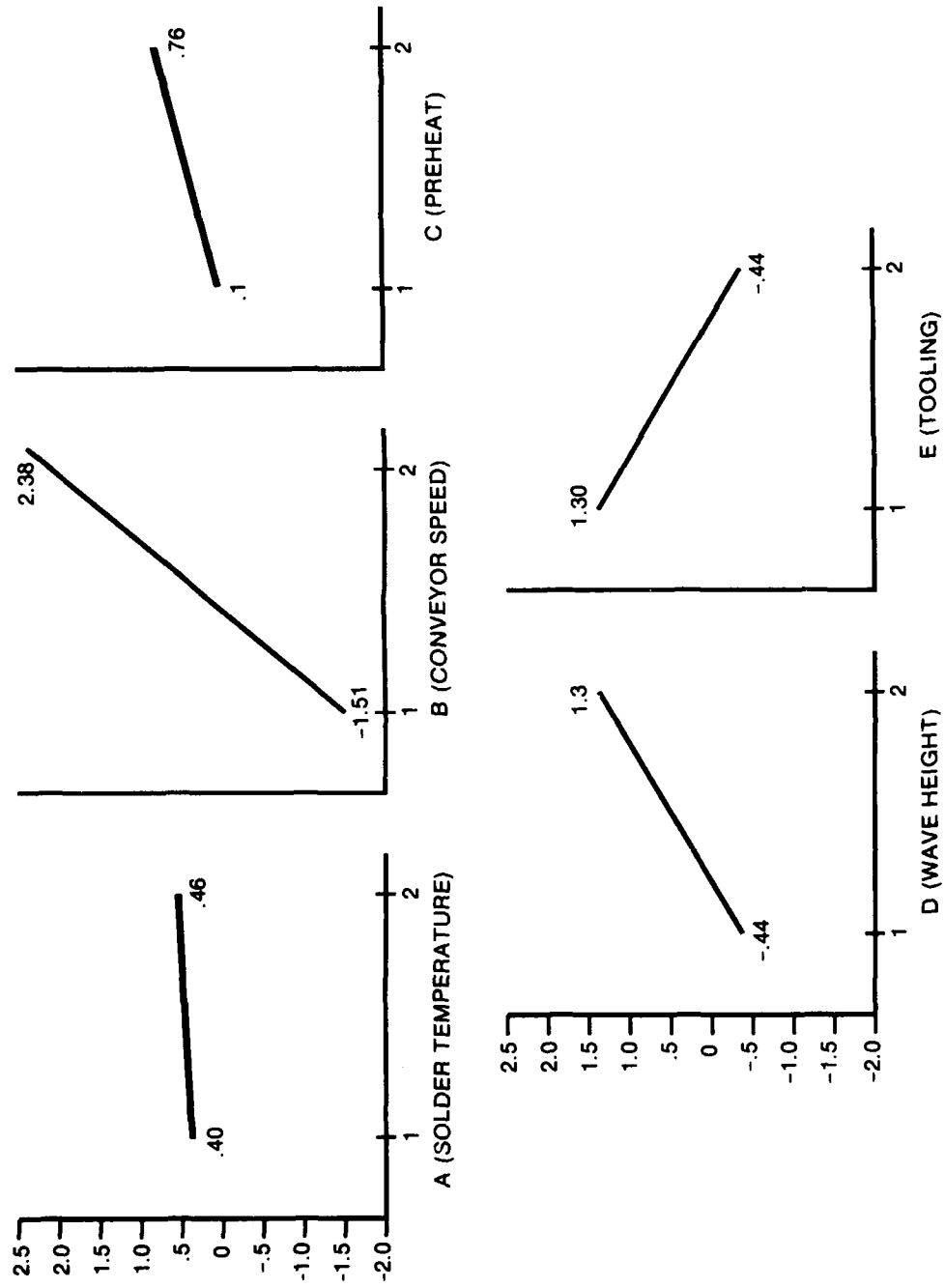


FIGURE 5. DIPS Pretinning Experiment - Linear Graphs - S/N

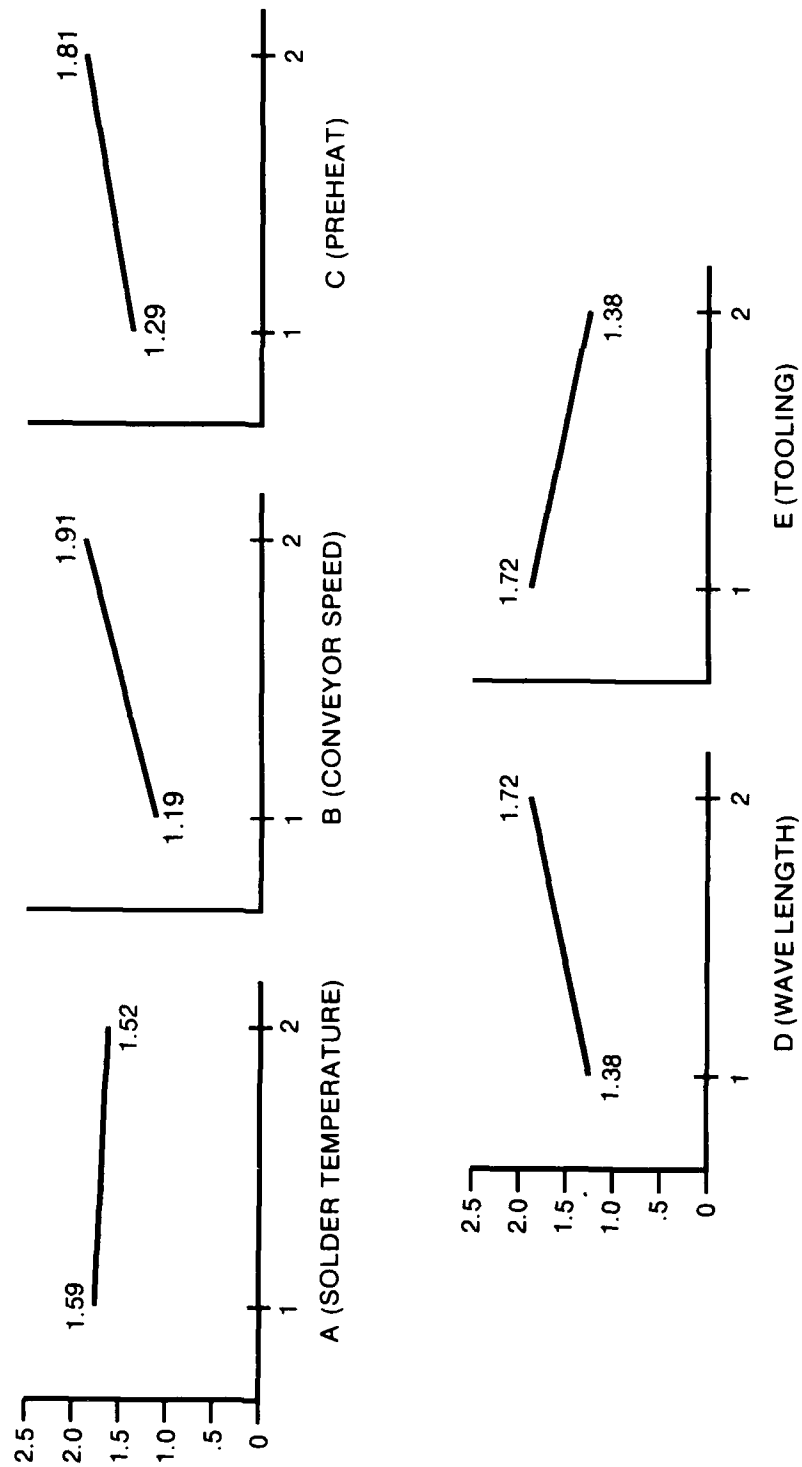


FIGURE 6. DIPS Pretinning Experiment - Linear Graphs - Means

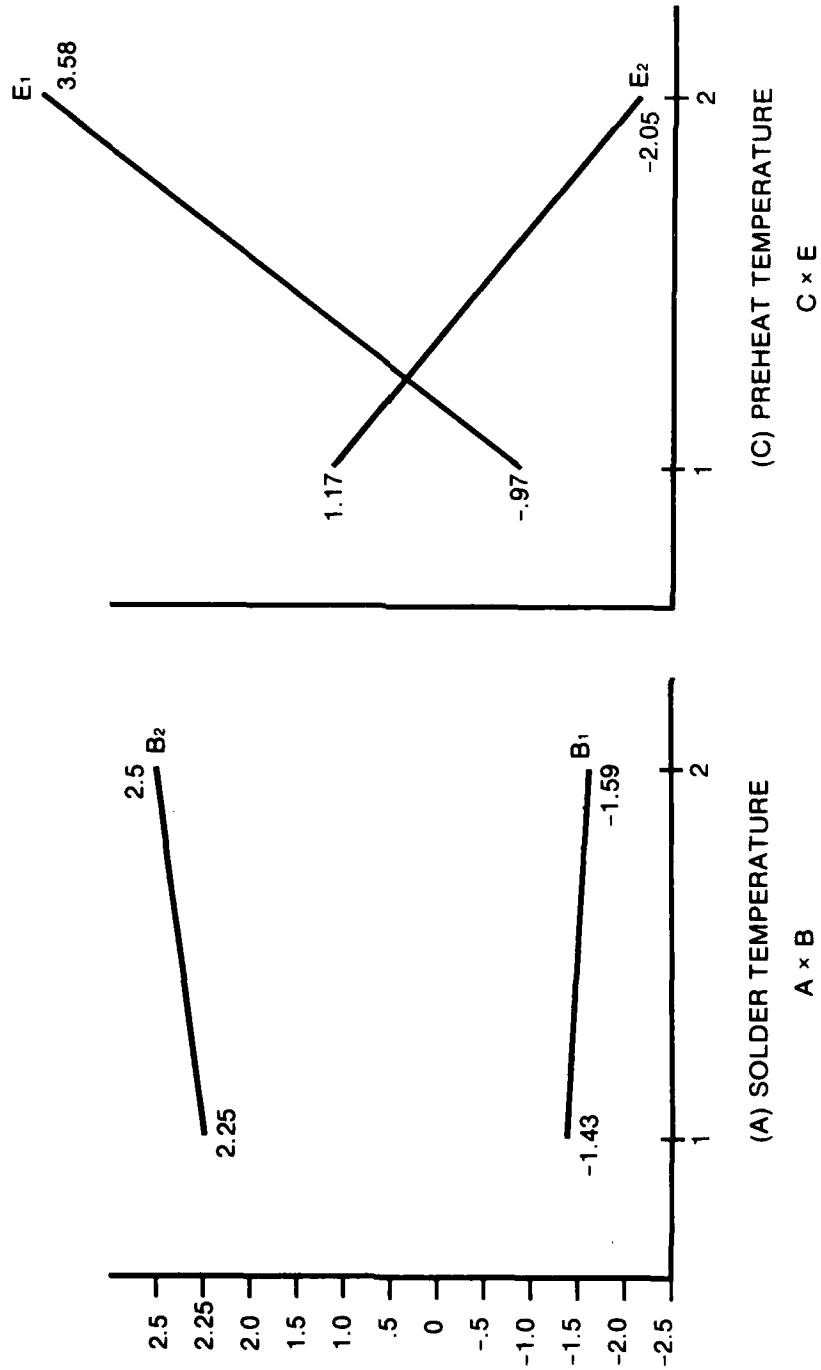


FIGURE 7. DIPS Pretinning Experiment - Interaction Plots

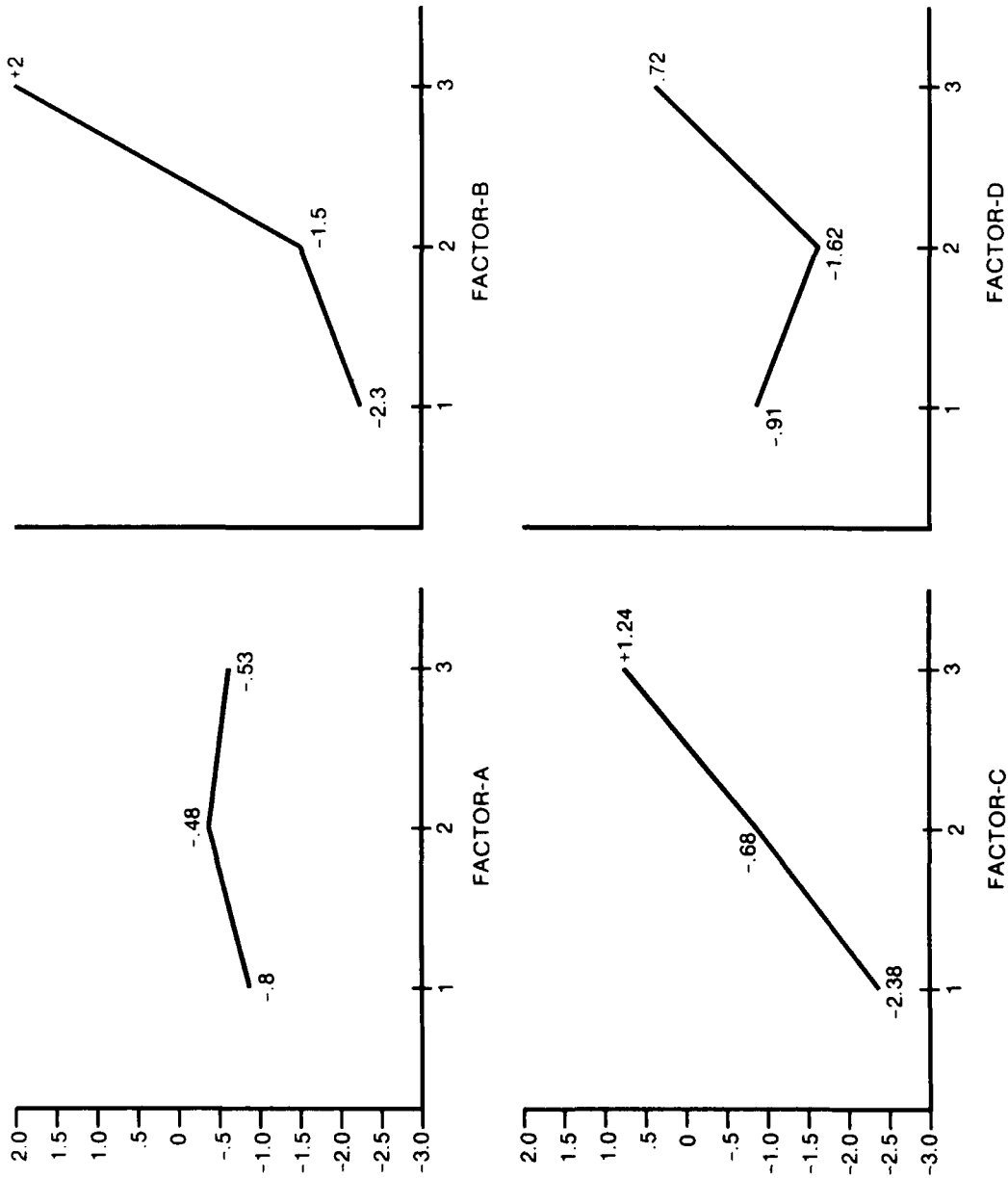


FIGURE 8. Discrete Component Pretinning Experiment - Linear Graphs - S/N

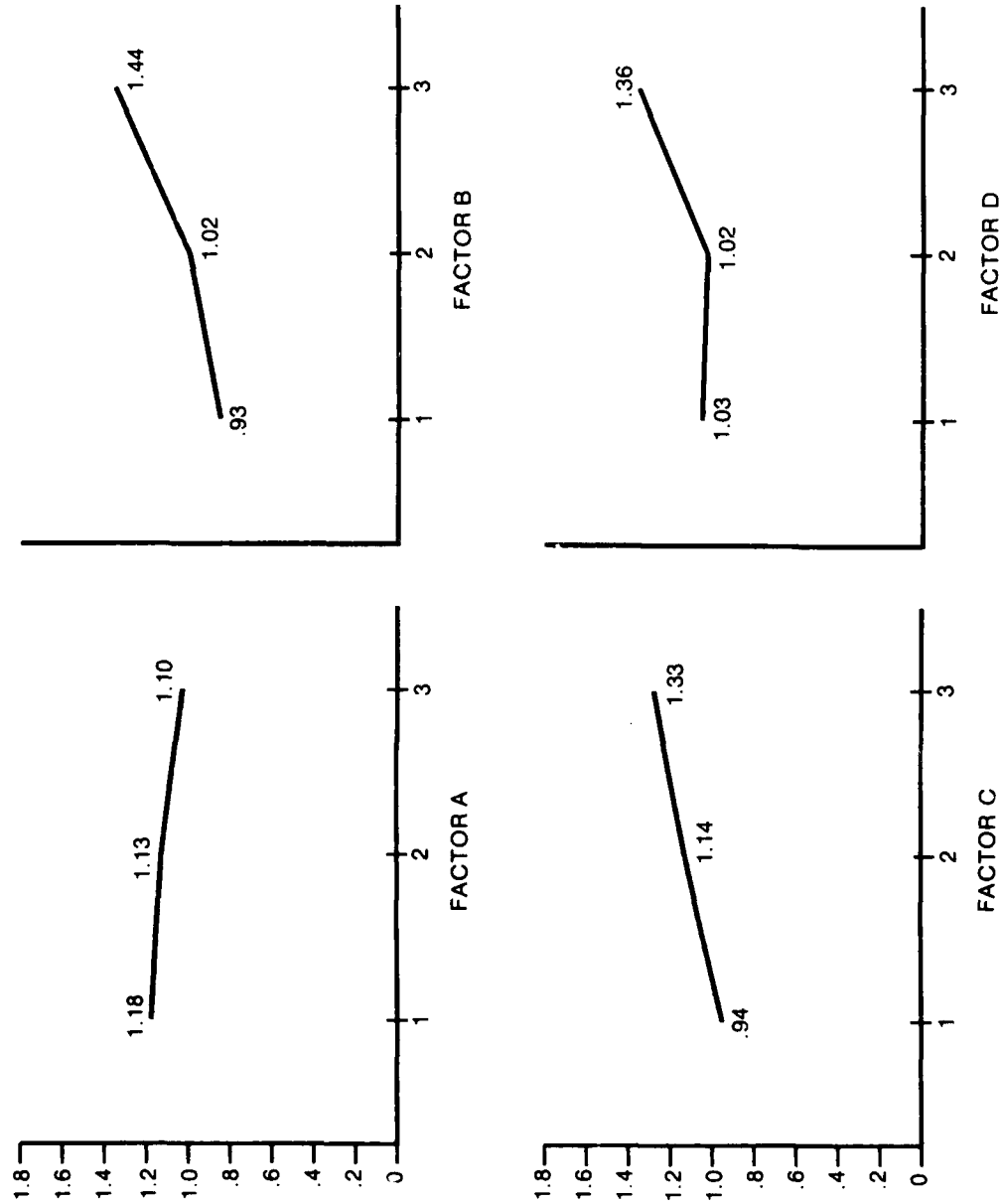


FIGURE 9. Discrete Components Pretinning Experiment - Linear Graphs - Mean

TABLE 1. DIPS Pretinning Experiment – L8 Array

NO.	A	B	A×B	C	D	E	C×E
1	1	1	1	1	1	1	1
2	1	1	1	2	2	2	2
3	1	2	2	1	1	2	2
4	1	2	2	2	2	1	1
5	2	1	2	1	2	1	2
6	2	1	2	2	1	2	1
7	2	2	1	1	2	2	1
8	2	2	1	2	1	1	2

TABLE 2. DIPS Pretinning Experiment – Layout and Data

NO	A	B	A×B	C	D	E	C×E	N1	N2	S/N	Mean.
								Thickness measured in tenth of mil	Thickness measured in tenth of mil		
1	1	1	1	1	1	1	1	0 1 1 1 1 .5 .5 2	2 1 1 1 1 0 1 1	-1.2	1.07
2	1	1	1	2	2	2	2	5 1 .5 .5 3 4 1 1	3 2 2 1 1 2 .5 0	-1.67	1.53
3	1	2	2	1	1	2	2	1 1 1 1 3 .5 2 2	1 1 .8 .8 1 2 .8 1	-.40	1.24
4	1	2	2	2	2	1	1	2 3 1 2 3 6 1.5 1.5	1 2 2 1.5 4 6 2 2	4.9	2.53
5	2	1	2	1	2	1	2	1.5 1.5 .5 1 1 1 1 1	.5 1 0 0 1 2.5 1.5 3	-.74	1.12
6	2	1	2	2	1	2	1	1 .5 0 0 1 .5 0 0	2 1 0 2 1 .5 1 0	-2.43	1.05
7	2	2	1	1	2	2	1	1 3 2 2 3 2 1 1	2 0 2 2 2 1 1 1	2.74	1.73
8	2	2	1	2	1	1	2	2 .5 1.5 1.5 3 3 1 2	2 3 2 3 3 5 1 1	2.27	2.16

$$S/N = -10 \log \left(\frac{1}{n} \sum \frac{1}{y^2} \right)$$

TABLE 3. DIPS Pretinning Experiment – Response Table – S/N

FACTORS LEVEL	A	B	A×B	C	D	E	C×E
1	.40	-1.51	.53	.1	-.44	1.30	1.33
2	.46	2.38	.33	.76	1.30	-.44	-.13

TABLE 4. DIPS Pretinning Experiment – Response Table – Mean

FACTORS LEVEL	A	B	A×B	C	D	E	C×E
1	1.59	1.19	1.62	1.29	1.38	1.72	1.6
2	1.52	1.91	1.48	1.81	1.72	1.38	1.51

TABLE 5. Interaction Graph (A×B)

		A	
		1	2
B	1	-1.43	-1.59
	2	2.25	2.5

A×B

TABLE 6. Interaction Graph (C×E)

		C	
		1	2
E	1	-.97	3.58
	2	1.17	-2.05

C×E

**TABLE 7. Optimum Combination of Controllable Factors and Levels –
Optimum Combination: A2, B2, C2, D2, E1**

FACTOR	DESCRIPTION	LEVEL
A	SOLDER TEMPERATURE (°F)	500
B	CONVEYOR SPEED (f.p.m.)	6
C	PREHEAT TEMPERATURE	HIGH
D	WAVE HEIGHT	HIGH
E	TOOLING	TYPE 1

TABLE 8. DIPS Pretinning Experiment – Confirmation Experiment

NO.	MEASUREMENTS								S/N	MEAN
1	2	2	3	1.5	2	3	1.5	2	4.68	2.06
2	2	1.5	3	4	2	4	1.5	2		
3	2	2.5	3	3	1.5	1.8	1.5	1.5		
4	2	1.5	1.5	1	1	1.8	1.5	1.5		
5	3	1.5	1.5	1.5	2	1	1.5	1		
6	1.5	1.5	1	1.5	2	2	1	1.5		
7	5	5	1.5	3	1.5	3	1	1.5		
8	2	2	5	2	2	1.5	3	2		

TABLE 9. Discrete Pretinning Experiment

A	SOLDER TEMPERATURE (°F)
B	DWELL TIME (SECONDS)
C	RATE OF ASCENT (INCHES PER SECOND)
D	RATE OF DESCENT (INCHES PER SECOND)

NOISE FACTORS

	COMPONENT TYPE
N1	RESISTORS
N2	CAPACITORS

PROCESS FACTORS

TABLE 1 Discrete Components Pretinning Experiment – Controllable Factors

NO.	PROCESS FACTOR	LEVEL 1	LEVEL 2	LEVEL 3
A.	SOLDER TEMPERATURE (°F)	450	500	550
B.	DWELL TIME (SECONDS)	2	3	4
C.	ASCENT RATE (IN./SEC)	.5	1.25	2.5
D.	DESCENT RATE (IN./SEC)	.5	1	2

TABLE 11. Discrete Components Pretinning Experiment - L₉ Array

COLUMN NO.	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

TABLE 12. Discrete Components Pretinning Experiment - Layout and Data

NO.	A	B	C	D	N1		N2		\bar{y}	S/N
1	1	1	1	1	.5	.5	1	1	.68	-4.58
					.5	.5	1	.5		
2	1	2	2	2	1	.5	.5	.5	.97	-2.89
					1.25	1	1.5	1.5		
3	1	3	3	3	2	1.5	2	1.75	1.90	4.98
					1.5	2	2	1.5		
4	2	1	2	3	.5	2	1	1	1.15	-.93
					1.5	1.5	1	.75		
5	2	2	3	1	1.25	1.25	1	.75	1.12	.15
					1.5	1.5	.75	1		
6	2	3	1	2	1.5	1	1	1	1.12	-.67
					1.5	1	.5	1.5		
7	3	1	3	2	1	1	1	1	.97	-1.40
					1.25	.5	1.25	.75		
8	3	2	1	3	1.25	1.25	1	.5	1.03	-1.89
					1.25	1.5	.5	1		
9	3	3	2	1	1	2	1	1.25	1.31	1.69
					1	1.5	1.5	1.25		

EXPERIMENTAL MEAN $\bar{y} = 1.13$

TABLE 13. Discrete Components Pretinning Experiment – Response Table

FACTOR LEVEL	A	B	C	D
1	-.8	-2.30	-2.38	-.91
2	-.48	-1.5	-.68	-1.62
3	-.53	2	1.24	.72

TABLE 14. Discrete Components Pretinning Experiment – Response Table – Mean

FACTOR LEVEL	A	B	C	D
1	1.18	.93	.94	1.03
2	1.13	1.02	1.14	1.02
3	1.10	1.44	1.33	1.36

**TABLE 15. Optimum Combination of Controllable Factors and Levels –
Optimum Combination: A2, B3, C3, D3**

FACTOR	DESCRIPTION	LEVEL
A	SOLDER TEMPERATURE (°F)	500
B	DWELL TIME (SECONDS)	4
C	ASCENT RATE (INCH/SEC)	2.5
D	DESCENT RATE (INCH/SEC)	2

TABLE 16. Confirmation Data and Analysis

ITERATION COMPONENT	1	2	3	4	5	6	7	8	9	MEAN	S/N
RESISTOR	1.5	1.75	1.5	3	2	2	1.5	1.5	2	1.83	4.86
CAPACITOR	1.5	1.5	2	2	1.5	2	1.75	2	2		

NWC TP 6896
EMPF TP 0003

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AGING ENVIRONMENTS AND THEIR EFFECTS ON SOLDERABILITY

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ABSTRACT

An attempt has been made to characterize the effect of various storage and accelerated aging environments on the wetting balance solderability of precoated electronic lead materials.

A variety of commercially available lead materials, together with an experimental 'age resistant' lead finish were tested for solderability following exposure to a number of aging atmospheres. Aging environments varied from high quality conditioned air at ambient temperature through steam at 100°C, all at atmospheric pressure.

Solderability was measured on a customized Multicore® wetting balance. Wetting curves were characterized by: time to zero force, time to $\frac{2}{3}$ of maximum wetting force and the percentage of maximum theoretical force achieved.

Results show that the selected measures of solderability demonstrate differing sensitivities to solderability loss due to aging and vary in their discriminating ability with aging environment. Results also show that all measures are necessary to adequately characterize solderability.

Materials have been ranked, dependent upon their relative performance in a given environment and some tentative conclusions drawn correlating the effects of the test environments studied.

EXPERIMENTAL GOALS

The purpose of this experiment was to study the effect of various aging environments on solderability as measured by a wetting balance. The goal was to gain a better understanding of how storage conditions affect the solderability of precoated solder lead finishes and to attempt correlation with accelerated aging environments.

In order to achieve a more precise characterization of the effect of environment on solderability, two commercially available solder lead finishes and several environments were examined.

The objective of this work was to aid the industry in making informed decisions about optimized lead finishes and their necessary storage conditions.

BACKGROUND AND HISTORY

Solderability of electronic components, whether leaded or leadless, whether through hole mounted or surface mounted, has long been known to be a major factor influencing printed wiring board yields and subsequent reliability. It has also been adequately demonstrated that board yields decrease with increased component storage times and/or aggressiveness of component manufacturing methods.

It is generally recognized that the optimized lead finish is a nominal 60/40 tin-lead solder but that its solderability deteriorates with time. The rate of deterioration depends upon the environment it is exposed to at any time prior to its bonding into the printed wiring assembly. Therefore, in order to properly test a lead material, it is necessary to simulate aging environments in a test situation. Analysis of the data gathered from both long-term natural atmosphere exposure and short-term accelerated aging can then be used to classify both material performance and accelerated aging test environment efficiency.

A series of trials were initiated in order to measure solderability of various lead finishes following exposure to a number of environments designed to simulate natural and artificial accelerated aging conditions. Attempts were also made to simulate some typical conditions found during component manufacturing and/or testing.

THE EXPERIMENT

The materials used in this experiment reflect commonly available commercial precoated electronic leads, together with an experimental 'age resistant' solder lead finish for comparison purposes. Solder coating thickness ranged from 5 through 10 microns, and solder composition was standardized at a normal 63% tin/37% lead on a copper substrate.

The full range of test lead finishes are shown in Table 1.

TABLE 1. Precoated Lead Materials

Type	Solder Thickness	Solder Analysis
Electroplated solder	$9.1 \pm 0.5 \mu\text{m}$ ($360 \pm 25 \mu''$)	$59 \pm 3\% \text{ Sn}$
Hot solder coated	$6.9 \pm 1.8 \mu\text{m}$ ($270 \pm 70 \mu''$)	$63 \pm 1\% \text{ Sn}$
Age resistant solder	$9.7 \pm 0.5 \mu\text{m}$ ($380 \pm 20 \mu''$)	$62 \pm 3\% \text{ Sn}$

The test environments were chosen in an attempt to simulate natural storage conditions, ranging from a controlled and conditioned air atmosphere at a nominal 21°C to an uncontrolled non-recirculated atmosphere representing perhaps the extremes of normally occurring storage conditions. In addition, two dry aging environments were studied with temperatures of a nominal 150°C and 88°C, respectively. Accelerated aging environments included both a high temperature, high humidity atmosphere and a low temperature, high humidity environment. For comparison purposes, tests were also conducted at a nominal 100°C in live steam (see Figure 1).

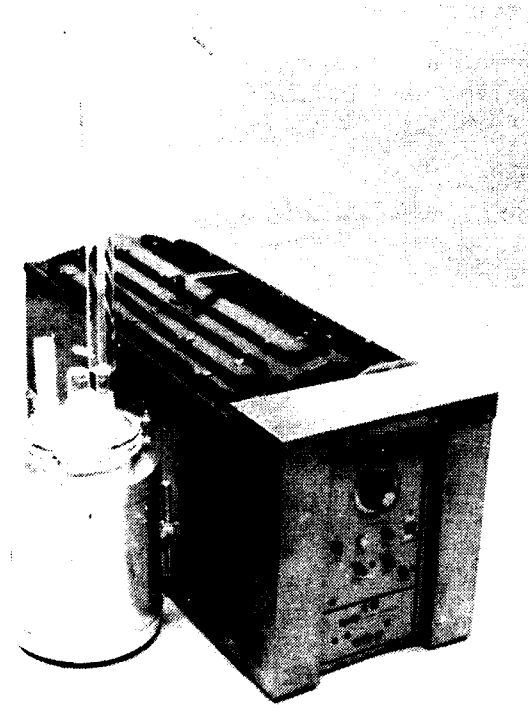


Figure 1: Steam Aging Equipment

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The full range of environments and control conditions are shown in Table 2.

TABLE 2. Aging Environments

Environment	Temperature	Relative Humidity
Controlled and conditioned air	$21 \pm 5^{\circ}\text{C}$	$60 \pm 10\%$
Non-controlled/non-recirculated air	-4 to $+32^{\circ}\text{C}$	45 to 95%
Low temperature dry	$88 \pm 5^{\circ}\text{C}$	N.A.
High temperature dry	$150 \pm 5^{\circ}\text{C}$	N.A.
Low temperature humidity	$4 \pm 1^{\circ}\text{C}$	$89 \pm 2\%$
High temperature humidity	$77 \pm 3^{\circ}\text{C}$	$92 \pm 2\%$
Steam	$97 \pm 3^{\circ}\text{C}$	100%

Test duration was chosen commensurate with the aging environment and varied from one day to 26 weeks for 'natural' environments and one hour to 168 hours for simulated 'burn in' and accelerated aging test environments.

Solderability was measured using a customized Multicore® wetting balance as shown in Figure 2. The resultant wetting curve was characterized by time to zero force, time to $\frac{2}{3}$ maximum force, and percentage of maximum theoretical wetting force achieved as shown in Figure 3 and tabulated in Table 3.

TABLE 3. Measures of Wetting Balance Solderability

Symbol	Description
T_0	Time to re-establish zero force
T_1	Time to achieve $\frac{2}{3}$ of maximum attained force
$F_{\text{Max.}}$	Maximum wetting force achieved
$\%F_{\text{Th}}$	$F_{\text{Max.}}$ as a percentage of theoretical maximum

Test conditions are detailed in the Appendix and comprise those parameters generally accepted as optimizing the discriminating ability of the Multicore® instrument.



Figure 2. Wetting Balance

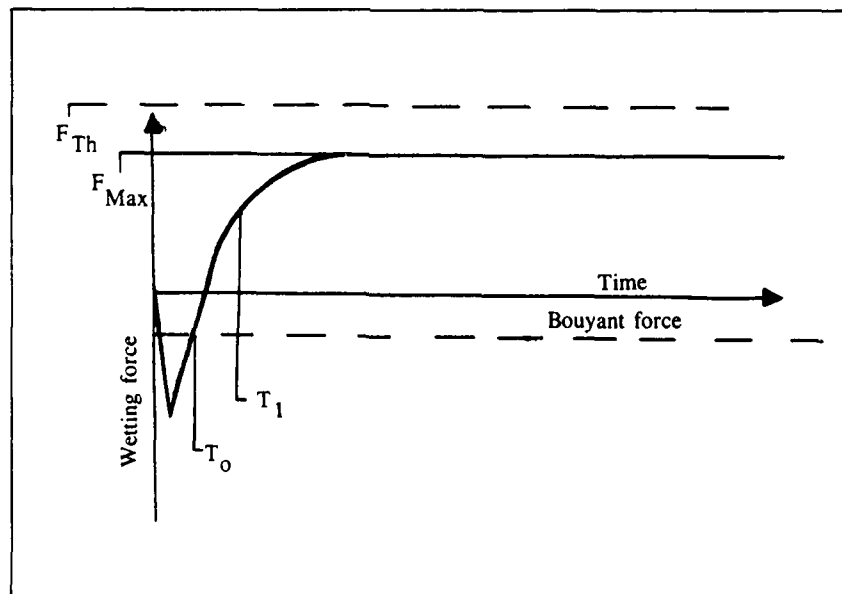


Figure 3. A Typical Wetting Balance Curve

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The samples subjected to artificial and accelerated aging environments were tested according to the various military and commercial specifications of tests, including MIL STD 202, MIL STD 883, IEC 68-2-54 and ANSI/IPC-S-805.

Samples for natural aging tests were held in a container designed by National-Standard comprised of a 6 x 6 x 6 in. box manufactured in ½ in. thick polypropylene. Each box, shown in Figure 4, was capable of holding approximately 400 wire samples for the test.

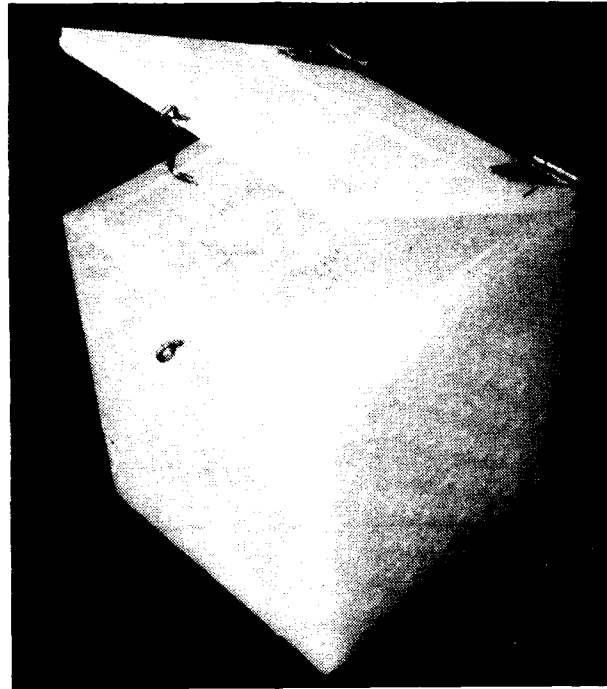
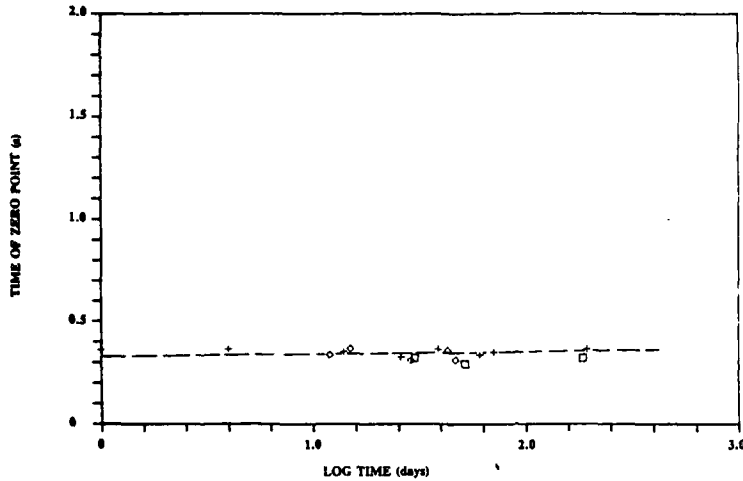
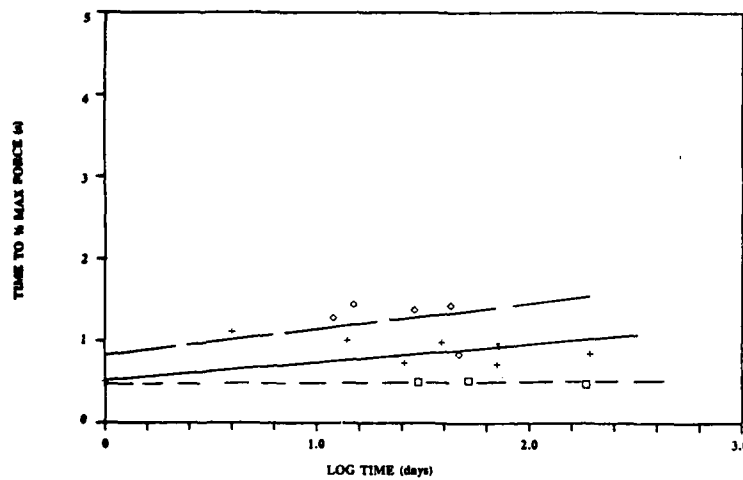


Figure 4.

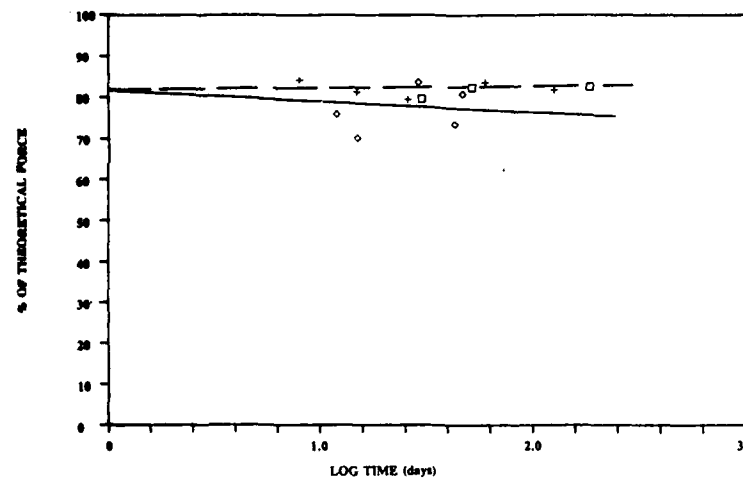
Figures 5 through 10 represent results obtained from the controlled and non-controlled natural age environments for each selected measure of solderability.



**FIGURE 5
NATURAL AGE
CONTROLLED
CONDITIONS**



**FIGURE 6
NATURAL AGE
CONTROLLED
CONDITIONS**



**FIGURE 7
NATURAL AGE
CONTROLLED
CONDITIONS**

□ AGE RESISTANT
+ ELECTROPLATED
◇ HOT SOLDER-DIPPED

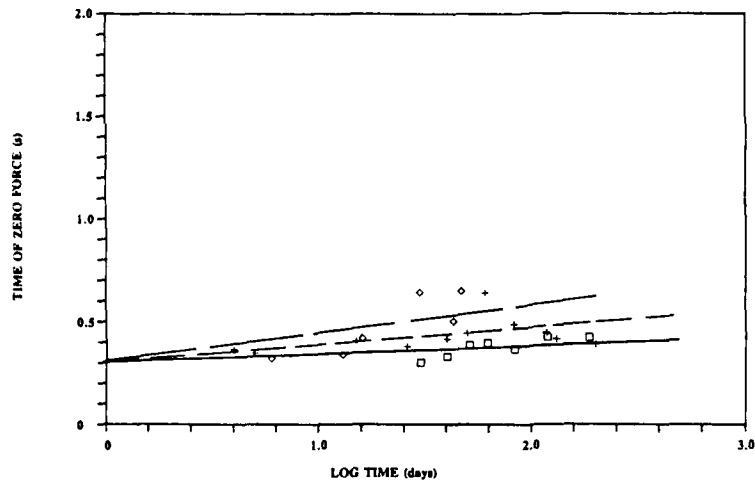


FIGURE 8
NATURAL AGE
NON CONTROLLED

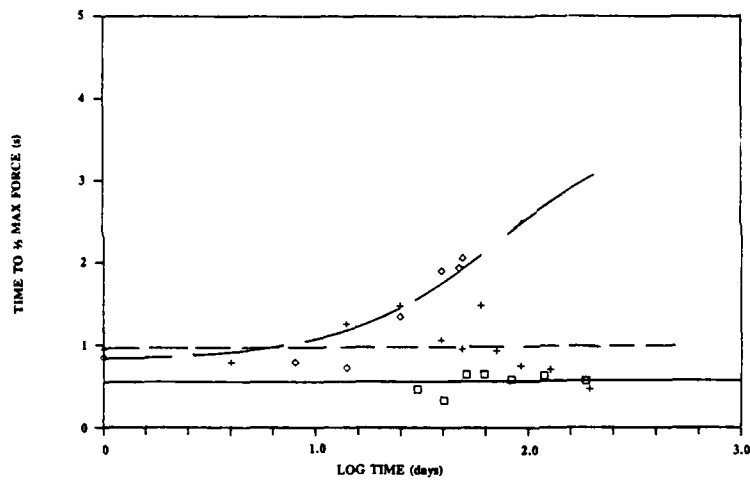


FIGURE 9
NATURAL AGE
NON CONTROLLED

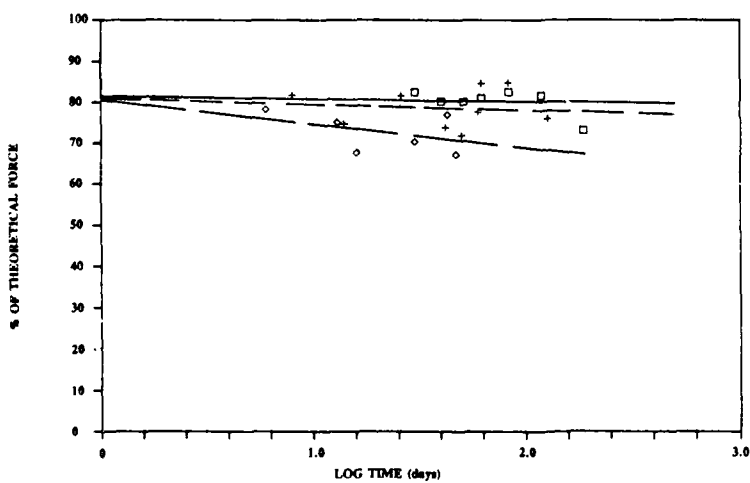


FIGURE 10
NATURAL AGE
NON CONTROLLED

□ AGE RESISTANT
+ ELECTROPLATED
◇ HOT SOLDER-DIPPED

Figures 11 through 13 show results obtained from dry aging for up to 168 hours.¹

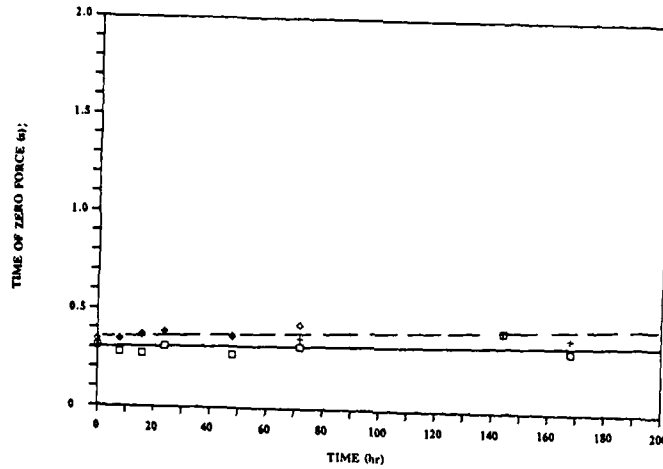


FIGURE 11
DRY AGE, 150 C

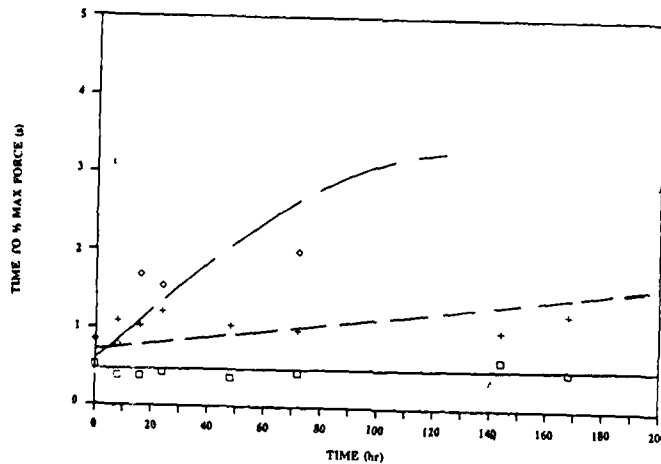


FIGURE 12
DRY AGE, 150 C

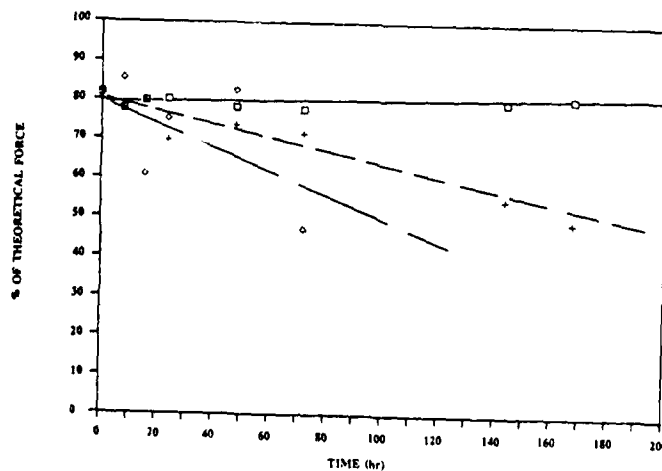


FIGURE 13
DRY AGE, 150 C

□ AGE RESISTANT
+ ELECTROPLATED
◇ HOT SOLDER-DIPPED

¹Results for low temperature humidity and low temperature dry aging have not been included in this report due to insignificant changes occurring in the test periods chosen.

Figures 14 through 16 illustrate results obtained from humidity aging, and Figures 17 through 19 represent long-term exposure to steam.¹

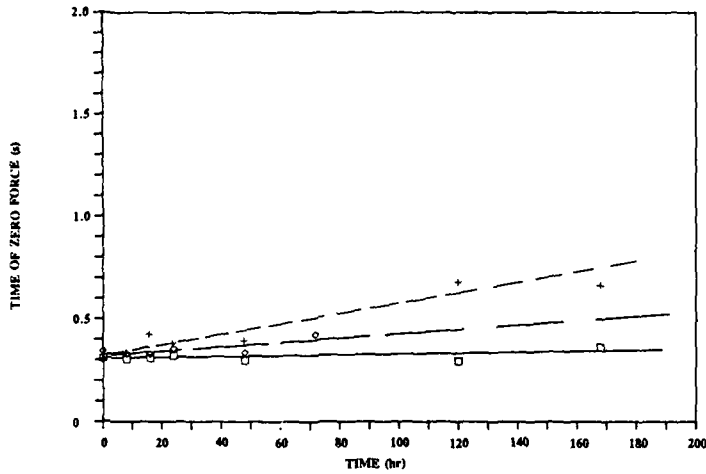


FIGURE 14
HUMIDITY AGE
77 C, 92% RH

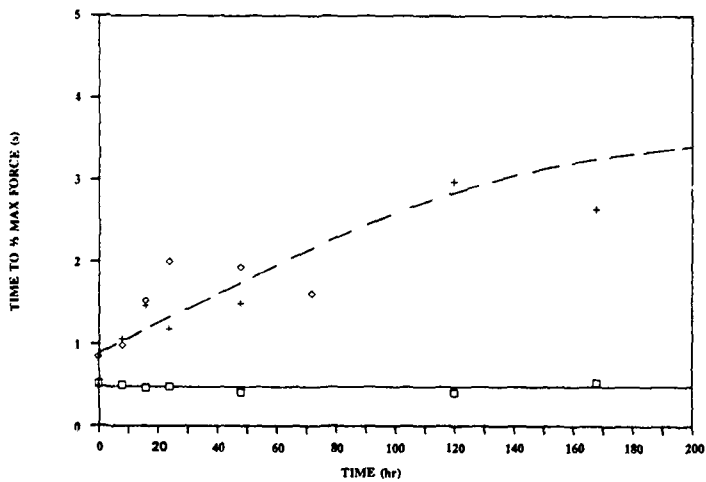


FIGURE 15
HUMIDITY AGE
77 C, 92% RH

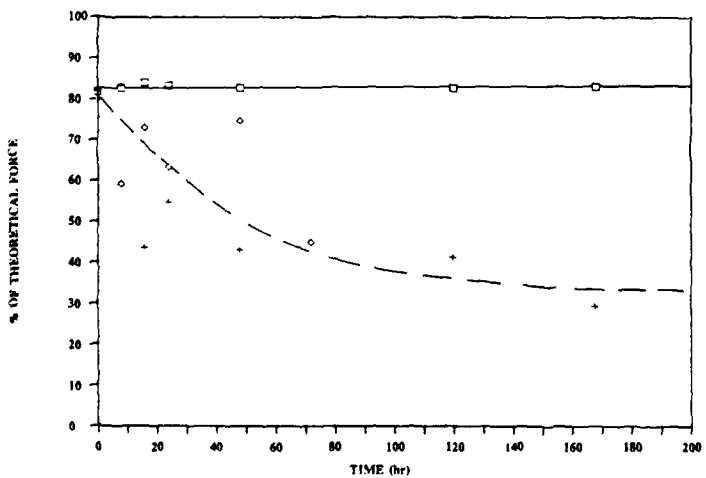


FIGURE 16
HUMIDITY AGE
77 C, 92% RH

□ AGE RESISTANT
+ ELECTROPLATED
◇ HOT SOLDER-DIPPED

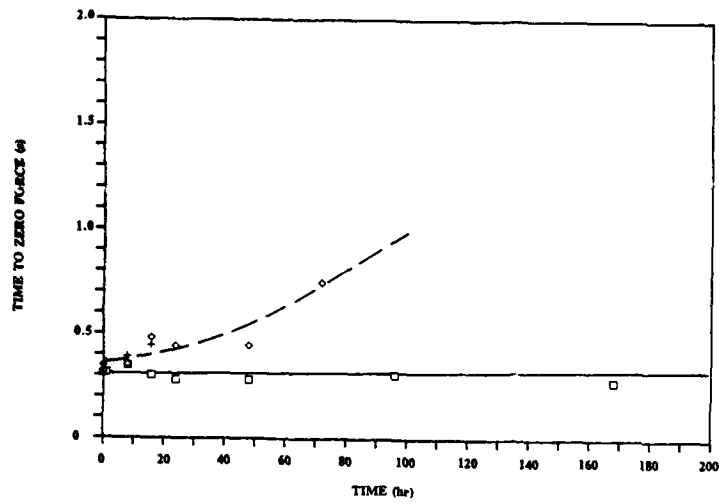


FIGURE 17
STEAM AGE

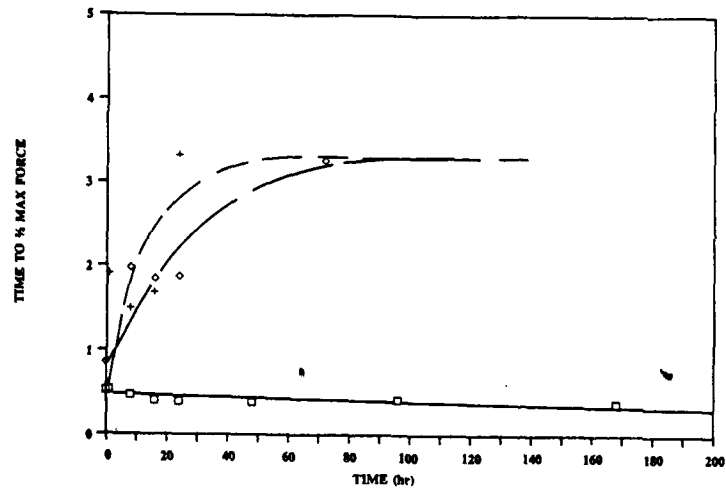


FIGURE 18
STEAM AGE

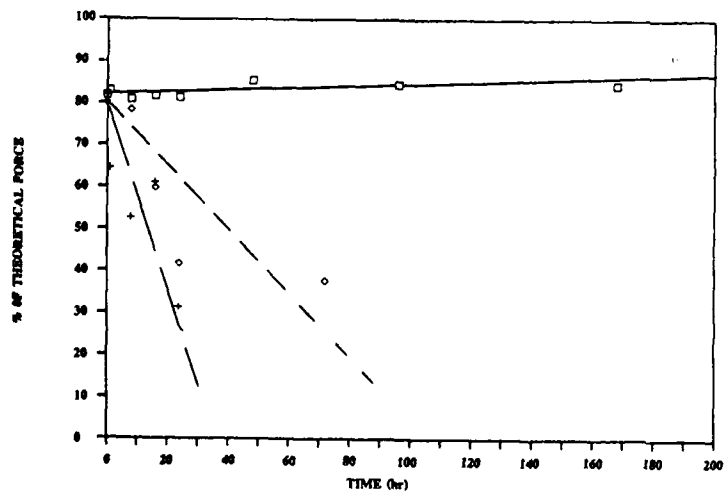


FIGURE 19
STEAM AGE

□ AGE RESISTANT
+ ELECTROPLATED
◇ HOT SOLDER-DIPPED

Figures 20 and 21 show changes in T_1 , time to reach $\frac{1}{2}$ maximum force, and $\%F_{Th}$, percentage of the maximum theoretical wetting force for a hot dipped solder finish for each environment studied.

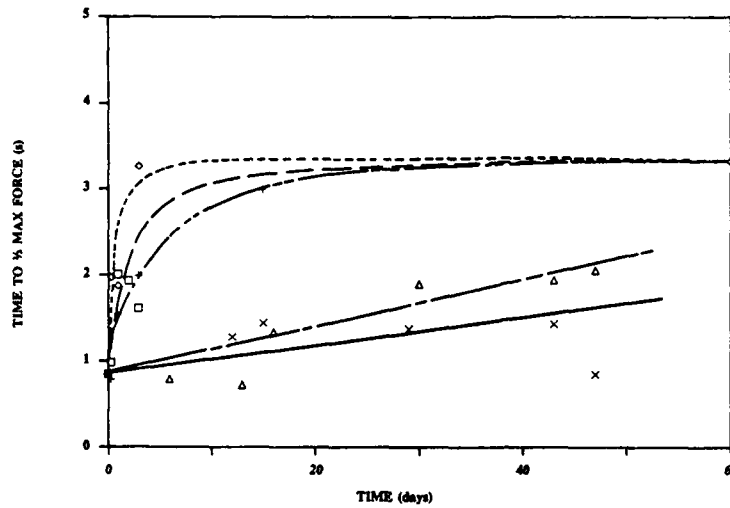


FIGURE 20
HOT SOLDER COATED

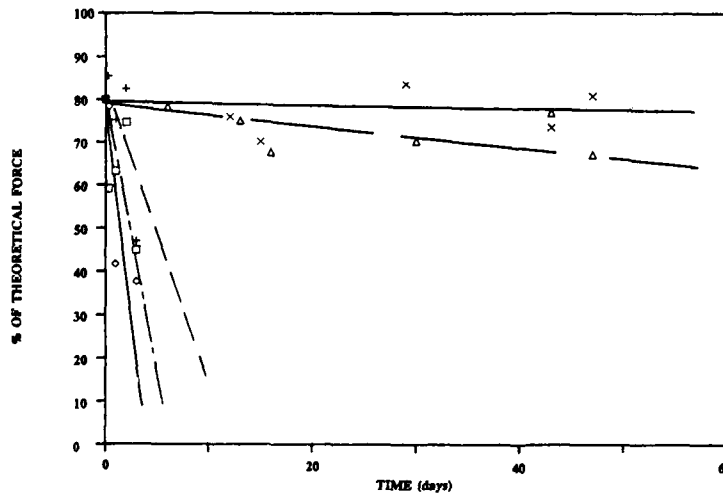
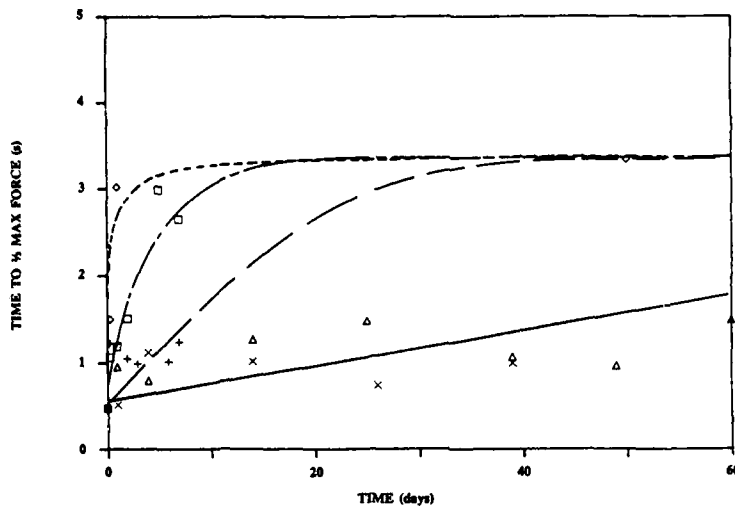


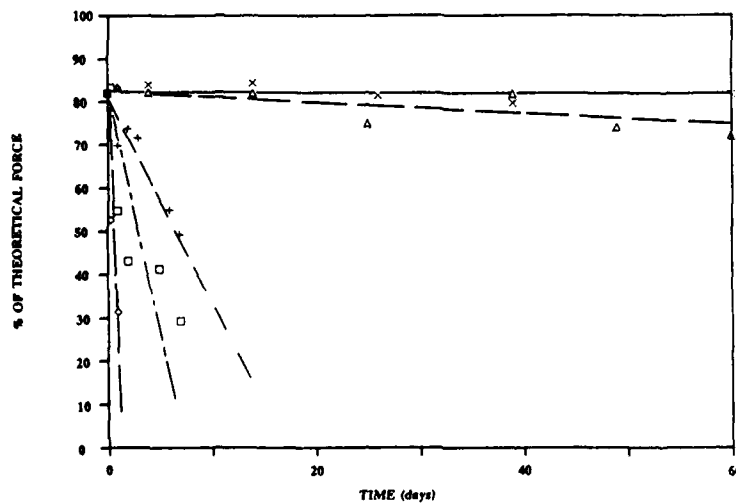
FIGURE 21
HOT SOLDER COATED

- HUMIDITY AGED
- + DRY AGED
- ◇ STEAM AGED
- △ NON-CONTROLLED
- × CONTROLLED

Figures 22 and 23 show results for an electroplated solder finish under the same conditions.



**FIGURE 22
ELECTROPLATED
SOLDER**



**FIGURE 23
ELECTROPLATED
SOLDER**

- HUMIDITY AGED
- + DRY AGED
- ◇ STEAM AGED
- △ NON-CONTROLLED
- × CONTROLLED

ANALYSIS OF RESULTS

Examination of the experimental results makes it possible to analyze how the aging environments used affect solderability. The aggressiveness of the aging environment has a marked effect on the rate of solderability loss. Each environment was ranked based on its aggressiveness in its relationship to the other environments. The ranking of environments was as anticipated with the exception of the non-controlled, non-recirculated fresh air, which was significantly less aggressive than expected. No quantitative measure ranking the environments has been attempted, however, qualitatively they can be ranked from less aggressive as follows:

1. Controlled, conditioned air
2. Non-controlled, non-recirculated fresh air
3. Dry aging
4. Humidity aging
5. Steam aging

Further analysis of the data shows that as the aggressiveness of the environment increases, the test procedure becomes less discriminating. This can be seen when comparing differences between hot solder-dipped material and electroplated materials in a given environment. For example, comparison of these materials in a benign environment shows distinct differences between the loss in solderability for each; whereas the same materials in an aggressive environment show little or no distinction in results.

Comparison of material performance was also possible with the data obtained. Results show that each of the three lead finishes reacted consistently to the various environments independent of the parameter used to measure solderability. 'Age resistant' solders performed well in all of the given environments, with virtually no loss in solderability seen in this material. Hot solder-dipped and electroplated solder materials reacted similarly in both steam and high temperature humidity aging environments. However, in steam aging environments, it appeared that hot solder-dipped material had a superior performance to electroplated solder. Under less hostile (natural aging) conditions, electroplated solder out performed hot solder-dipped material and showed superior resistance to loss in solderability.

The parameters used to measure solderability allow conclusions about their usefulness for evaluating material and environment performance. Results from this experiment suggest that all three measures of wetting balance solderability, time to zero force (T_0), time to $\frac{2}{3}$ of maximum force (T_1), and percentage of theoretical maximum force ($\%F_{Th}$) are indeed necessary to adequately describe solderability.

The most suitable parameter for any particular application is dependent upon the discriminating power needed and the test environment used. Where a high degree of sensitivity is not required and a very aggressive environment is used to accelerate the test, any or all of the parameters may be chosen. In contrast, discrimination between materials in benign environments appears to be best characterized using either time to achieve $\frac{2}{3}$ of maximum force (T_1) or maximum percentage of theoretical force (F_{Th}).

For example, if a test does not require a high degree of sensitivity and the materials are known to be significantly different, e.g. hot solder-dipped vs 'age resistant' solder material, a steam-age test may be performed and any of the three parameters used. Conversely, if a test requires sensitivity, as in a comparison of hot solder-dipped and electroplated material, in most cases a less aggressive environment should be used in conjunction with time to reach $\frac{2}{3}$ of maximum force (T_1) or percentage of maximum theoretical force ($\%F_{Th}$).

CONCLUSIONS

1. The aggressiveness of the aging environment had a marked effect on the rate of solderability loss.
2. The more aggressive the environment, the less discriminating the test procedure becomes.
3. The ranking of environments from benign to aggressive is as expected with the exception of the non-controlled, non-recirculated fresh air which was significantly less aggressive than expected. This confirms similar results recently reported in the published literature.
4. The results indicate that all three measures of wetting balance solderability, T_0 , T_1 , and $\%F_{Th}$ are required to comprehensively describe solderability. The most suitable measure for any particular application is strongly dependent upon the discriminating power needed and the test environment used. Solderability testing in very aggressive environments where high sensitivity is not required, can be adequately measured using all or any single attribute. Testing in less aggressive environments, suggest T_1 and $\%F_{Th}$ as the best measure of loss in solderability.
5. Results show that different lead finishes react consistently to the various environments, independent of the attribute used to measure solderability. 'Age resistant' solder finishes appear to be remarkably resistant to aging, independent of the aging environment. Under the most aggressive environmental conditions (steam and high temperature humidity) electroplated solders appear to show a higher rate of solderability loss than hot solder dipped leads. Under relatively benign conditions, electroplated solders show marginally superior resistance to aging.
6. As with most accelerated test procedures, some caution needs to be exercised in drawing correlations between performance under accelerated testing and behavior under normal storage conditions. It is clear, however, that the currently accepted accelerated aging environments of steam and high humidity are reasonably good at predicting natural aging phenomena.

ACKNOWLEDGEMENTS

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APPENDIX

Buoyant Force (F_b)

$$F_b = \rho g V \quad (1)$$

ρ = Density of solder (8155 Kg.m^{-3})

g = Gravitational constant

V = Volume of solder displaced by lead

Force at $\frac{2}{3}$ Maximum Force ($F_{2/3}$)

$$F_{2/3} = \frac{2}{3} (F_{\text{Max}} + F_b) \quad (2)$$

F_{Max} = Maximum Force value attained

Time to $\frac{2}{3}$ of Maximum Force (T_1)

$$T_1 = \text{Time Value at } F_{2/3} \quad (3)$$

Theoretical Maximum Force (F_{Th})

$$F_{\text{Th}} = 490 (\mu\text{N.mm}^{-1}) \times P \quad (4)$$

P = Perimeter of Lead

Surface energy = 0.49 J.m^{-2}

Percentage of Theoretical Maximum Force

$$\%F_{\text{Th}} = \frac{F_{\text{Max}} \times 100}{F_{\text{Th}}} \quad (5)$$

Wetting Balance Parameters

Immersion /Extraction Speed	= 20 mm.s^{-1}
Depth	= 2.5 mm
Duration	= 5.0 s
Bath Temperature	= 245°C
Flux Type	= Alpha®, 40% Solids
Specimen Diameter	= 0.500 mm
Number of Tests per Data Point	= 3 Averaged

BIBLIOGRAPHY

- Allen, B.M., *Testing for Solderability: Part 1 & 2*, Connection Tech., May/June 1986, pp 35-42
- Davy, J.G., *Wetting Balance Solderability Testing for Electronic Components at Receiving Inspection*, 10th Annual Soldering/Manufacturing Seminar Proceedings, 1986
- Davy, J.G., and Skold, R., *Computer-Aided Solderability Testing for Receiving Inspections*. Circuit World, 1985, 12, (1), pp 34-41
- Devore, J.A., *The Use of Wetting Balance Data to Predict Soldering Materials Performance and Soldering Process Parameters*, 11th Annual Electronics Manufacturing Seminar Proceedings, 1987
- Devore, J.A., *Solderability*, The Journal of Metals, July 1984
- Edgington, R.J., and Worrell, C.W., *Measuring Solderability*, Connection Technology, February 1987
- Fenawire, D.L.; Wolverton, W.M.; Spitz, D.; Burkett, A.; Russell, W.; and Waller, B., *Today and Tomorrow in Soldering*, 11th Annual Electronics Manufacturing Seminar Proceedings, 1987
- Geiger, A.L., *Solderability of Capacitor Lead Wires*, 10th Annual Soldering/Manufacturing Seminar Proceeding, 1987
- Lish, E.F., and Weber, J.O., *Solderability Testing of Leaded and Leadless SMDs by Means of a Modified Wetting Balance*, 11th Annual Electronics Manufacturing Seminar Proceedings, 1987
- Wild, R.N., *Component Lead Solderability vs. Artificial Steam Aging (Status Report II)*, 11th Annual Electronics Manufacturing Seminar Proceedings, 1987
- Wild, R.N., *Component Lead Solderability vs. Artificial Steam-Aging*, 10th Annual Soldering/Manufacturing Seminar Proceedings, 1986

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INTERMETALLIC COMPOUND GROWTH IN TIN AND TIN-LEAD PLATINGS
OVER NICKEL AND ITS EFFECTS ON SOLDERABILITY

BY

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ABSTRACT

The growth rates for stable Ni-Sn intermetallic compounds (IMC) are much lower than those for Cu-Sn IMC. Therefore, Ni appears to be a good choice for a diffusion barrier between Cu and Sn. However, growth of a metastable plate-like IMC is a potential cause for long-term solderability degradation. This IMC has an approximate composition NiSn_3 , which does not correspond to any of the stable Ni-Sn IMC's on the equilibrium phase diagram. A long-term low-temperature aging study confirmed the undesirable effects of NiSn_3 growth upon solderability. Consequently, the growth rates for NiSn_3 were studied as a function of aging temperature, lead content, and plating type, and were found to be affected by all of these variables. Lead was determined to reduce the NiSn_3 growth in matte Sn-Pb. The growth rate reaches a maximum between 100°C and 140°C and then decreases. This behavior is indicative of a metastable phase, and so is the composition. Differential scanning calorimetry measurements determined that NiSn_3 indeed is a metastable phase which rapidly transforms into stable IMC's and free tin at temperatures above the tin melting point. The kinetic parameters of NiSn_3 transformation were calculated using data from isothermal DSC measurements, and a time-temperature-transformation (T-T-T) diagram was constructed using these kinetics parameters. The implications of the findings on solderability, soldering techniques and accelerated aging testing for tin-based platings over nickel underplating are discussed. Also discussed is the work to determine the actual mechanisms of solderability deterioration.

INTRODUCTION

The growth of intermetallic compounds in various platings affects solderability, and is one of the main factors in determining the shelf life of plated components. It has been known for several decades that the formation of certain intermetallic compounds (IMC's) in tin and tin-base platings can have an undesirable effect resulting in a serious degrading of component solderability. Consequently, a considerable research effort was undertaken by the plating industry to understand the formation and growth of IMC's, and, if possible, to control the undesirable effects.

Ni has been successfully used as a diffusion barrier to prevent interdiffusion of Cu and Au. This success prompted considerations of using Ni as a barrier between Cu and Sn to prevent growth of Cu-Sn intermetallics and to prolong the shelf life of plated parts. Initially, there were some indications that growth rates of Ni-Sn intermetallics are very low. Since the early seventies, there were several investigations of Ni diffusion barrier performance for Sn-based platings (References 1-4). The results obtained by these authors indicated a rather complex behavior.

There are three IMC's in the Ni-Sn binary system, all stable at room temperature: Ni_3Sn_4 , Ni_3Sn_2 , Ni_3Sn (Reference 5). Early work indicated that out of these three intermetallics, only Ni_3Sn_4 is present. The growth rates of Ni_3Sn_4 at 70°C were found to be much smaller than those of Cu-Sn intermetallics (References 2,3), and, our results confirm this (See Figure 1). However, together with the slow growth of Ni_3Sn_4 , an extremely fast growth of an intermetallic of unknown nature was detected (References 1,3). The composition of this intermetallic roughly corresponds to NiSn_3 , which cannot be identified with any of intermetallics on the phase diagram.

The characteristic platelet morphology of this compound is shown in Figure 2. It has been suggested that the extremely fast growth of this intermetallic can cause deterioration of solderability (Reference 3). This happens when the platelets penetrate all the way through the tin layer to the surface and then oxidize. Therefore, from the practical

point of view, it is important to be able to control this undesirable growth.

At the start of our research on NiSn_3 the knowledge about the compound was rather limited. We knew that it grew in significant amounts only at lower temperatures, below approximately 160°C . Above this temperature, only a continuous layer of Ni_3Sn_4 had been observed. NiSn_3 grew in a large variety of platings. The growth of the compound was the largest in bright tin over bright nickel platings, and the lowest in matte Sn over sulphamate Ni (Reference 3). Another study found that it was not possible to control the occurrence or growth rate of the compound by variation in plating parameters, both for tin and nickel. The occurrence of the compound was either eliminated or greatly reduced in non-plated layers (Reference 6).

This paper can be divided into four parts. The first part is a brief description of a long-term low-temperature solderability study for matte tin over Cu and electroplated Ni. The second part presents results of our study of short-term growth rates of NiSn_3 . The third part describes the work on the thermal stability of NiSn_3 . And finally, we will discuss how what we learned about this intermetallic was applied to the determination of actual mechanism of solderability deterioration and ways to improve solderability.

1. LONG-TERM LOW-TEMPERATURE AGING SOLDERABILITY STUDY

The purpose of the study was to assess the effects of low-temperature aging on solderability of matte tin and tin-lead platings over copper and electroplated nickel. The variables were: (a) composition - 100% Sn, 90% Sn - 10% Pb, 60% Sn - 40% Pb (all wt.%); (b) temperature - 24°C (room temperature) and 50°C (maximum warehouse temperature); (c) time - samples taken out for testing at 6 month intervals, up to 24 months. Plating thickness was $200 \pm 50\mu$ ", underplating (Ni) thickness was about 100μ ", substrates were pure copper.

Solderability testing was done by two methods. First is the test procedure for estimating solderability of metallic surfaces, a dip test,

using non-activated rosin flux. The required coverage to pass the test is 95%. Table 1 represents results of the test. We can see that tin-lead over nickel has the best solderability. These results show a trend, but are somewhat subjective, since they depend on the operator's judgement. Therefore, a second method was used, the meniscograph, or wetting balance (Reference 7). Two characteristics were employed to evaluate solderability: the final value of wetting force and the time to cross zero line. Results for samples aged for 2 years are presented in Table 2 (Reference 7). These results contradict to some extent the results of the first test, since both kinds of underplating display solderability of the same order.

To investigate the cause of the solderability failure, all samples were cross-sectioned to reveal IMC growth. Such cross-sections for matte Sn, 90% Sn - 10% Pb and 60% Sn - 40% Pb (all over Ni underplating) are shown in Figures 3a, b and c. For matte Sn and 90% Sn - 10% Pb, the intermetallic consists of a thin continuous layer, Ni_3Sn_4 , and discontinuous "needles" (actually, platelets), NiSn_3 . Addition of 10% Pb greatly reduces the amount of NiSn_3 and the addition of 40% Pb practically eliminates it. This correlates well with solderability testing results. Most likely, the thin layer of Ni_3Sn_4 does not affect the solderability at all, and all the detrimental effects come from NiSn_3 , particularly if it grows all the way to the surface or close to the surface. Another interesting phenomenon that was found in this study was the effect of preaging at a higher temperature. Figures 4a and b show this decrease in the NiSn_3 IMC for 100% Sn samples. The decrease is the result of preaging at 155°C for 8 hours. Samples were consequently aged at room temperature for 1.5 years. Figures 5a and b show the same effect for the 90% Sn - 10% Pb sample; preaging nearly eliminated subsequent NiSn_3 growth.

2. STUDY OF NiSn_3 GROWTH RATES

The purpose of this study was the determination of the growth rates of the NiSn_3 compound from 75°C up to the melting point in matte Sn and 75% Sn - 25% Pb (wt.%) platings, and in particular, the temperature region in which the growth rates are at their maximum.

This objective is important in establishing the time frame for the aging tests. The maximum growth rates can be used for accelerated aging tests.

The variables in our test were aging temperature and composition of the tin alloy plating. The temperatures varied from 75°C to 225°C. Isochronal anneals at three temperatures were performed at a single time, with annealing times starting from 16 days for 75°C, 100° and 125°C anneals, and down to 2 days for 210°C and 225°C anneals. These times were chosen to allow sufficient growth of intermetallic at appropriate temperatures, so that the growth rates at various temperatures can be easily compared.

Substrates suitable for metallographic examination and scanning electron microscopy were prepared from copper strip. They were plated with Ni using a sulfamate bath operated at 60°C and 40 ASF. Then half of the substrates were plated with matte Sn, and the other half with 75% Sn - 25% Pb. Matte Sn was plated using a stannous sulfate bath at room temperature and 40 ASF, and matte Sn-Pb was plated using a fluoborate system at room temperature and 40 ASF. The baths used were standard baths from our manual plating line.

All aging treatments were performed in Blue M air circulating ovens. The aged samples were analyzed in two ways. Some of them were mounted, cross-sectioned and etched to reveal the intermetallic. The others were stripped of remaining free tin in the International Tin Research Institute (ITRI) stripping solution for consequent examination by optical and scanning electron microscopy. Tin stripping is much less time consuming than cross-sectioning and, therefore, can be used for fast analysis of a large number of samples.

Both cross-sectioning and tin-stripping produced similar results for matte Sn samples. The size of the platelets increases up to 125°C (Figure 6) then stays relatively constant up to 155°C (Figure 7) and then decreases (Figure 8). The number of platelets continually declines with rising temperature. No platelets were observed in cross-sections above 175°C. The tin stripping method is more sensitive: single platelets are still observed at temperatures as high as 195°C (Figures

9,10). It is likely that crystals observed at high temperatures nucleated and partially grew at room temperature during the time that passed between plating and annealing (several months), and then went through fast growth during heating up to the aging temperature (several minutes). The orientation of platelets seems to be random.

In the case of matte 75% Sn - 25% Pb plating, the number and size of the platelets were not large enough for the platelets to be observed in cross-sections by optical microscopy. First of all, this confirms our previous finding that lead drastically decreases both the density of the platelets and the rate of their growth. Otherwise, the growth is very similar to that in matte Sn. The size of crystals increases and density decreases up to 125°C (Figure 11). Then the amount of intermetallic stays relatively constant up to 145°C, and drops at 155°C (Figure 12).

The total mass of NiSn_3 IMC, which is a product of the density of platelets and their average size, will peak at some intermediate temperature, most likely between 100°C and 125°C. This behavior has two probable causes. First, if NiSn_3 nucleates at the Ni-Sn interface at a higher temperature, it has to compete with nucleation and growth of Ni_3Sn_4 . But this does not account for the complete disappearance of NiSn_3 after aging above 200°C. This disappearance can be explained by the second cause, the instability of NiSn_3 at these temperatures. As we will describe in the next part, NiSn_3 is not a thermodynamically stable phase. At elevated temperatures it transforms by decomposing into free tin and stable tin-nickel IMC's.

3. STUDY OF DECOMPOSITION PARAMETERS OF NiSn_3

3.1 THERMAL STABILITY OF NiSn_3

The transformation of NiSn_3 at higher temperatures was studied by differential scanning calorimetry (DSC). The intent has been to characterize the thermal stability of the NiSn_3 IMC.

The weight of a DSC sample has to be anywhere from 1 to 10 mg. Under normal aging conditions, (i.e. single-temperature aging, reasonable aging time) the amount of intermetallic in aged plating will not be sufficient for DSC work. Therefore a special two-step aging was

used based on our previous findings about the NiSn_3 growth rates. First, the samples were aged at 75°C for two months to nucleate and start growing NiSn_3 crystals. Second, they were aged for one to two and a half months at 125°C to increase the crystals' size to maximum. Two kinds of samples were aged in such manner: matte Sn over sulfamate Ni underplating and bright Sn over bright Ni underplating. The second sample's choice was based on work that reported the highest NiSn_3 growth in such samples (Reference 6). The first sample produced a large quantity of IMC; the concurrent growth of stable IMC was minimal (Figure 13). The second sample (bright Sn) produced amounts sufficient for DSC measurement, but not as large, and concurrent growth of stable IMC was substantial. It was found afterward that the second step temperature (125°C) was too high for that sample - aging below 100°C produces much better results.

The aged samples (coupons $1" \times 1"$) were stripped of free tin using the ITRI stripping solution. The DSC samples were prepared by carefully scraping the IMC from the substrates into the DSC's aluminum sample pans.

A typical DSC scan for the NiSn_3 intermetallic is shown in Figure 14. The sample, in this case, was grown in matte Sn over sulfamate Ni. Figure 15 is a typical scan of decomposed IMC sample (i.e. second scan). A pure tin sample scan is used as a standard to calibrate temperature. The onset of the peak (i.e. melting point) is about 503K. The actual melting point of tin is 505K, so the temperature scale must be corrected by two degrees for this particular scan rate, 40K/min. (In the following discussion, all temperatures are corrected.) A DSC scan for "matte Sn" IMC sample (Figure 14) has a peak with onset at about 513K, eight degrees higher than melting point of tin (in Figures 14 through 18 the corrected temperature is in parentheses). The difference between the tin melting point (standard) and the IMC peak onset decreases with decreasing scanning rate. Figure 16 shows scan for NiSn_3 at a lower scanning rate. The difference between tin melting point and onset is about three degrees. The shift of the peak to lower temperatures with

decreasing scanning rate is characteristic of a metastable phase that transforms by a thermally activated process.

The IMC NiSn_3 decomposes into tin and stable intermetallic compounds. This was confirmed by x-ray diffraction of the decomposed sample, which detected mostly tin and also Ni_3Sn_2 and Ni_3Sn_4 (Reference 8). It was also confirmed by SEM microprobe that detected Sn and Ni_3Sn_4 only. Therefore the peak, observed upon second and following scans is produced by tin that resulted from NiSn_3 decomposition (Figure 15). However, the onset of the peak in Figure 15 (at 503.2K) is 1.9 degrees lower than for pure tin at the same scanning rate. There are two likely reasons for this shift. First, the product of decomposition is not pure tin but tin-nickel eutectic. The melting point of this eutectic is 504K, one degree below that of tin. The observed melting point is shifted down by about 1K more because the sample is in the form of fine powder, so the surface energy component of the free energy becomes important.

Figure 16 also illustrates another feature of NiSn_3 , a small peak before the IMC peak. The onset for this peak is at 503.2K, similar to that of the fully decomposed sample in Figure 15. Hence, that peak was attributed to tin that evolved as result of partial decomposition of NiSn_3 below 503K. This assumption was checked by scanning the temperature part way into the IMC peak and thus partially decomposing the intermetallic (Figure 17), then cooling the sample and performing the second scan all the way through the IMC peak (Figure 18). It can be seen that the first, partial scan resulted in a large increase of the first peak, thus confirming that the first peak is the tin peak.

3.2 KINETIC PARAMETERS OF NiSn_3 DECOMPOSITION

Most isothermal reactions in solid metallic phases are described by the Mehl-Johnson-Avrami (M-J-A) equation (Reference 9):

$$x = 1 - \exp [-(kt)^n] \quad (1)$$

where x is the fraction of material transformed at the time t , n is a dimensionless exponent, and k is the reaction rate. k changes with temperature exponentially (Arrhenius type of relation):

$$k = k_0 \exp \left(- \frac{E}{RT} \right) \quad (2)$$

where E is the activation energy, k_0 the frequency factor, R the gas constant and T the temperature (Kelvin). The equation (1) can be rewritten as:

$$\ln \ln \left(\frac{1}{1-x} \right) = n \ln t + n \ln k \quad (3)$$

Therefore, if x vs t is plotted in coordinates $\ln \ln \left(\frac{1}{1-x} \right)$ vs $\ln t$, the parameters n and k can be measured directly from the plot: n is the slope of the plot, and $n \ln k$ is the intercept. The DSC technique does not measure fraction x directly; instead, dx/dt (the x derivative with time) is measured. The measurement produces a curve as those in Figure 19. The transformed fraction x at time t can be determined as the ratio of area under the curve up to time t (hatched) to the total area under the curve. If this fraction x is plotted as $\ln \ln \left(\frac{1}{1-x} \right)$ vs $\ln t$, we obtain plots as in Figure 20. It is linear at lower values of t , but deviates from linearity at higher times indicating a lower transformation rate than that expected according to M-J-A equation. This non-linearity at high values of t is most likely due to the restriction of crystal growth by the small size of the analyzed NiSn_3 particles (Reference 10). It must be noticed that as a rule the nonlinearity becomes significant at around $x = .8$, i.e. when the 80% of NiSn_3 is decomposed. Therefore, the use of M-J-A equation is still justified. After the kinetic parameters are determined, we calculate the fraction of transformed material as a function of time at isothermal conditions (Figure 23). From that, the time-temperature-transformation (T-T-T) diagram can be calculated (Figure 24).

Samples. The sample used in this study was NiSn_3 grown in matte Sn plated over sulfamate Ni. A substantial amount of the sample was produced by two-stage aging. Unfortunately, there was not enough of the original sample, aged at 75°C for 2 months and consequently at 125°C for 2 months. Therefore, another sample, aged at 75°C for 2 months and at 125°C for 2.5 months was used to extend the temperature range of measurements from 517K to 521K. Another similar sample, aged at 75°C

for 2 months and then at 125°C for 1 month, was used to confirm the results of the first series of measurements. The weights of samples used in this study were between 2 and 5 milligrams.

Isothermal DSC. The Differential Scanning Calorimetry is not normally used for isothermal measurement. However, our DSC apparatus can be set up for isothermal runs. Usually, the specimen was heated up to about 40K below the temperature of isothermal run and equilibrated at this temperature. Then it was heated as fast as possible to the temperature of the run (anywhere from 505K to 521K). Data acquisition was started immediately after reaching the working temperature. The main problem in isothermal DSC is the initial instability because of high heating rate prior to the start. This instability was partly overcome by using larger samples. The very initial part of the DSC runs was determined by extrapolation to the baseline at time $t = 0$. The data were stored and then plotted out in an appropriate scale. The plots were digitized using an HP digitizer, and then stored for further analysis.

The typical isothermal DSC curves are shown in Figure 19 which covers the whole range of temperatures used. Using these data, the fraction x was calculated and then plotted in coordinates $\log \log \left(\frac{1}{1-x} \right)$ vs $\log t$, where the logarithm with base 10 is used. These plots are shown in Figure 20. The Avrami plots were used to calculate parameters n and k . The average value of the parameter n is 1.5. The reaction rate k is plotted in Figure 21. It has an Arrhenian dependence, as expected. Using the determined n and k , the transformed fraction was calculated. Figures 22a, b and c show the calculated decomposition curves together with data: the fits are very reasonable. Figure 23 is the same plot, but for a wider range of temperatures, using extrapolated values of k from Figure 21. And finally, Figure 24 presents a T-T-T diagram calculated using Figure 23. The left boundary of the T-T-T diagram represents the beginning of transformation (5% decomposed), and the right boundary - the completion of transformation (95% decomposed).

4. METASTABLE IMC: ENGINEERING IMPLICATIONS

4.1 EFFECTS ON SOLDERABILITY

Since the stable IMC Ni_3Sn_4 grows very slowly at room temperature, the deterioration of solderability in tin platings with nickel underplating is caused by fast growth of metastable NiSn_3 . The exact mechanism of deterioration is not clear at the moment; the most likely cause is oxidation of NiSn_3 near or at the surface of the plating (Reference 3). The metastability of NiSn_3 might offer an opportunity to offset the undesirable effects by adjusting the process variables. The amount of stable intermetallic after NiSn_3 decomposition is much less than the amount of original NiSn_3 . For example, 1 gram of NiSn_3 will decompose into .2 gram of Ni_3Sn_2 , .2 gram of Ni_3Sn_4 and .6 gram of tin. Therefore, the soldering process that exposes the intermetallic to high enough temperature for a sufficient time to decompose NiSn_3 might result at least in a partial restoration of solderability. Below, we will briefly describe the work on determining the actual mechanism of solderability deterioration, and ways to overcome the deterioration. Based on work to date, some trends are already evident.

As we can see from the T-T-T diagram (Figure 24), NiSn_3 will fully transform at 260°C in less than one second, while at 215°C it will take about 10^5 seconds (i.e. about 28 hrs.). Samples were aged (using two-step aging) to produce large intermetallic growth and then tested for solderability at these temperatures (5 sec. dip). The 215°C samples have large non-wetted areas, and the wetted areas display a lot of surface irregularities (Figure 25). Wetting is much better for 260°C samples, but again there are a lot of surface irregularities ("bumps"). The cross-sections of the test samples reveal that these "bumps" are caused by needle-like IMC in the solder layer (Figure 26). The IMC compositions were analyzed by microprobe. For 260°C , the compositions correspond to Ni_3Sn_4 ; NiSn_3 is definitely absent. In 215°C samples, the IMC is NiSn_3 . Thus, just raising the temperature is not enough to insure good solderability, since the products of NiSn_3 decomposition cause a lot of surface irregularities.

Indeed, raising the temperature to 275°C did not substantially

improve the surface appearance. The increase of dip time from 5 sec. to 30 sec. (to allow the decomposition products to float off) had only a marginal effect. The best results were achieved by the combination of time and temperature adequate for nearly full decomposition of NiSn_3 (10 sec. at 245°C , Figure 24), combined with sample movement in the solder, to facilitate the removal of decomposition products. Figure 27 shows these test samples; movement of the samples markedly improved the regularity of the surface. The representative cross-sections are shown in Figure 28; the IMC is nearly absent in the samples that were moved.

Based on these tests, it is possible to predict how NiSn_3 intermetallic will affect solderability in various soldering processes. In wave soldering, at a solder wave temperature of 255°C it will decompose in less than a second, and at 265°C - in less than .1 sec.; this is combined with the movement of the solder. On the other hand, at the vapor phase reflow temperature, 215°C , it will take about 28 hours to fully decompose the intermetallic. Therefore, the presence of NiSn_3 might be acceptable in the case of wave soldering, but will be unacceptable for vapor phase reflow.

4.2 ACCELERATED AGING

The growth rates of NiSn_3 IMC go through a maximum at temperatures between 100°C and 140°C , depending on the plating's type. This fact, coupled with the metastability of the NiSn_3 IMC, dictates caution in the use of conventional accelerated aging. The high-temperature aging, above 140°C , may not be used at all, since it will not detect the potential for NiSn_3 growth at lower temperatures.

The morphology of growth (particularly density of growth) at temperatures higher than 100°C may differ from that at room temperature or slightly above. Due to complexity of the situation, a new approach such as two-step aging, may be appropriate. This aging will be similar to the aging used to grow DSC sample (see Section 3.1). During the first, low-temperature step (anywhere from 50°C to 100°C) small crystals of NiSn_3 will nucleate and start to grow. During the second,

high-temperature step (anywhere from 100°C to 140°C) these crystals will undergo fast growth. It was already demonstrated that such aging can produce NiSn_3 with both large crystal size and high growth density. This kind of IMC growth is similar to that produced during long-term natural aging.

CONCLUSIONS

Solderability of matte tin platings over nickel underplating, stored at room temperature or slightly above, deteriorates after a relatively short time. This deterioration is not caused by the growth of stable Sn-Ni IMC's, which is extremely slow, but by the fast growth of a metastable NiSn_3 IMC. NiSn_3 grows in the form of platelets. The number of platelets per unit area continually decreases with increasing temperature. The average size reaches a maximum around 125°C and decreases above 155°C. The addition of 10% Pb greatly reduces NiSn_3 growth, and the addition of 40% Pb practically eliminates it.

It was determined by differential scanning calorimetry (DSC) that NiSn_3 is a metastable phase which decomposes into free tin and stable Sn-Ni IMC's. Isothermal DSC was used to calculate the kinetic parameters of the NiSn_3 transformation, and a time-temperature-transformation (T-T-T) diagram was constructed using these parameters. This diagram predicts that while high-temperature soldering processes, such as wave soldering, might not be affected by the presence of NiSn_3 , the processes that use lower temperatures, such as vapor phase reflow, will be affected. The testing of aged samples showed that the combination of time and temperatures adequate to decompose NiSn_3 , and solder movement can drastically improve solderability.

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REFERENCES

1. P.J. Kay and C.A. Mackay. "The Growth of Intermetallic Compounds on Common Basis Materials Coated With Tin and Tin-Lead Alloys". Trans. Inst. Met. Fin., 54, (1976), 68.
2. P.J. Kay and C.A. Mackay. "Barrier Layers Against Diffusion". Trans. Inst. Met. Fin., 57, (1979), 169.
3. A. C. Harman. "Rapid Tin-Nickel Intermetallic Growth: Some Effects on Solderability". Proceedings, InterNepcon U.K., Brighton 1978, p. 42.
4. U. Lindborg, B. Asthner, L. Lind and L. Revay. "Intermetallic Growth and Contact Resistance of Tin Contacts After Aging". Proc. 21st Ann. Holm Seminar on Electrical Contacts, Chicago, 1975, p. 25.
5. M. Hansen & K. Anderko. "Constitution of Binary Alloys", 1958. McGraw-Hill, New York.
6. A.C. Harman and C.A. Park. "Rapid Intermetallic Growth in Tin and Tin-Lead Coatings on Nickel Underlayers". Report #: IR/R446/1986/938, Standard Telecommunications Laboratories, Ltd., Harlow, Essex, 1980.
7. T. Davis. AMP Incorporated, Unpublished Research, 1985.
8. D. Kahn. AMP Incorporated, Memorandum to J. Haimovich, May 28, 1986.
9. J.A. Augis and J.E. Bennett. "Kinetics of Transformation of Metastable Tin-Nickel Deposits. 1. Determination of the Avrami Equation Parameters by DSC or DTA." J. Electrochem. Soc., 125, (1978), 330.
10. R.F. Speyer and S.H. Risbud. "Methods of Determination of the Activation Energy of Glass Crystallization From Thermal Analysis." Physics and Chemistry of Glasses, 24, (1983), 26.

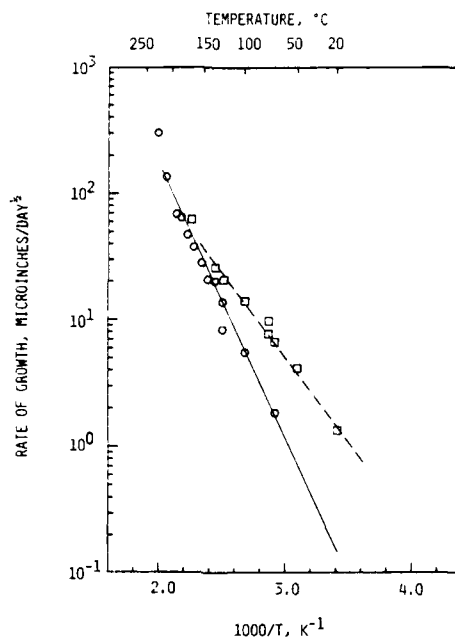


FIGURE 1. Intermetallic Growth in Matte Sn on Cu and Ni Substrates. Solid line - Ni; dotted line - Cu.



FIGURE 2. Intermetallic Growth in Matte Sn, Ni Underplate. Aged 1.5 years at 50°C.

TABLE 1. SOLDERABILITY TEST RESULTS (% PASSED)

Sample	Aging Time			
	6 Months	12 Months	18 Months	24 Months
<u>A. AGED AT 50°C</u>				
100 Sn/Ni	100	57	43	0
90 Sn-10Pb/Ni	100	86	86	86
60 Sn-40Pb/Ni	100	100	100	100
100 Sn/Cu	86	86	29	0
90 Sn-10Pb/Cu	38	38	0	0
60 Sn-40Pb/Cu	29	29	14	14
<u>B. AGED AT 24°C</u>				
100 Sn/Ni	100	100	75	0
90 Sn-10Pb/Ni	100	100	86	86
60 Sn-40Pb/Ni	100	100	100	100
100 Sn/Cu	100	86	43	14
90 Sn-10Pb/Cu	14	14	14	0
60 Sn-40Pb/Cu	75	50	25	25

TABLE 2. MENISCOGRAPH TEST RESULTS (From Reference 7)

AGING TIME 24 MONTHS

SAMPLE	AGED AT 24°C		AGED AT 50°C	
	FINAL VALUE OF WETTING FORCE, GRAMS	TIME TO CROSS ZERO, SECONDS	FINAL VALUE OF WETTING FORCE, GRAMS	TIME TO CROSS ZERO, SECONDS
100 Sn/Cu	- .23 ± .02	--	- .29 ± .03	--
100 Sn/Ni	- .14 ± .03	--	- .20 ± .03	--
90 Sn -10 Pb/Cu	.05 ± .01	2.9 ± .4	.05 ± .01	3.1 ± .3
90 Sn -10 Pb/Ni	.05 ± .01	2.7 ± .2	.02 ± .01	3.9 ± .6
60 Sn -40 Pb/Cu	.18 ± .05	2.1 ± .2	.16 ± .06	2.2 ± .3
60 Sn -40 Pb/Ni	.14 ± .03	2.2 ± .2	.13 ± .03	2.3 ± .1

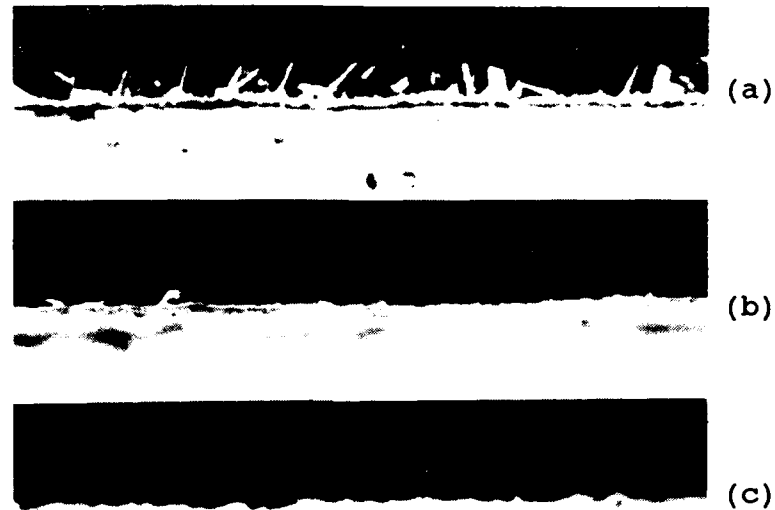


FIGURE 3. Decrease of Ni-Sn IMC growth with Increasing Lead Content: (a) 100% Sn; (b) 90% Sn-10% Pb; (c) 60% Sn-40% Pb. Aged 1.5 years at 50°C.

1000X

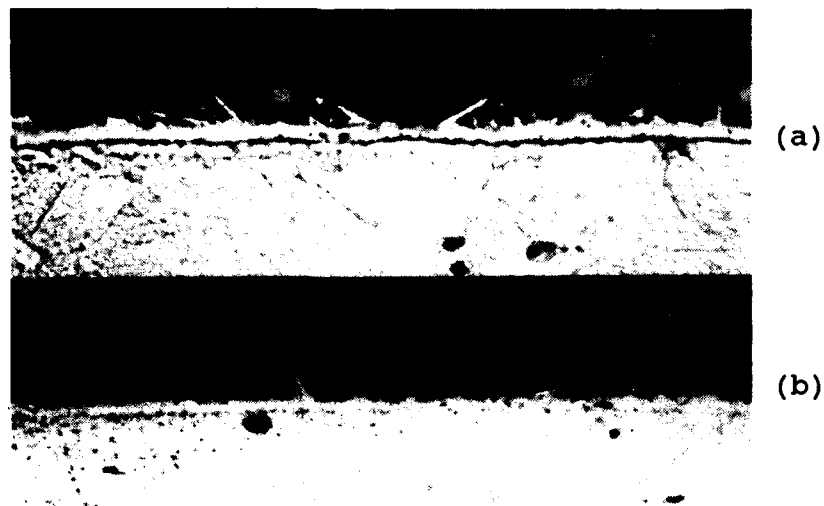


FIGURE 4. Decrease of Ni-Sn IMC growth with High-Temperature Preannealing: (a) No Preanneal. (b) Was Preannealed at 155°C for 8 hours. All aged at room temperature for 1.5 years.

1000X



FIGURE 5. Combined Effect of Preannealing and Lead Content; 90% Sn-10%Pb, (a) No Preanneal. (b) was Preannealed at 155°C for 8 hours. All aged at room temperature for 1.5 Years.

1000X

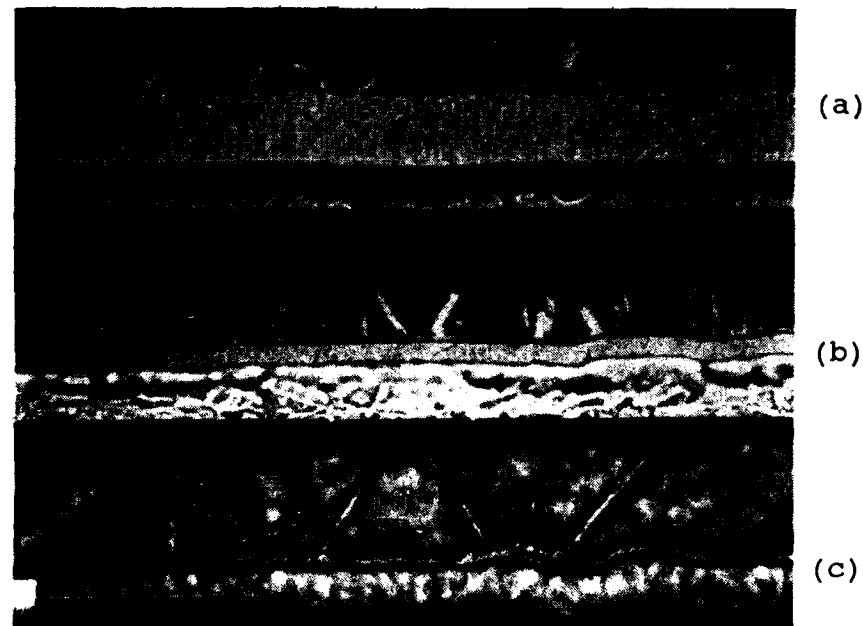


FIGURE 6. Matte Sn on Ni; tin etched. Aged 16 days at: (a) 75°C, (b) 100°C, (c) 125°C.

1000X



FIGURE 7. Matte Sn on Ni; tin etched. Aged 8 days at: (a) 135°C, (b) 145°C, (c) 155°C.
1000X

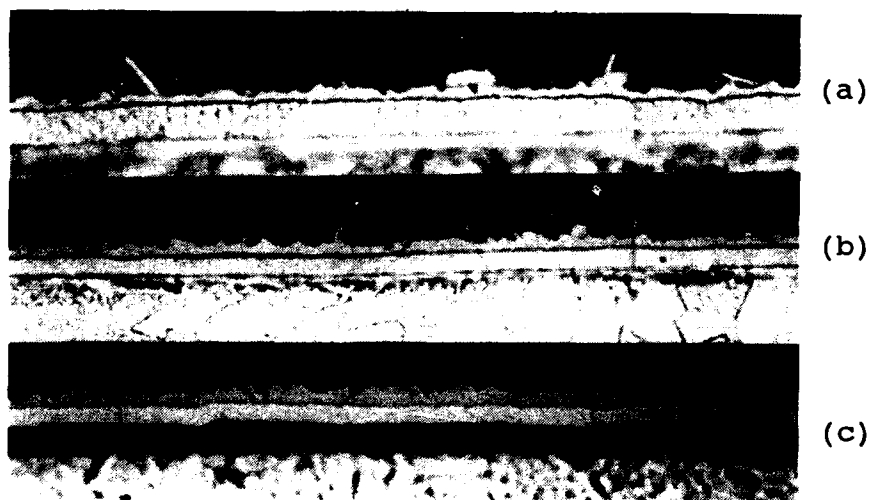
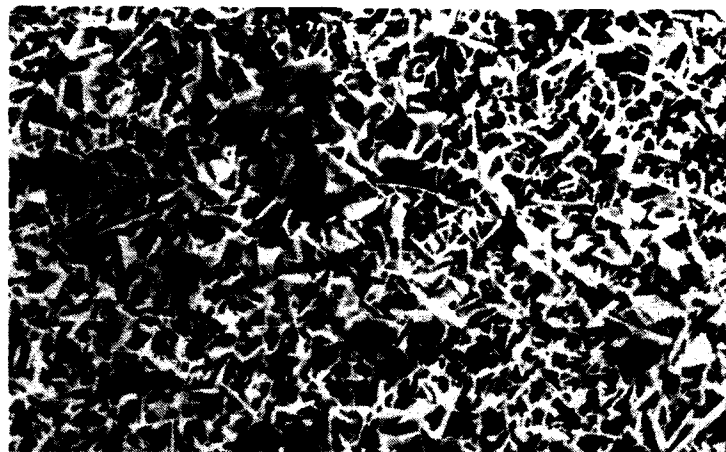


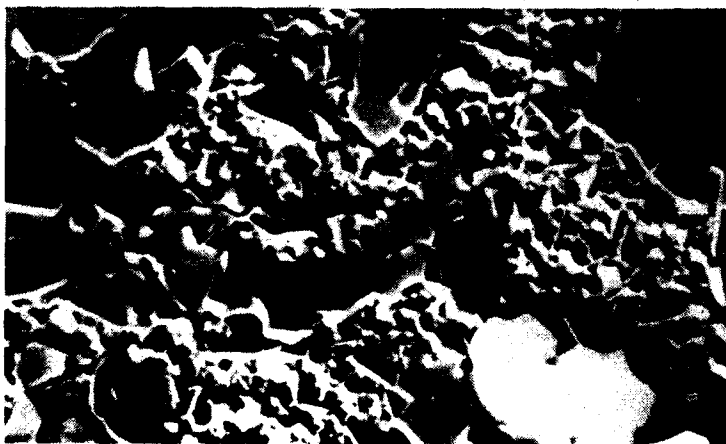
FIGURE 8. Matte Sn on Ni; tin etched. Aged 2 days at: (a) 165°C, (b) 175°C, (c) 185°C.
1000X



(a)



(b)



(c)

FIGURE 9. Matte Sn on Ni; tin removed. Aged 16 days at (a) 75°C, (b) 100°C, (c) 125°C.

1000X

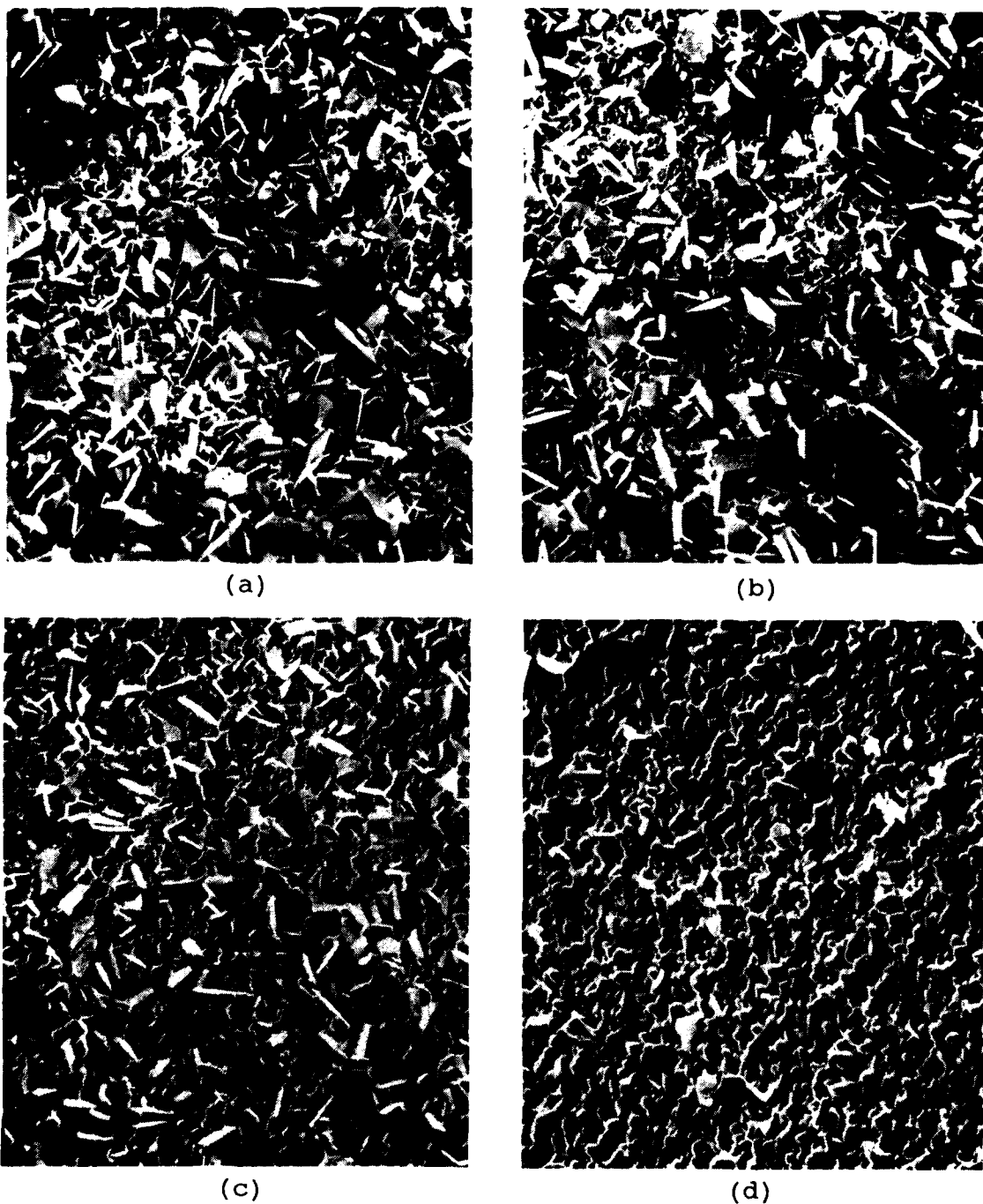
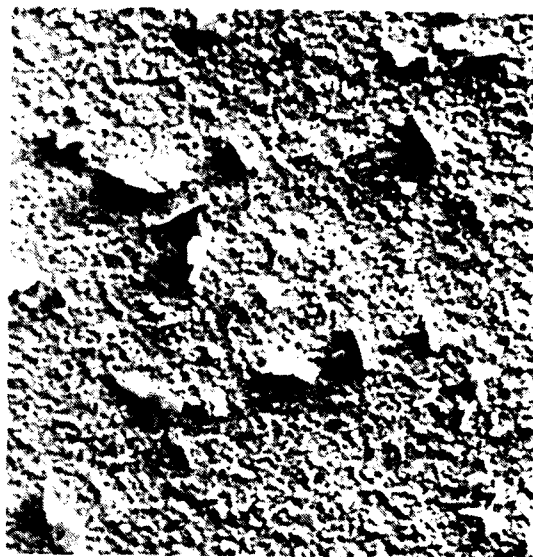


FIGURE 10. Matte Sn on Ni; tin removed. Aged 2 days at (a) 125°C, (b) 145°C, (c) 165°C, (d) 185°C.

1000X



(a)

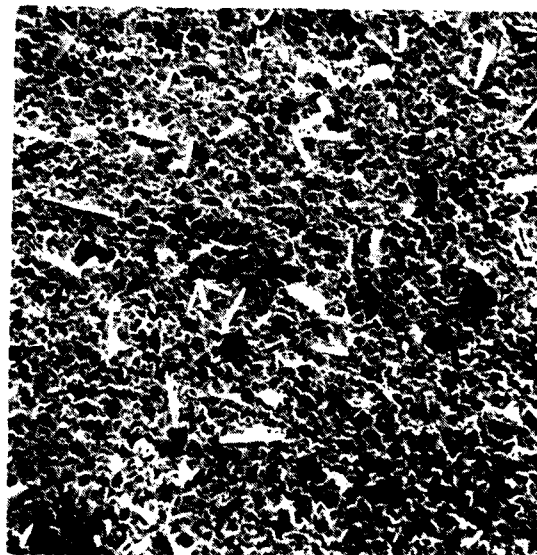


(b)

FIGURE 11. Matte 75% Sn - 25% Pb on Ni - solder removed. Aged 16 days at: (a) 75°C, (b) 100°C.
1000X



(a)



(b)

FIGURE 12. Matte 75 Sn - 25 Pb on Ni, solder removed. Aged 8 days at: (a) 125°C, (b) 155°C.
1000X

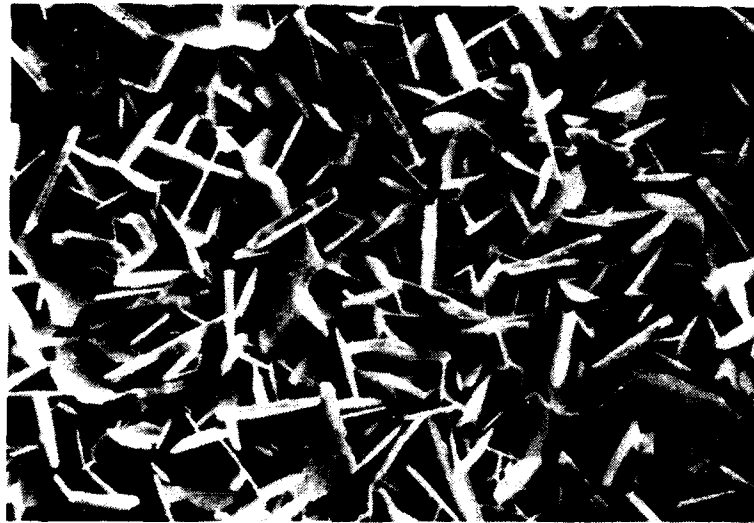


FIGURE 13. Intermetallic growth in matte Sn over sulfamate Ni, aged 2 months at 75°C, and consequently 1 month at 125°C. Free tin removed.
1000X

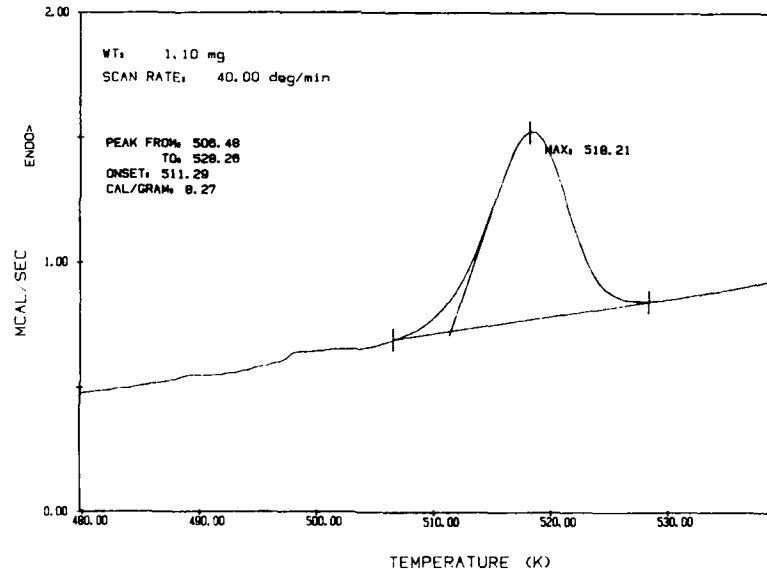


FIGURE 14. A typical DSC scan for NiSn_3 ; "matte Sn" sample. Scan rate 40 deg/min. Onset at 511.3 (513.3)K. The corrected temperature for this and the following figures through Figure 18 is given in parentheses.

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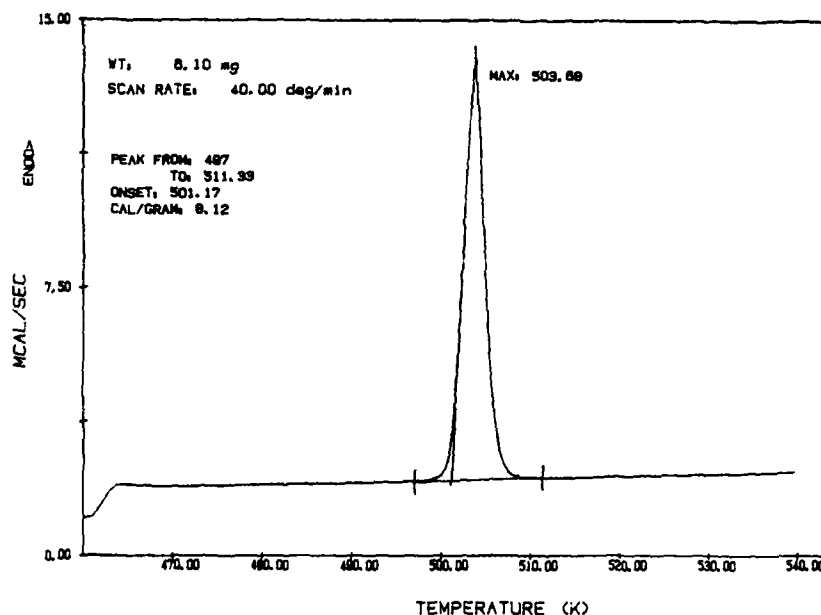


FIGURE 15. A typical DSC scan for decomposed NiSn_3 ; "matte Sn" sample. Scan rate 40 deg/min. Onset at 501.2 (503.2)K.

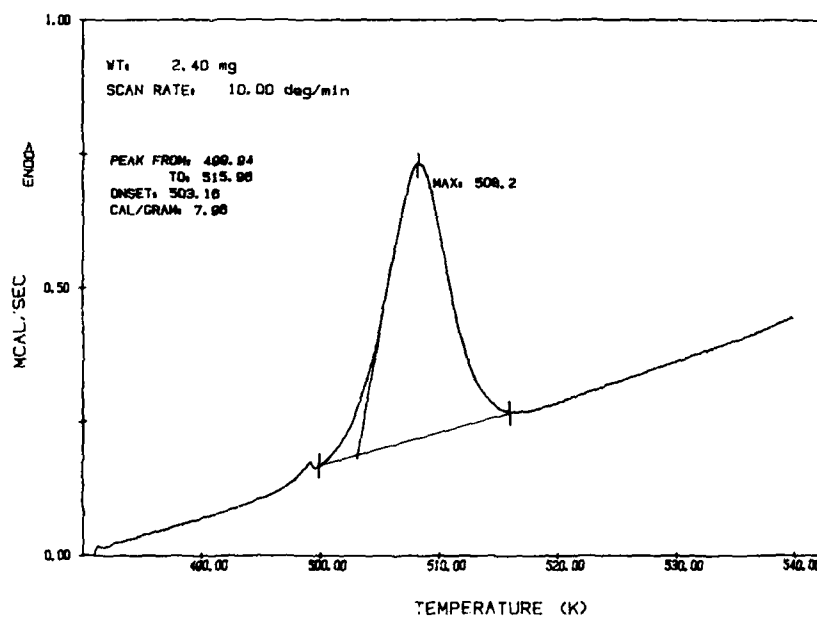


FIGURE 16. DSC scan for "bright Sn" sample; lower scan rate, 10 deg/min. Onset at 503.2 (508.0)K.

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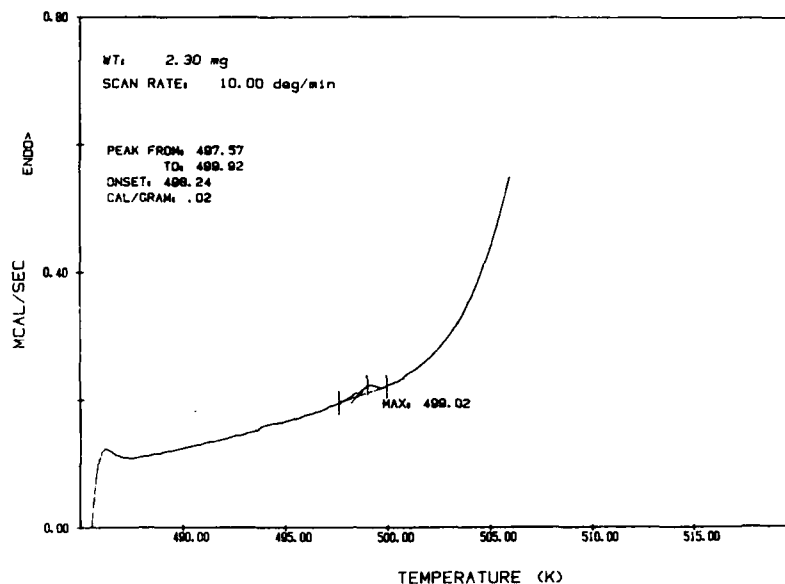


FIGURE 17. First scan for NiSn_3 sample. Scan was stopped at 506 (510.8)K, and sample cooled. Tin peak at 499 (503.8)K is very small, since only a small fraction of NiSn_3 decomposed below 498 (502.8)K.

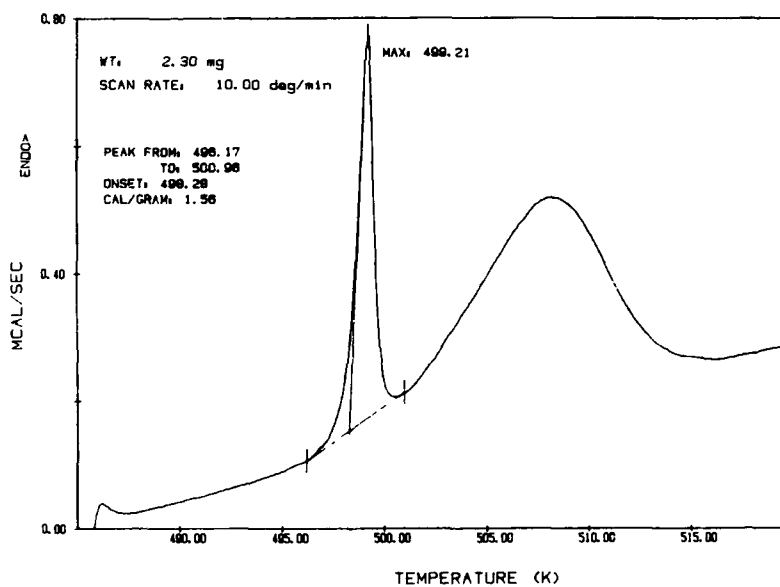


FIGURE 18. Second scan for the sample in Figure 17. Tin peak is much larger because NiSn_3 partially decomposed when heated to 506 (510.8)K.

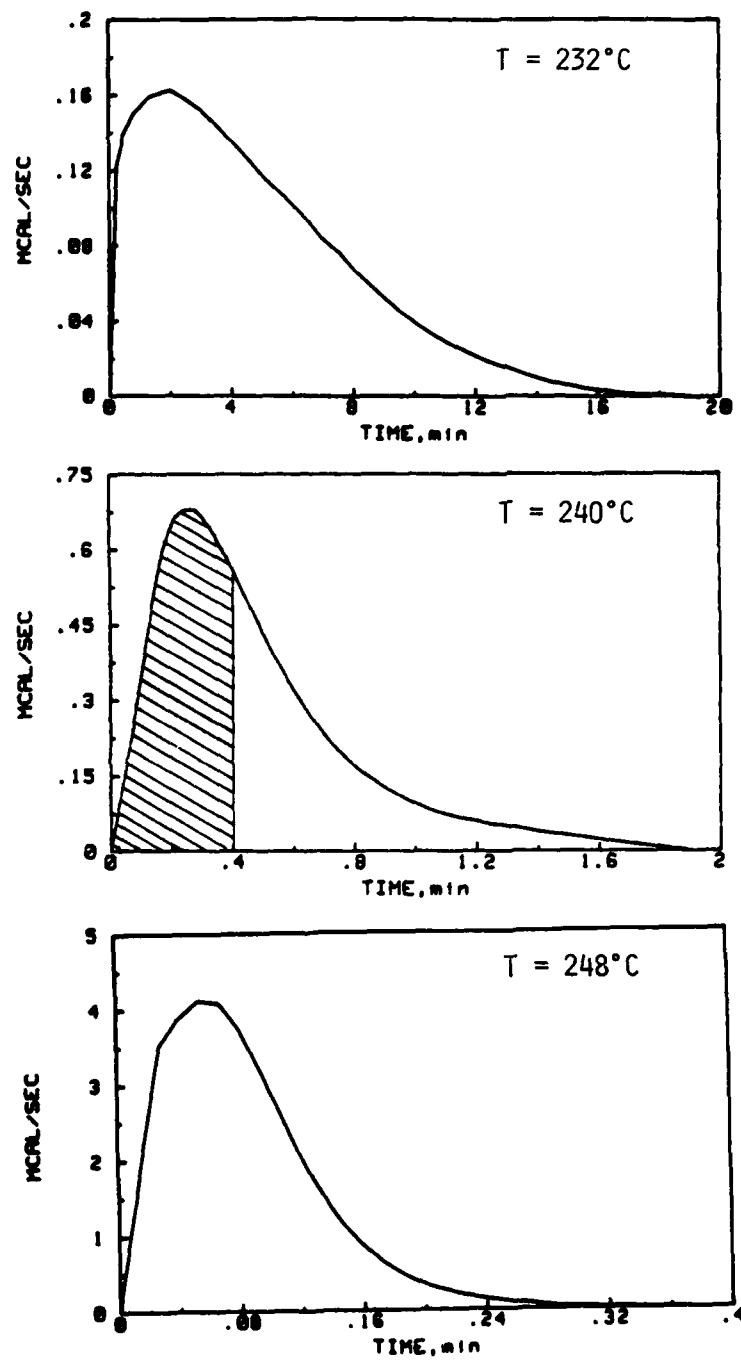


FIGURE 19. Isothermal DSC curves. The sample is NiSn_3 that grew in matte Sn over sulfamate Ni during $75^{\circ}\text{C}/2$ mo. - $125^{\circ}\text{C}/1$ mo. two-step aging.

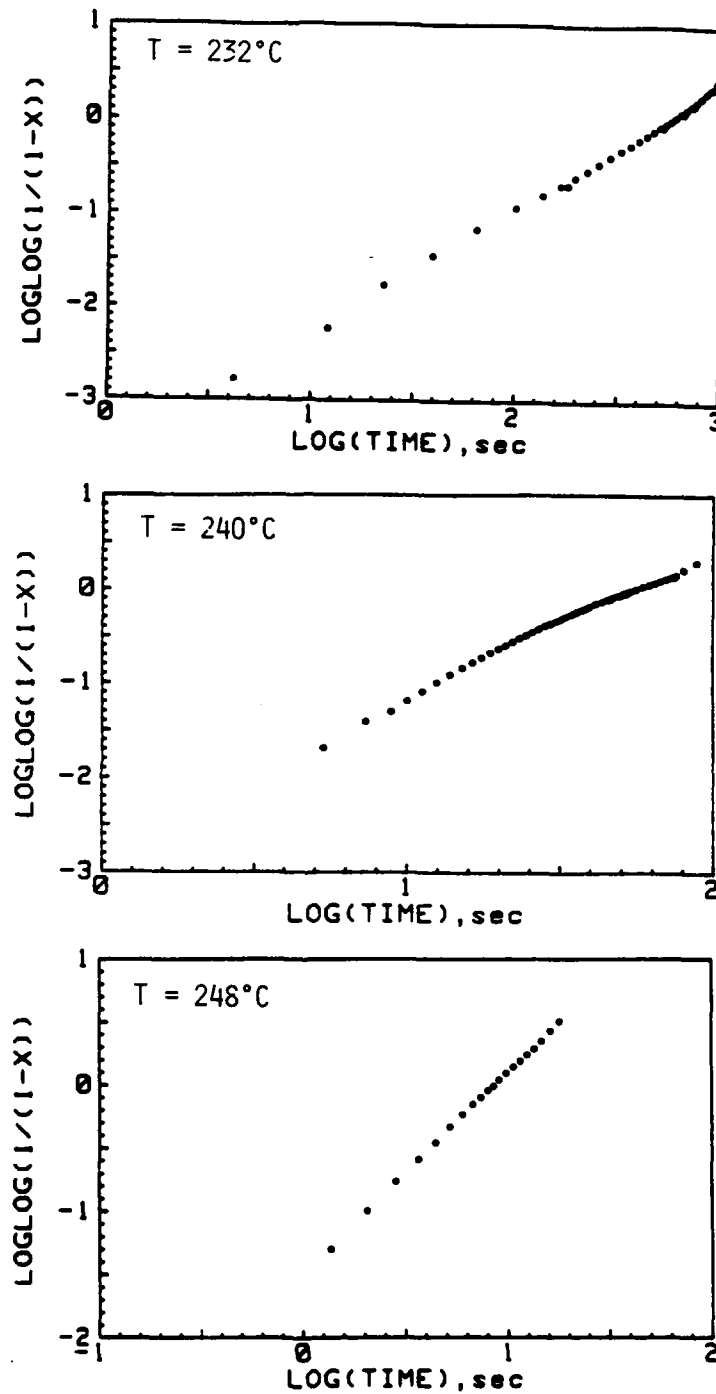


FIGURE 20. Avrami plots obtained using data from Figure 19.

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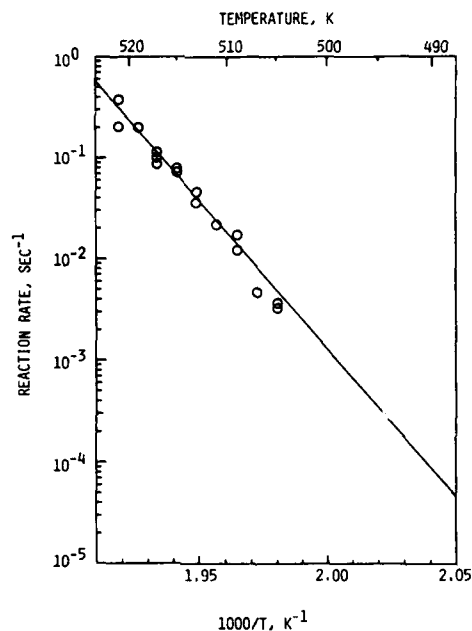


FIGURE 21. Arrhenius plot for rate constant k . Circles are data points; line is fit through data points.

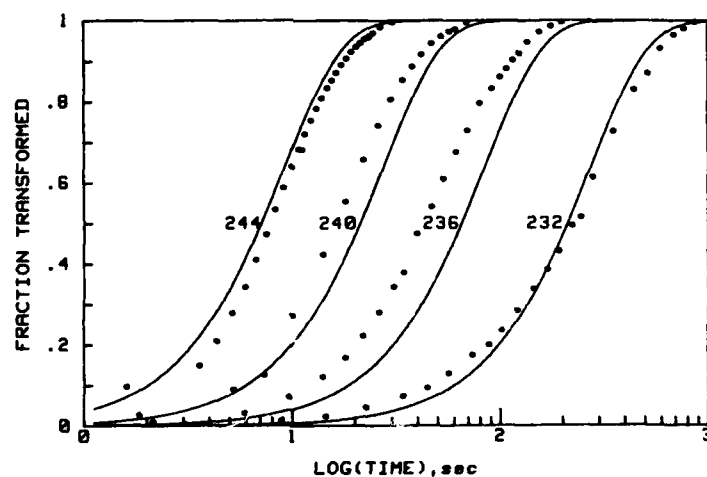


FIGURE 22a. Sigmoidal curves for decomposition of NiSn₃. The circles are the actual data, and the curves are Avrami fits using $n = 1.5$ and k obtained from Figure 21. The temperatures indicated are in degrees C. Sample aged 75°C/2 mo. - 125°C/2 mo.

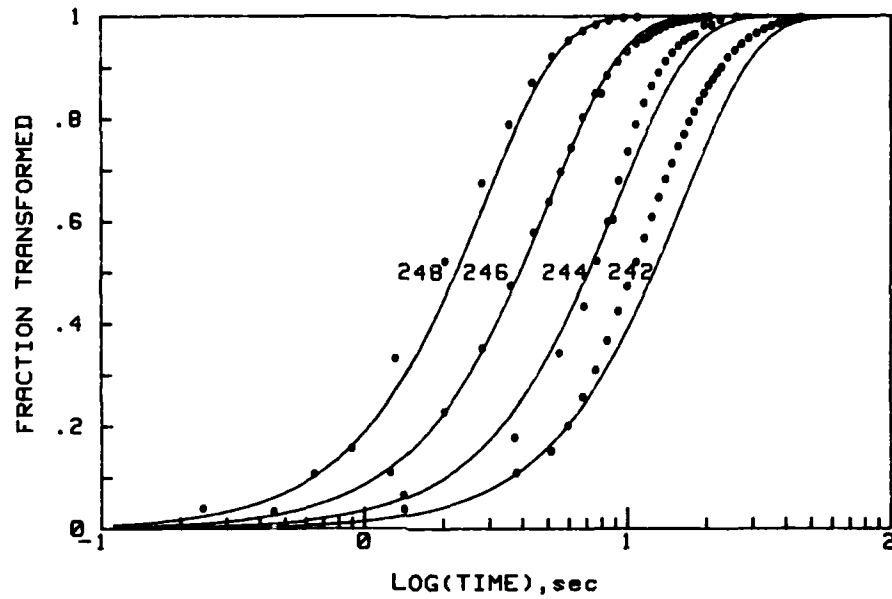


FIGURE 22b. Same as Figure 22a, but for sample aged 75°C/2 mo. - 125°C/2.5 mo.

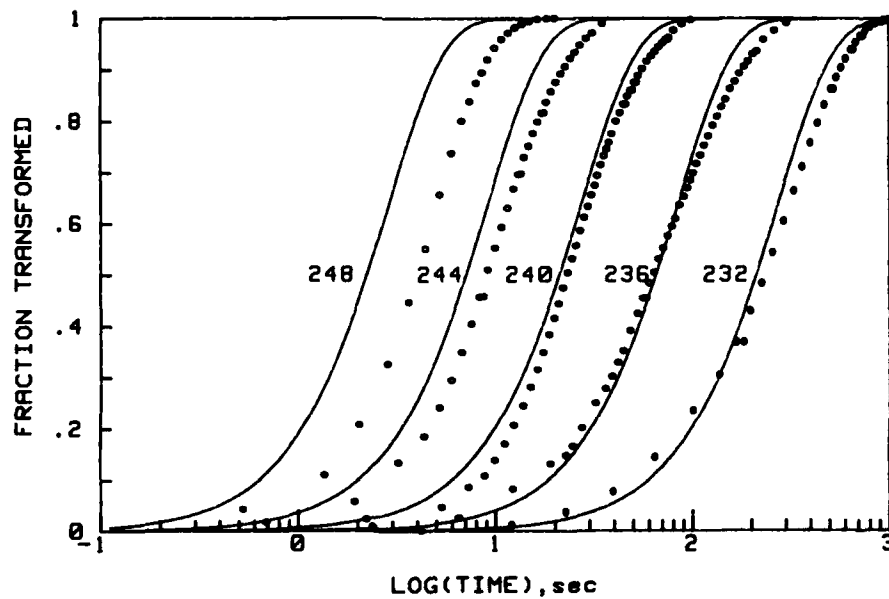


FIGURE 22c. Same Figure as 22a, but for sample aged 75°C/2 mo. - 125°C/1 mo.

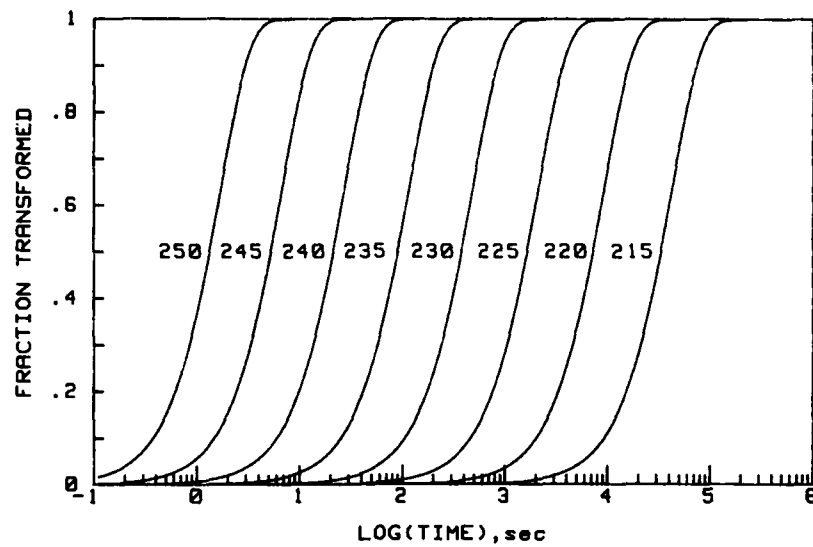


FIGURE 23. Sigmoidal curves for decomposition of NiSn_3 . Obtained in same manner as Figure 22a.

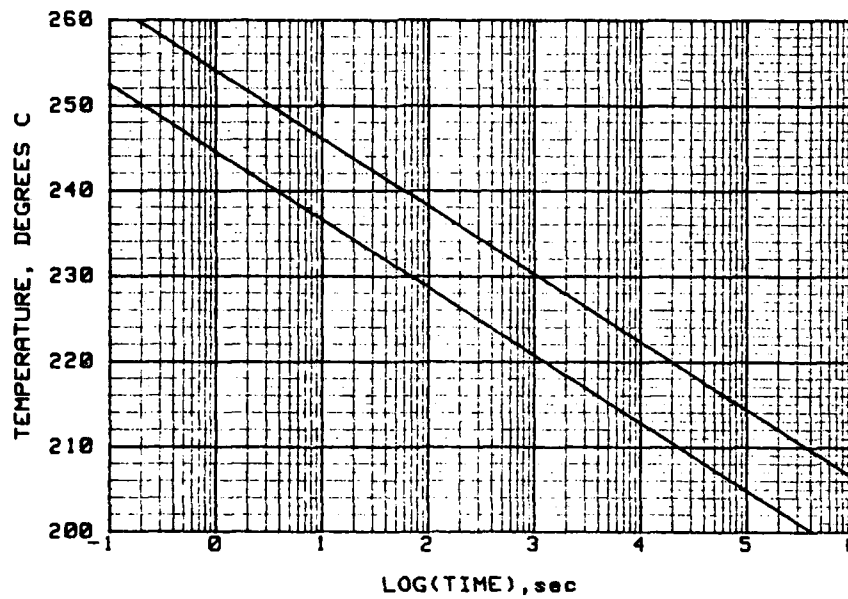


FIGURE 24. T-T-T Diagram for NiSn_3 IMC. The line on the left represents the beginning of transformation (5% transformed); the line on the right - the completion of transformation (95% transformed).

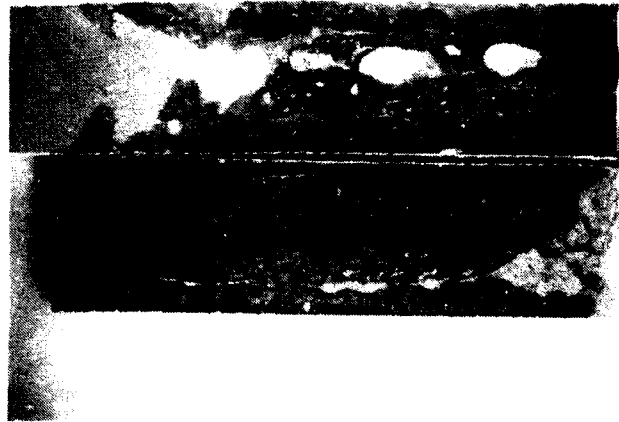


FIGURE 25. Solderability test samples tested at 215°C (top) and 260°C (bottom).

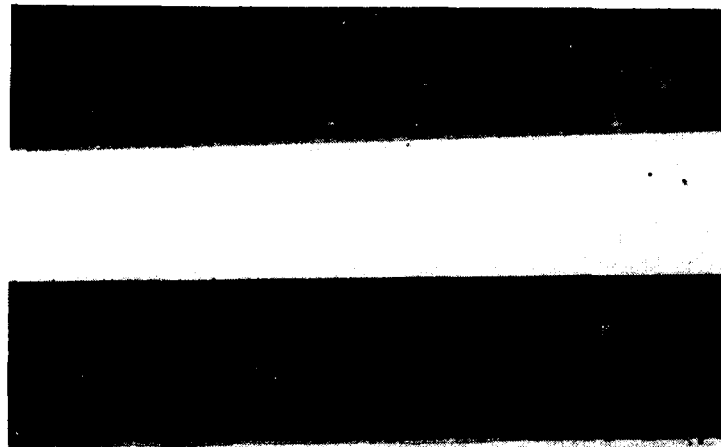


FIGURE 26. Cross-sections of the solderability test samples tested at 215°C (top) and 260°C (bottom).

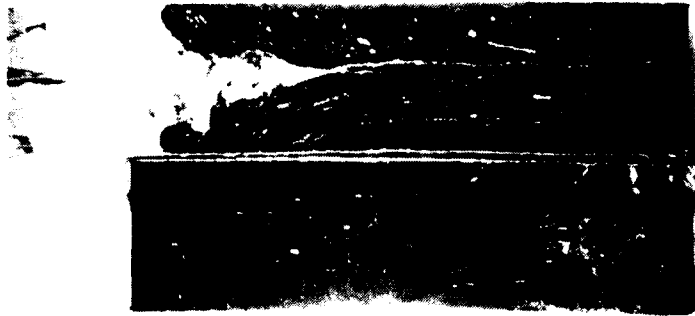


FIGURE 27. Solderability test samples tested at 245°C: top, stationary; bottom, moving.

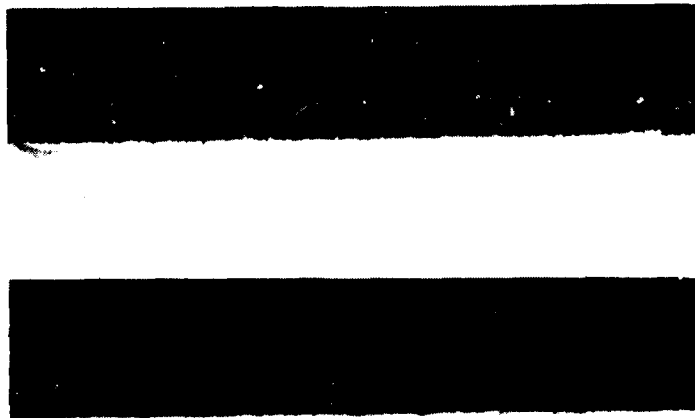


FIGURE 28. Cross-sections of solderability test samples tested at 245°C: top, stationary; bottom, moving.

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A STUDY OF I.C. PACKAGE SOLDERABILITY

BY

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ABSTRACT

This paper will address several important areas of integrated circuits (I.C.) package solderability such as test methods, lead finishes, correlation studies, process control requirements and statistical sampling sizes.

A detailed analysis of both MIL-STD-833 Method 2003 and Method 2022 will be presented that will show while the meniscograph test, Method 2022, provides solderability test results that show excellent means for measuring lot process capabilities. It should be combined with method 2003 to fully evaluate solderability.

An explanation of present I.C. package lead finishes such as tin plate, single solder dip and double solder dip will be shown as well as solderability test results for these lead finishes using both Method 2003 and 2022.

The paper will conclude with a brief demonstration of how present MIL-STD-883 dictated sample sizes, while improved, are still not adequate to control I.C. solderability, and as a result of this the I.C. vendor must use Statistical Quality Control to monitor I.C. solderability.

Introduction

Method 2003-Solderability and 2022-Meniscograph (wetting balance) solderability of Mil-Std-883C have been in effect for several years. Both methods have desirable and undesirable characteristics which will be discussed. The need for statistical Quality

Control above Mil-Std-883 sample sizes will be covered. A wetting balance comparison of pre and post burn-in solder dip is included. Data on solderability with R flux of units processed in different manners is presented. A discussion on the maximum force for given units and pin counts is shown.

Comparison of Method 2003-Solderability and 2022
Meniscograph (Wetting Balance) solderability

The key points of both specifications are shown in Table 1. Recent revisions in the specifications have made them virtually the same. However, several items deserve comment.

Both methods show 8 hours of steam age. The methods allow the vendor to test at 4 hours and the customer to test at 8 hours. This is not expected to be a problem as most parts that pass 4 hours will also pass 8 hours. However most vendors are testing for 8 hours as a safety measure.

While not covered in the specifications the flux applications should be mechanical. Reference 1 shows that improper flux application (too much or too little) can result in apparent dewet rejects on units that will pass the specification.

The solder pot is specified to be either wave or static for Method 2003 and static for Method 2002.

The action of the wave will improve the solderability over that of a static pot. To be consistent the static pot should be required for both specifications.

The mechanical dip method has been in the Method 2003 for several years and still has not been fully implemented by the industry. With the specification being tightened in the last few years, it is now impossible for a typical inspector to manually do the test accurately.

The inspection range of Method 2003 is 10-20X. The high side of this inspection should be increased to 50X. Stains and other minor surface imperfections can be mis-interpreted at lower magnifications.

Reject criteria is different on both methods, Method 2003 requires visual criteria while Method 2022 measures various times on the force curve. It will be shown later in the paper that both of these reject criteria have pro's and con's.

The LTPD is now at 10 based on the number of leads rather than the number of units. While an LTPD of 10 says that lots that are 10% defective will be rejected 90% of the time, the probability of acceptance at very high quality levels is also important. One of the sample sizes for an LTPD of 10 is 38 accept on zero or one reject. Table 2. shows the probability of acceptance for this sample size for various lead % defectives.

Table 2.

% Defective	Probability of Acceptance
-----	-----
.01	99.9
.1	99.9
.5	98.4
1.0	94.5
10.	10.0

With customer manufacturing goals in the range of 1 per 1000 to 1 per 10,000 defects, the sampling plan is not sensitive to the required % defective.

This is an ideal case for statistical quality control. Data shows that hot solder dip parts are capable of Parts Per Million of less than 100. The process control charts should be set to trigger based on these PPM's, rather than counting on the sample plan to identify potential problems.

It is also interesting to review the capabilities of both methods.

The experimental data which follows was collected from ceramic flat packs with alloy 42 lead frames. Examples of flat pack devices are shown in Figure 1. This was done because the flat pack has uniform lead dimensions. The wetting balance curves were replotted to improve their clarity.

The first test sample was a 24 pin unit that had been post burn solder dipped with an active flux (CR09). The unit was dipped in R flux and the wetting balance curve shown in Figure 2 was obtained.

One lead of the unit then had all solder removed and a drop of salt water was put on the unit and left for 24 hours. The wetting balance curve shown in Figure 3 and photo shown in Figure 4 were the result of this test. The wetting balance curve is virtually the same as the curve shown in Figure 2 and is excellent. The photo, Figure 4 clearly fails the solderability requirements of Method 2003. The unit was then solder dipped in active flux. The visual defects were eliminated by these actions and the wetting balance curve shown in Figure 5 was obtained.

A solderability test per Method 2022 test was also run with units that were pre and post burn in solder dipped. A sample of 32 14 lead package was selected for this test. The wetting balance curves shown are average values. Figure 6 shows the post burn-in solder dip results. All units passed the requirements of Method 2022. Figure 7 shows the preburn-in solderdip results. Figure 7 fails the requirements of 2022 from a wetting time and a % of maximum force at 1 second.

All leads of all units passed the 95% coverage requirements of Method 2003. This is not surprising since the maximum force at 5 seconds is almost the same on both curves.

Data was taken using the wetting balance to compare time to cross the zero force axis for ceramic dip and flat pack units processed with several different lead finishes and different R flux solids contents, which is shown in Figure 8. Reference 2 shows similar data. These times are based on 5 units for each data point. All the post burn-in solder dip units on all lead counts show constant wetting times which are independent of flux solids content. The other units show increasing times as the solids content is decreased. The solderability of the tin plated part which was plated before burn-in is significantly affected by the decrease in solids content. Reference 3. shows steam aging also impacts tin plated parts more than hot solder dipped parts.

Figure 9 shows the results of data taken on 10 lead through 24 lead flat pack. The units were dipped and redipped using the same flux (Active or R) until the maximum force was obtained. When the active flux was used this occurred on the first dip. No degradation in maximum force was seen through 5 more solder dips. When R flux was used the maximum force was not obtained until 3-5 solder dips were made. The force then remained constant through 10 solder dips. The data confirms the expected result that maximum force is proportional to the periphery of the material dipped into the solder.

The data also shows that the maximum force obtained is almost independent of the flux used once the unit has achieved its maximum solderable state.

One of the possible additions to the meniscograph method would be to include the maximum force as a requirement. While this is a desirable item to have included, it would be difficult to implement, due to differences in lead counts and shapes of leads on such units as ceramic dip.

Summary

With the move of the I.C. vendors away from tin plated parts to hot solder dipped parts the overall solderability of integrated circuits has improved dramatically in the last few years.

The specification requirements of both Method 2003 and 2022 have also been tightened making the test more difficult to perform and generating some false rejects. Improvements in the ability to do the test need to continue.

The sample sizes required remain too small to act as a gate to insure the potential quality level of the process is controlled. It is important that the I.C. vendors use statistical methods to insure process capabilities are maintained.

Both inspection and wetting balance techniques need to be used. The wetting balance is an outstanding tool for evaluating over all process capabilities but is insensitive to discrete problems on single leads.

With the improved solderability, the solids content of the flux is less important and on very solderable parts the flux used is not significant.

The maximum wetting force is an important parameter but will be difficult to specify as the number and shape of the leads cause it to vary dramatically.

The authors are indebted to Elisa Hernandez, John Bryant and Peter Huang for their help in data collection.

References

1. Lessons Learned in Testing Solderability of Integrated Circuits Using Method 2003 of Mil-Std-883C by Buford G. Slay. Presented at 11th Annual Electronics Manufacturing Seminar Proceedings, February 18-20, 1987.
2. The Use of Wetting Balance Data to predict Soldering Materials Performance and Soldering Process Parameters by John A. Devore. Presented at 11th Annual Electronics Manufacturing Seminar Proceedings, February 19-20, 1987.
3. Component Lead Solderability vs. Artificial Steam Aging (Status Report II) by Roger Wilde. Presented at 11th Annual Electronics Manufacturing Seminar Proceedings, February 18-20, 1987.

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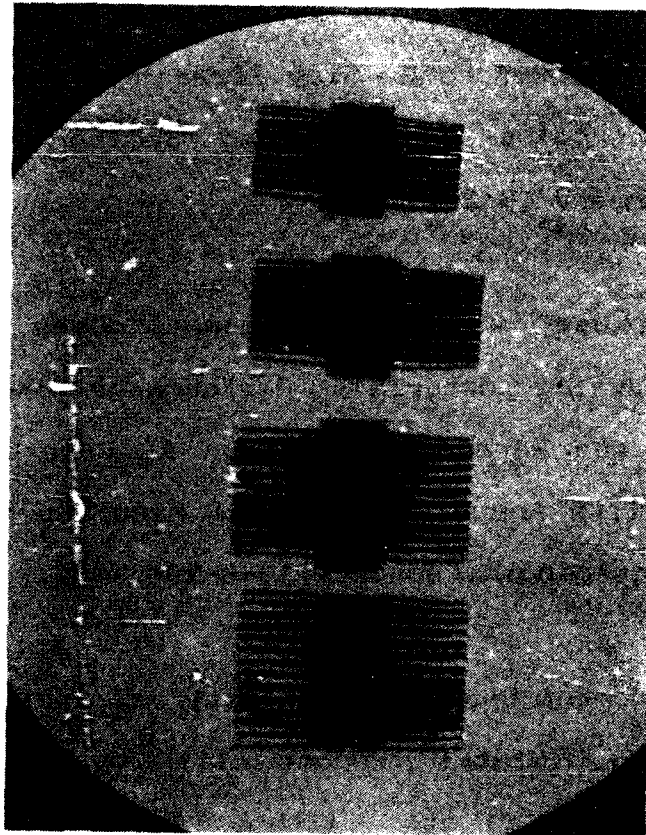


FIGURE 1.

FIGURE 2.

INITIAL DIP

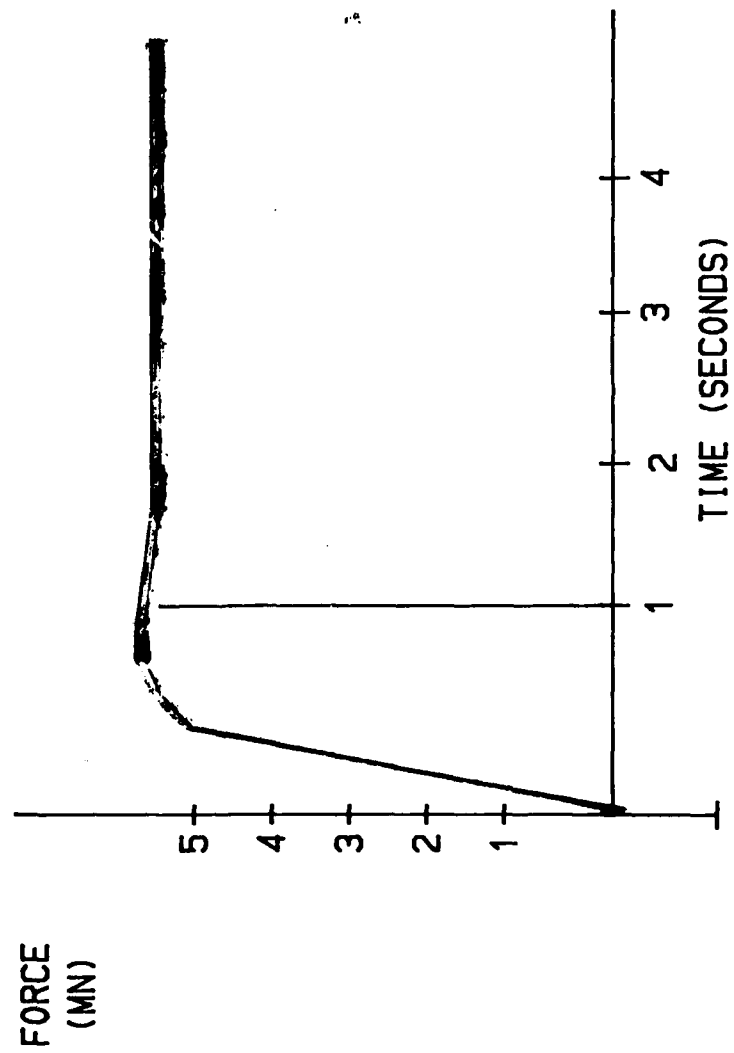
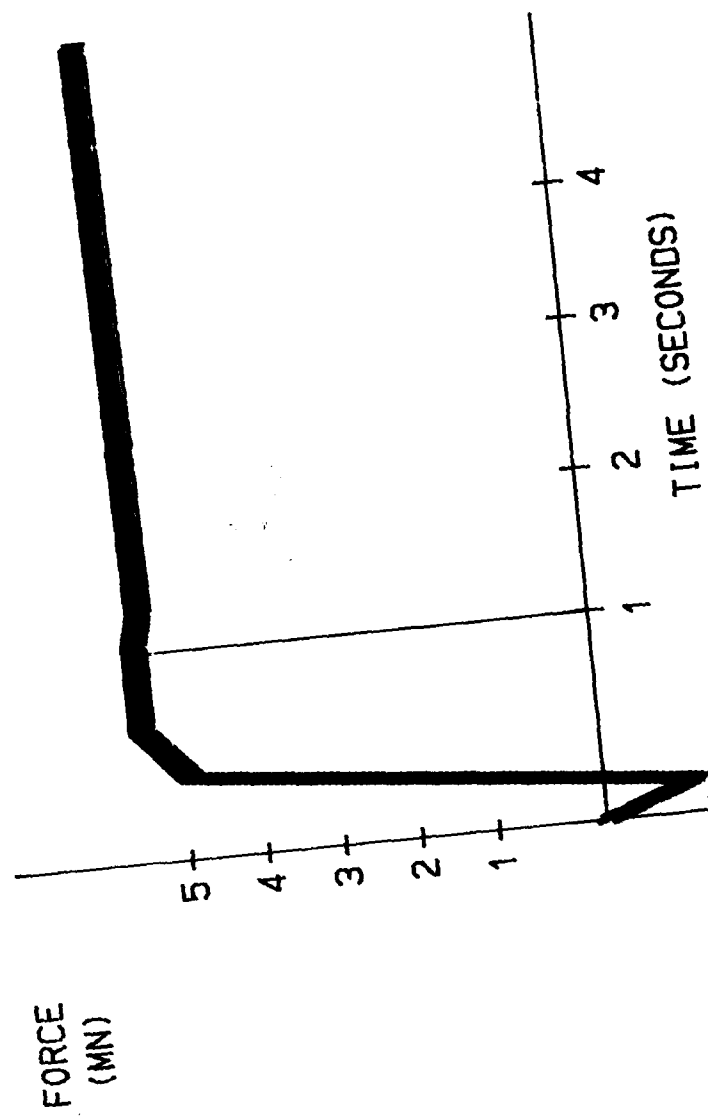


FIGURE 3.
2ND DIP AFTER SALT ATMOSPHERE



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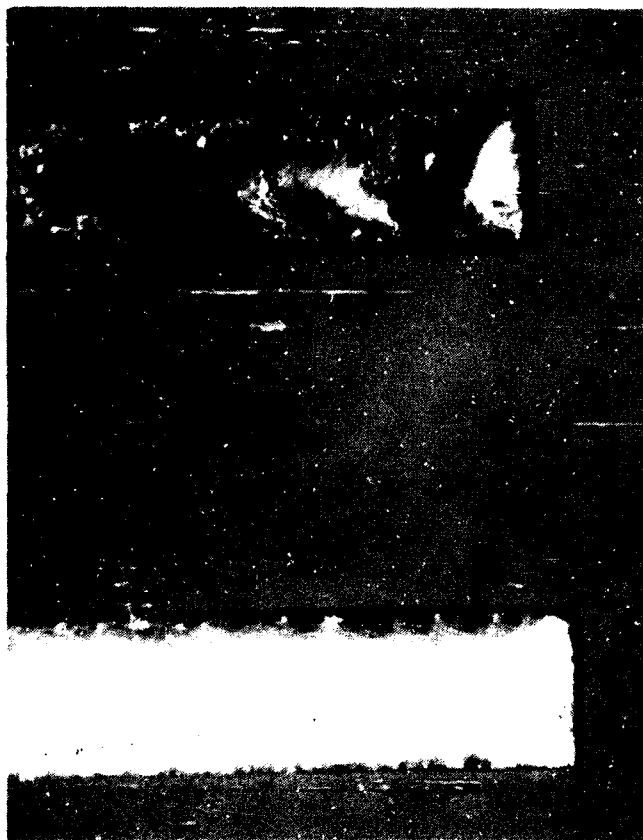


FIGURE 4.

FIGURE 5.

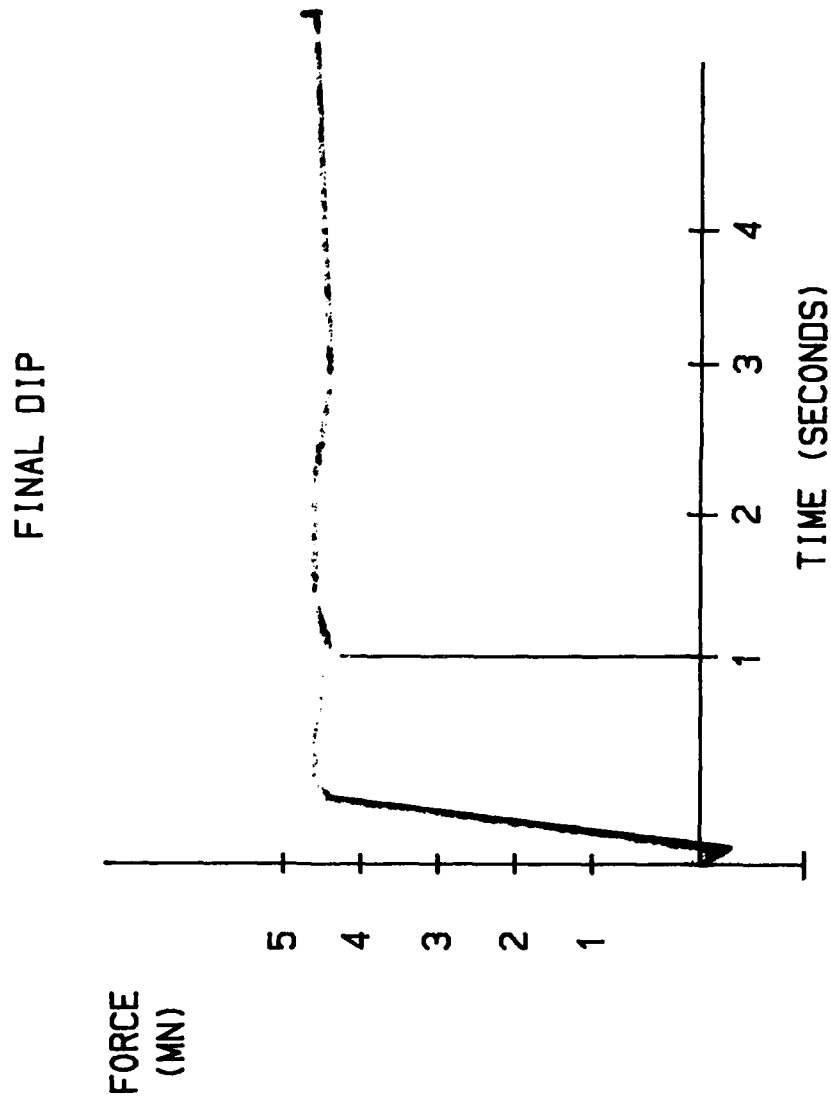
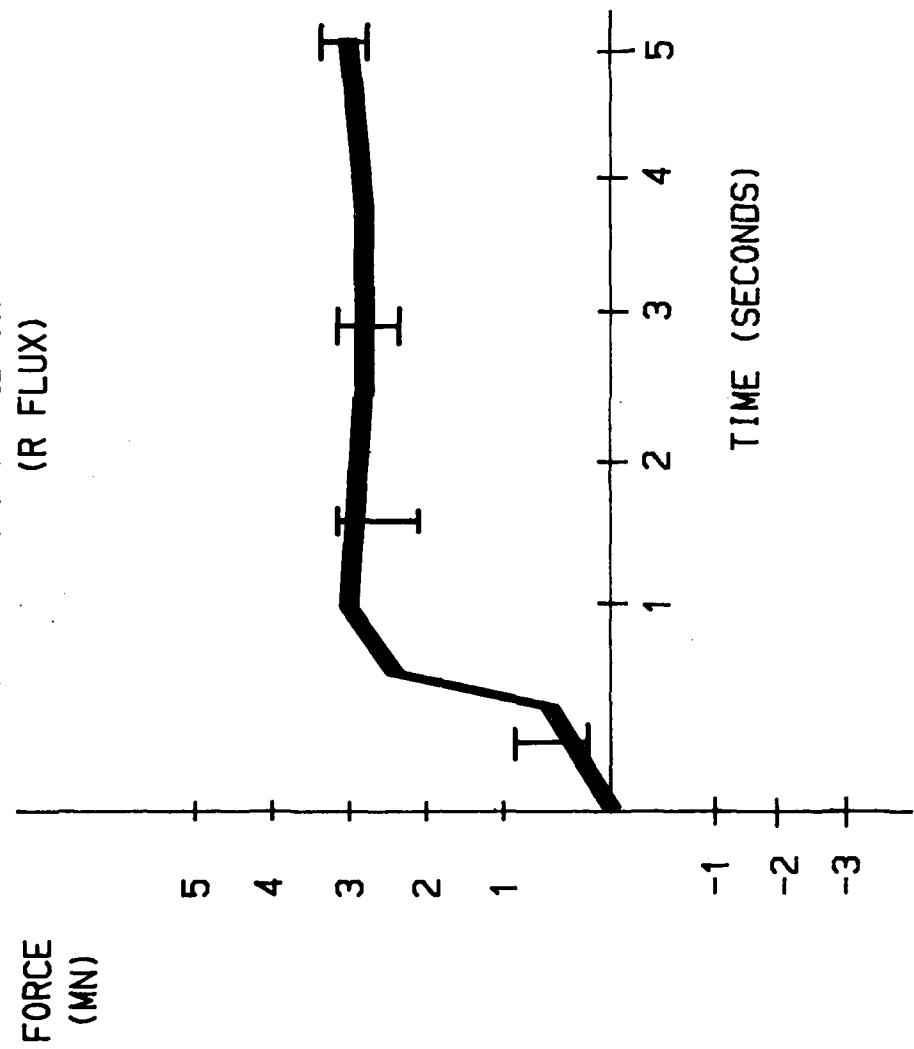


FIGURE 6.
POST BURN IN SOLDER DIP
(AVG CURVE BASED ON 32 UNITS)
(R FLUX)



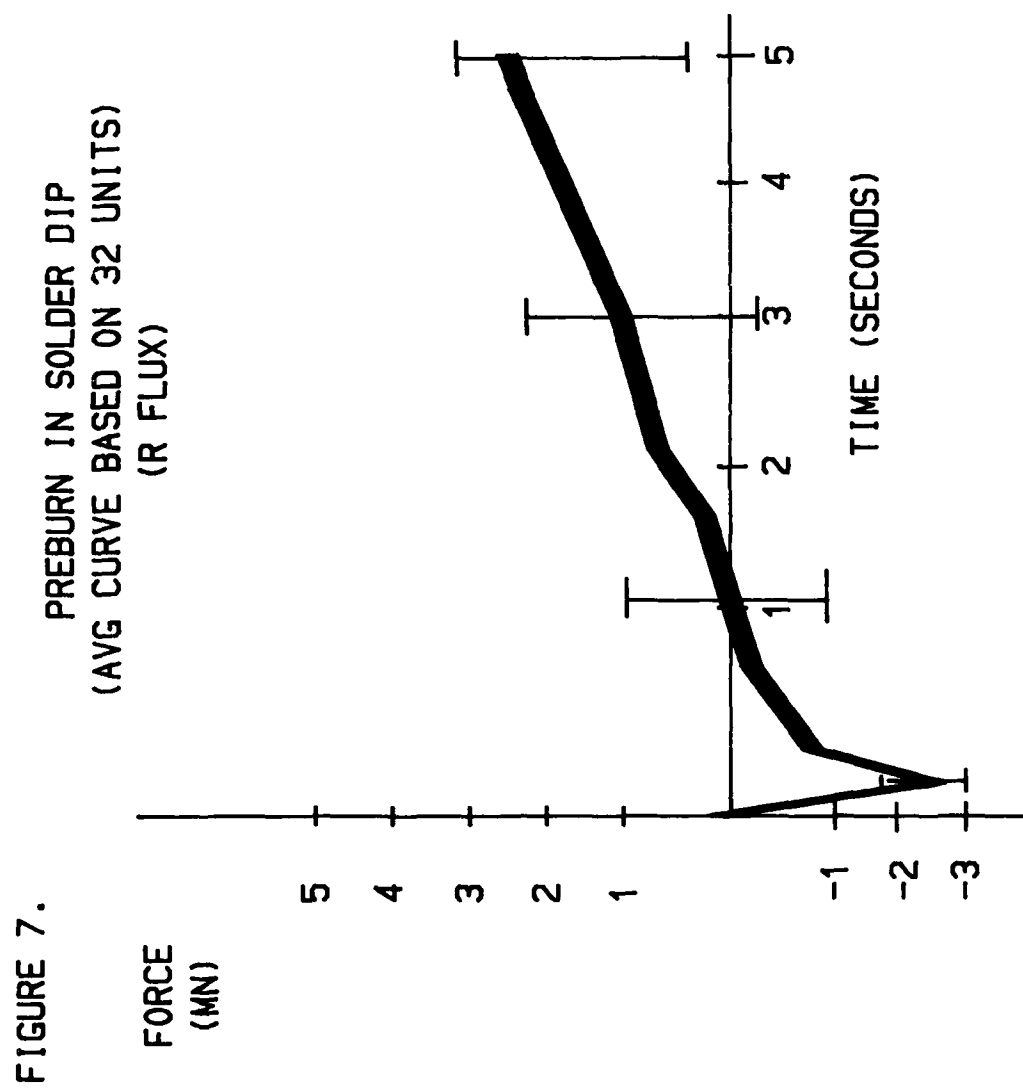


FIGURE 8.
 COMPARISON OF PREBRUN vs POST BURN SOLDER DIP
 AS A FUNCTION OF FLUX SOLIDS CONTENT

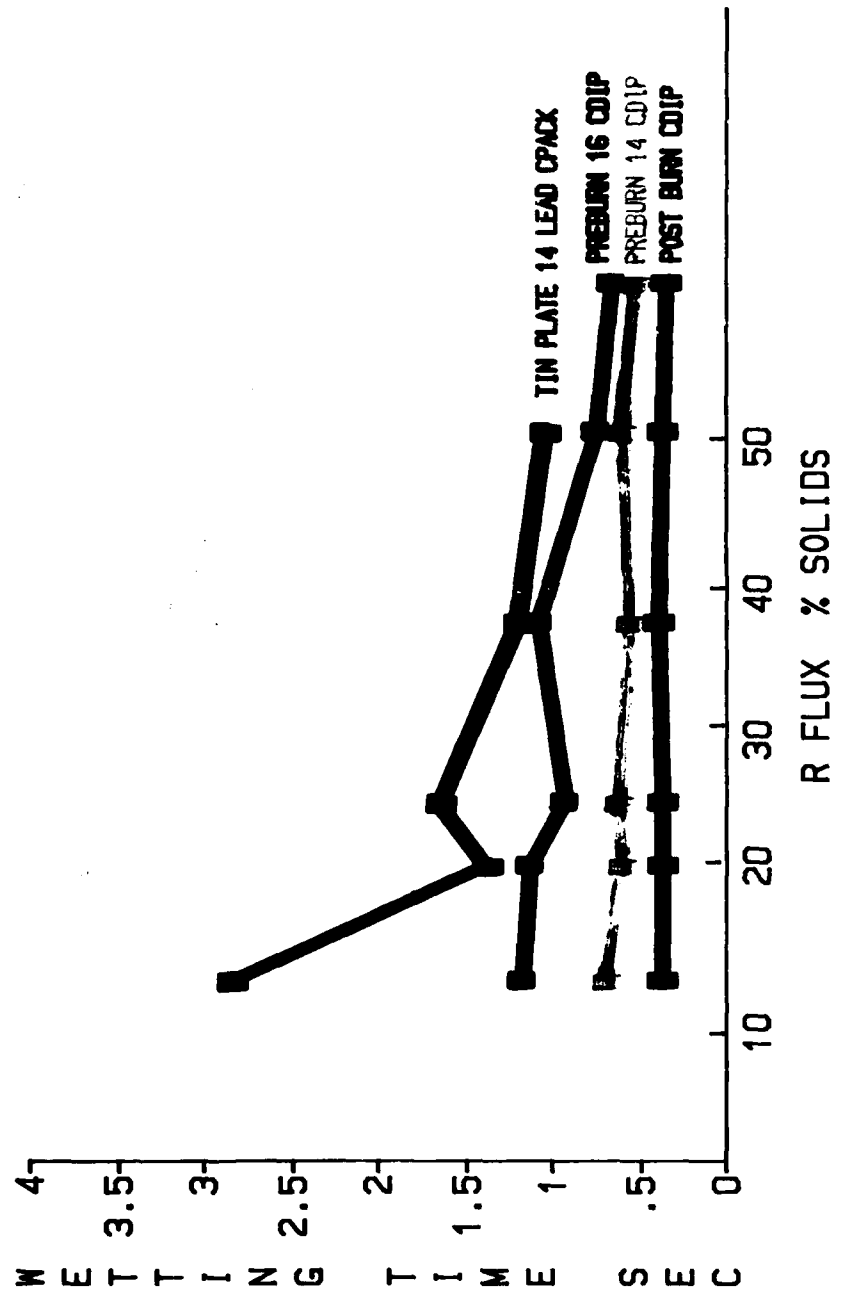


FIGURE 9.
 COMPARISON OF MAXFORCE vs LEAD COUNT

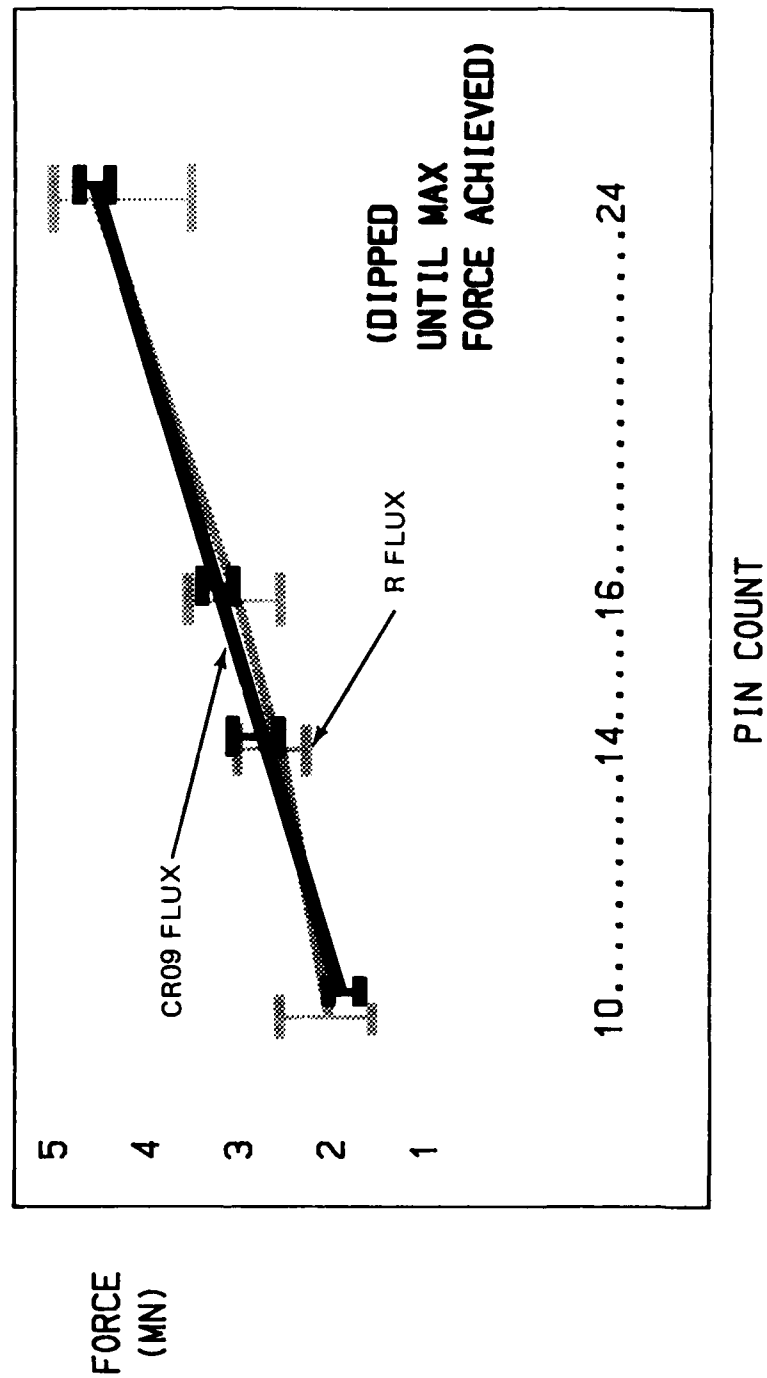


TABLE 1.
COMPARISON OF METHOD 2003-SOLDERABILITY
AND METHOD 2022-MENISCOGRAPH SOLDERABILITY

SPECIFICATION	2003	2022
	4-8 HOURS STEAM R	4-8 HOURS STEAM R
AGING		
FLUX		
FLUX TIME	5-10 SECS	5-10 SECS
POT	STATIC OR WAVE 2 LBS SOLDER	STATIC 750 GRAMS
DIP METHOD	MECHANICAL	MECHANICAL
SOLDER TEMP	245 DEG C +/- 5 DEG C	245 +/- 5 DEG C
RATE	1 +/- 1/4 MIN.	1 +/- 1/4 MIN.
DWELL	5 SEC +/- 1/2 SEC	5 SEC +/- 1/2 SEC
REJECT CRITERIA	95% COVERAGE (PIN HOLES, VOIDS, NONWETTING DEFECTS)	.59 SECS TO RETURN TO ZERO .667 OF MAX VALUE IN 1 SEC (NO MAX VALUE SPECIFIED)
INSPECT	10-20X	NOT REQUIRED
SAMPLE SIZE	LTPD 10, 30-1	LTPD 10, 30-1

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A CRITIQUE OF IONIC CONTAMINATION TESTING
FOR SURFACE MOUNT TECHNOLOGY

by

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INTRODUCTION

Ionic contamination testing is perhaps the most commonly used technique for measuring the cleanliness of electronic assemblies. In its simplest form, the test involves washing an assembly with a solution of isopropanol and water, generally 75 vol. % isopropanol, 25% water, and measuring the resistivity of the collected washings. The change in resistivity of the isopropanol/water solution can be related to the equivalent weight of sodium chloride necessary to produce that change.

Over the years several instruments have become available which perform this test quickly and easily. Nearly all of these consist of a chamber or tank containing the isopropanol/water test solution into which is placed the assembly being tested. The solution is circulated while changes in resistivity, or conductivity, are continuously monitored. The utility of this test rests on the assumption that all or nearly all of the residual ionics are extracted by the test solvent and are thus detectable. The ionic contamination test instrument functions, in part, as a cleaning unit with its effectiveness at measuring ionic contamination limited by its ability to clean the assembly being tested. Failure to achieve complete extraction results in overstating the cleanliness of the assembly.

The cleaning problems associated with surface mount assemblies (SMAs) are well known. The small component standoff which is characteristic of SMAs impede the flow of solvent under the components, often resulting in inadequate cleaning. To meet the challenge posed by SMAs, new cleaning equipment is being developed capable of cleaning under small standoffs. Effective cleaning of SMAs is possible using a fluorocarbon solvent in conjunction with a high pressure spray system in the defluxer. See Figure 1 for a depiction of a new in-line defluxer having liquid seals and high pressure sprays. One would expect that small standoffs would impact the effectiveness of ionic test instruments also. This was demonstrated in a study by Bredfeldt in which SMAs were tested in a Model 590 Ionograph*, first with components in place and then with components removed. A significantly greater amount of ionic residue was detected with the components removed than had been measured with the components in place. Since it is neither desirable nor always practical to utilize a destructive test in production, there is a need for more effective ionic testing equipment if this test is to be of value to producers of SMAs.

*Trademark of Alpha Metals Inc.

LESSONS FROM SMA CLEANING STUDIES

Much effort has been expended by the manufacturers and users of defluxing equipment to develop equipment and processes for effectively cleaning SMAs. Studies have generally shown that spraying, often at elevated pressures, is essential to achieve proper cleaning of SMAs. Cleaning processes in which the assembly is simply immersed in solvent for some specified time are largely ineffective, especially when standoffs are small. Thus for cleaning SMAs after reflow it can be demonstrated that spraying is better than soaking. One would expect this to be true for ionic contamination testing of SMAs also. The advent ionic contamination testing equipment in which assemblies are sprayed with isopropanol and water makes it possible to test this hypothesis.

EXPERIMENTAL OBJECTIONS

The objectives of this experiment were to evaluate spraying versus soaking for measuring ionic contamination under closely mounted components, and to determine the effect of standoff on each technique. It should be noted that this is intended to be an evaluation of test techniques, only, and is not an overall comparison of the instruments used.

EXPERIMENTAL PROCEDURES

Two instruments were used in this evaluation. The first instrument, call it Unit A, is a relatively familiar instrument containing a tank in which the assembly being tested is soaked in a 75 vol. % isopropanol, 25% deionized water solution which is recirculated during the course of the test. The second instrument, call it Unit B, consists of a chamber with spray nozzles located on two opposing side walls. During the course of a test the isopropanol/water solution is sprayed onto the assembly. The solvent collects in the bottom portion of the tank, away from the assembly, and is recirculated. Both instruments measure changes in the resistivity of the test solution. Unit A reports both the final resistivity of the test solution and the corresponding ionic contamination level in milligrams of sodium chloride or equivalent per square inch. For our purposes, these values were converted to micrograms of NaCl or equivalent/square inch. Unit B reports only final resistivity. This is converted to micrograms of NaCl equiv./sq. in. by means of a graph provided by the manufacturer.

The assemblies used in this study were bare FR-4 panels onto which were mounted 1" x 3" x 1/8" brass slides. The brass slides were machined and drilled such that each contained a "channel" running nearly the entire length of the slide with a hole on each end through which screws could be inserted. This is shown diagrammatically in Figure 2. The slides were milled so that the "channels" were at a uniform depth of 1, 2, 5 or 7 mils, respectively. These slides could be firmly attached to the FR-4 panels with screws creating fixed standoffs of the dimensions described. The FR-4 panels, brass slides and fastening screws were precleaned to a zero ionic contamination level prior to assembly and were thereafter handled only with gloves.

A fifty microliter (50 μ l) quantity of a liquid RA flux was deposited in the area under each slide and allowed to air dry for 2 minutes, after which the slides were affixed. Each assembly contained 2 slides. The assemblies were passed over a solder wave, flux-side up, to reproduce the temperatures to which an SMA would normally be exposed prior to cleaning and testing. The assemblies were then tested in the two respective instruments, Unit A and Unit B. Four

assemblies per standoff were tested in each instrument. Each test lasted 15 minutes with readings taken at 5 minute intervals. On completion of the first 15 minute test, the assembly was removed from the test chamber and disassembled. All of the component parts were then placed back into the chamber and another 15 minute test conducted. The total amount of ionic contamination on each assembly was taken to be the sum of the amount detected in the first 15 minute test plus the additional amount detected when the disassembled unit was tested.

Before beginning the test sequence, four(4) substrates were prepared as described above except that no brass slides were attached. Two of these were tested in each instrument to demonstrate that, in the absence of any impediment to solvent flow, the instruments are equally capable of extracting ionic contamination in a 15 minute test. The two boards tested in Unit B both yielded a value of $38.4 \mu\text{g NaCl equiv./in}^2$ while the boards tested in Unit A yielded values of $37.9 \mu\text{g NaCl equiv./in}^2$ and $38.6 \mu\text{g NaCl equiv./in}^2$ respectively. For both instruments the final value was actually attained within the first 5 minutes of the test.

RESULTS

Measured ionic contamination levels for each assembly, at each time interval are shown in Tables 1 and 2. The total quantity of ionic contamination found on each assembly is also reported in those tables. From these data, the average percent of total ionics detected at each interval was calculated. The results for both instruments are shown in Table 3.

The data contained in Tables 1-3 show that more complete extraction of ionics occurred when the assemblies were sprayed during the test than when they were simply soaked in the test solution. This was especially true at the smaller standoffs. Spraying yielded average extraction rates ranging from about 78% for the 1 mil standoff to nearly 90% for the higher standoffs. Soaking, on the other hand, yielded average extraction rates ranging from about 15% for the 1 mil standoff to 76% for the 7 mil standoff. In no case was complete extraction achieved within the 15 minute test period, even at the higher standoffs. At best, only about 90% of the total ionics present were extracted within 15 minutes. This is surprising given the relative simplicity of the assemblies used in these tests.

The data also show that extraction of ionics is strongly affected by standoff when the assemblies are soaked. Standoff has a much smaller impact on extractability when the assemblies are sprayed. This can be seen in Figure 3 which shows the average percent of total ionics detected in 15 minutes as a function of standoff for each instrument. For Unit A, the extraction rate is nearly the same at 7 mils and 5 mils but drops sharply as standoff is reduced to 2 mils and to 1 mil. The extraction rate is relatively flat at 7, 5 and 2 mils for Unit B and drops only slightly as standoff is reduced to 1 mil.

There is some indication that the spray method provides a faster analysis than the soak method. With the exception of the assemblies on which the standoff was 1 mil, spraying generally resulted in higher percentage of total ionics being extracted within the first 5 minutes of the test than did soaking.

SUMMARY

It was stated previously that numerous cleaning studies involving SMAs have concluded that spraying is much more effective than soaking, especially when component standoffs are small. It was then reasoned that an ionic contamination test in which assemblies were sprayed with the test solution would generally lead to more complete extraction of ionics, and hence more accurate contamination measurements, than one in which the assemblies were soaked. This was experimentally demonstrated by using two commercially available instruments to measure ionic contamination on simulated SMAs. It was further demonstrated that the effectiveness of the spray method is not strongly affected by standoff while the soak method is strongly impacted by standoff. Finally, and most importantly, it was shown that neither method extracted more than 90% of the total ionics present on the assemblies within a 15 minute test period.

REFERENCES

1. MIL-P-28809A, "Printed Wiring Assemblies", U.S. Government Printing Office, Washington, (1981).
2. Karin Bredfeldt, "How Well Can We Quantify Cleanliness for Surface Mount Assemblies?", Proc. NEPCON West '87, Feb. (1987).
3. John K.(Kirk) Bonner, "Effective Cleaning of Surface Mount Assemblies", Proc. EXPO SMT '87, Oct. (1987).
4. Donald A. Elliott and John Gileta, "In-Line High Pressure Solvent Cleaning of Surface Mount Assemblies - Part II", Proc. NEPCON West '87, Feb. (1987).
5. David S. Lermond, "Model Studies in the Cleaning of Surface - Mounted Assemblies With High Pressure Fluorosolvent Sprays", Proc. NEPCON West '86, Feb. (1986).

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TABLE 1

IONIC CONTAMINATION MEASUREMENTS AT 5 MINUTE INTERVALS - UNIT A

Standoff (mils)	Time (Min.)	Ionic Contamination as Micrograms NaCl equiv/sq.in.			
		Assembly 1	Assembly 2	Assembly 3	Assembly 4
1	5	3.9	3.8	4.9	2.9
	10	3.9	4.7	5.6	3.3
	15	4.8	5.4	6.2	3.7
	D*	30.5	37.9	33.2	35.2
2	5	4.4	3.2	5.9	11.4
	10	6.1	6.2	9.7	17.3
	15	8.1	8.9	12.8	20.8
	D*	29.4	32.6	39.1	31.5
5	5	14.5	15.0	13.9	13.6
	10	19.9	23.5	23.0	22.8
	15	22.8	27.4	26.1	26.2
	D*	30.9	35.2	33.2	37.6
7	5	22.5	22.7	20.4	21.4
	10	26.8	25.4	24.5	25.6
	15	28.3	26.3	25.7	25.6
	D*	40.9	32.6	34.7	32.1

*Total Ionics, i.e. the 15-min. value plus the additional quantity detected when the board was disassembled.

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TABLE 2

IONIC CONTAMINATION MEASUREMENTS AT 5 MINUTE INTERVALS - UNIT B

Standoff (mils)	Time (Min.)	Ionic Contamination as Micrograms NaCl equiv/sq.in.			
		Assembly 1	Assembly 2	Assembly 3	Assembly 4
1	5	14.1	21.3	7.3	8.9
	10	23.8	26.4	19.5	17.5
	15	26.0	29.0	26.2	22.7
	D*	31.5	32.1	30.8	42.7
2	5	26.0	25.1	17.7	-
	10	26.9	28.5	23.0	-
	15	27.4	29.6	25.1	-
	D*	32.1	33.5	30.2	-
5	5	26.9	29.0	26.4	27.4
	10	27.9	29.6	26.9	27.4
	15	29.0	30.2	27.9	27.9
	D*	33.5	32.8	30.2	30.8
7	5	29.6	28.5	25.5	25.1
	10	30.2	29.6	27.4	26.9
	15	30.8	30.8	28.5	26.9
	D*	38.2	32.8	32.1	32.8

*Total Ionics, i.e. the 15-min. value plus the additional quantity detected when the board was disassembled.

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TABLE 3

AVERAGE PERCENT OF TOTAL IONICS DETECTED AT 5 MINUTE INTERVALS

UNIT A AND UNIT B

Standoff (mils)	Time (Min.)	Unit A		Unit B	
		Mean % Detected	S.D.	Mean % Detected	S.D.
1	5	11.4	2.9	38.9	21.2
	10	12.9	3.1	65.5	18.1
	15	14.8	3.4	77.8	16.7
2	5	19.0	11.7	71.3	11.3
	10	29.8	16.9	81.5	4.7
	15	38.4	18.6	86.0	2.7
5	5	41.9	4.4	86.3	4.0
	10	65.3	3.7	87.9	3.1
	15	75.0	4.1	90.4	2.7
7	5	62.5	6.8	80.1	4.7
	10	73.4	6.6	84.2	4.8
	15	76.0	5.4	86.3	6.2

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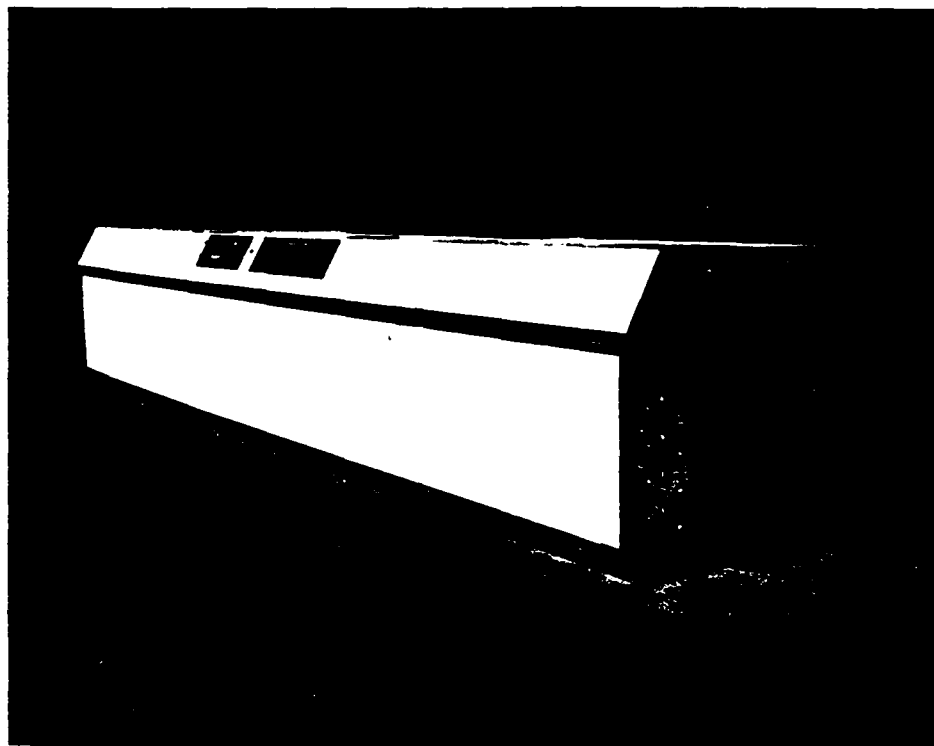


FIGURE 1. In-Line Defluxer With Liquid Seals and High Pressure Sprays.

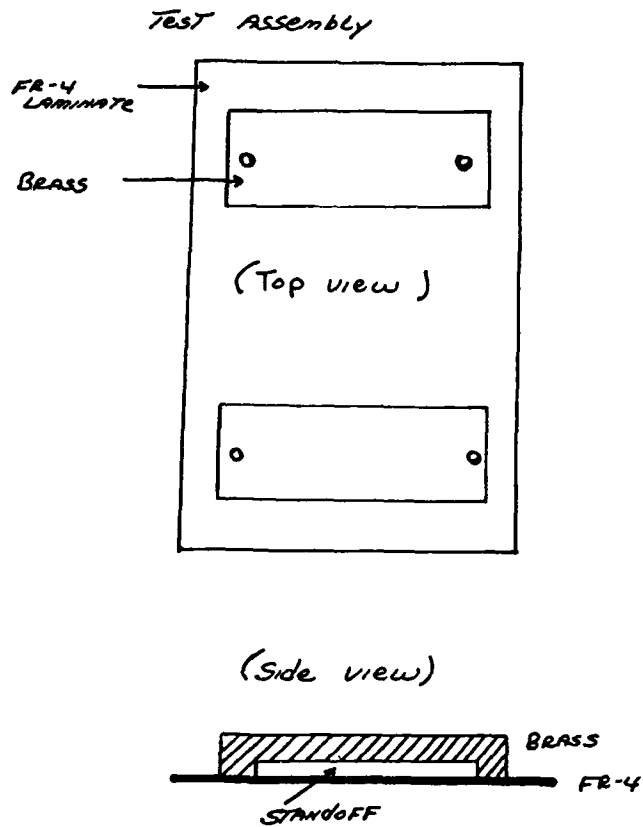
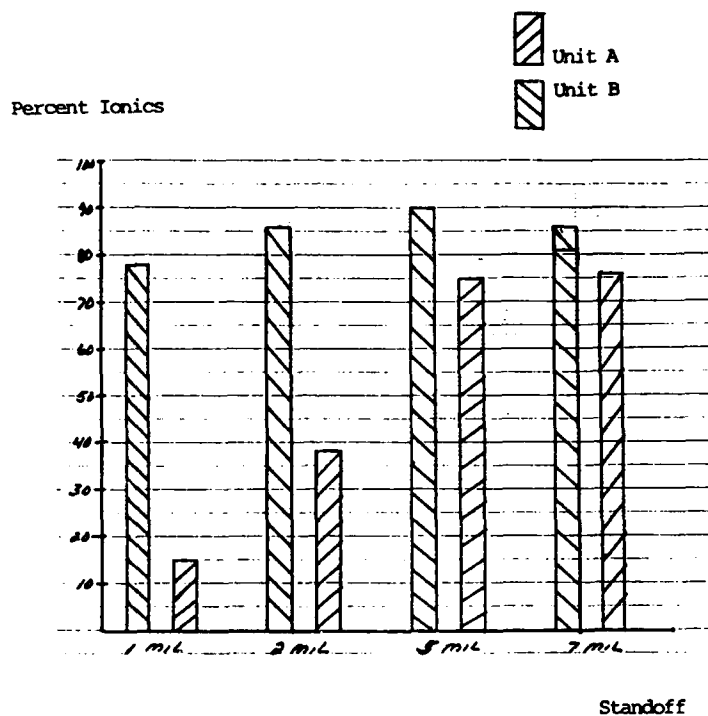


FIGURE 2. Diagram of FR-4 Test Board.

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CLEANING ALTERNATIVES FOR THE 1990's

by

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ABSTRACT

In August 1987, the EPA held a conference in Washington DC with consultants and users from the electronics industry (Reference 1) to determine the feasibility of practical cleaning alternatives to reduce emissions of chlorofluorocarbon solvents which are considered be a major contributor to the ozone problem in the stratosphere the world over.

This paper presents a short resume of these goals and how they will affect cleaning in the Electronics Industry.

Electronic design and packaging are the first steps in the soldering and cleaning processes. Selection of components compatible with alternative cleaning methods as well as process changes to permit low solids fluxes in some cases where cleaning can be eliminated will be discussed. "High containment" in-line solvent cleaning systems which reduce emissions will become the new standard for the industry. Machines will become longer in order to include internal drying stages, instead of allowing a board with residual solvent trapped under components to evaporate after it exits from the machine prior to electronic test. Alternative solvents will become available. Designers of components and assemblies will respecify their designs to permit water cleaning, even for surface mount assemblies.

HISTORICAL BACKGROUND

Many newspaper articles have described "The Hole in the Atmosphere Over Antarctica" and about "The Hazards of Depleting the Ozone Layer". On March 22, 1985, the Vienna Convention for the Protection of the Ozone Layer was adopted. On September 16, 1987, the United Nations Environment Program (UNEP) Diplomatic Conference concluded with the signing of the Montreal Protocol on substances that deplete the ozone layer. The agreement was signed by 24 nations and the European Economic Community (Reference 2).

The compounds covered in the agreement include CFC's 11, 12, 113, 114 and 115, and Halons 1211, 1301, 2402.

CFC 113 is widely used in solvent cleaning of electronic assemblies because of its gentle nature, - it does not attack plastics or other materials. Another benefit has been its long term chemical stability. However, when the solvent evaporates from an electronic assembly as drag-out or when it is lost from a defluxing tank or machine, it is this same stability which results in it remaining so long in the atmosphere causing the the long term problem in the ozone layer.

CFC's 11, 12 and 115 are used as refrigerants in the heat pumps or refrigeration systems in solvent cleaning equipment. CFC 11 is also used in some cleaning solvents.

Halons are used as fire extinguishing chemicals in production machinery such as wave soldering equipment as well as electronic facilities installations, for example, in a computing center.

GOALS TO REDUCE CONSUMPTION AND PRODUCTION OF CFC COMPOUNDS

Emissions of CFC 113 in the manufacturing of electronic assemblies occur primarily during the removal of flux from boards after soldering and therefore this paper concentrates on solvents containing that compound and on the alternatives. The detailed objectives are outlined for all CFC's in Reference 2.

- Freeze consumption on production of the CFC compounds at 1986 levels beginning on the first day of the seventh month after the date of entry into force (EIF);
- Reduce consumption and production of CFC compounds to eighty percent (80%) of 1986 levels beginning in a twelve month period of July 1, 1993 to June 30, 1994;
- Further reduce consumption and production of the CFC compounds to fifty percent (50%) of 1986 levels beginning in the twelve month period of July 1, 1998 to June 30, 1999.

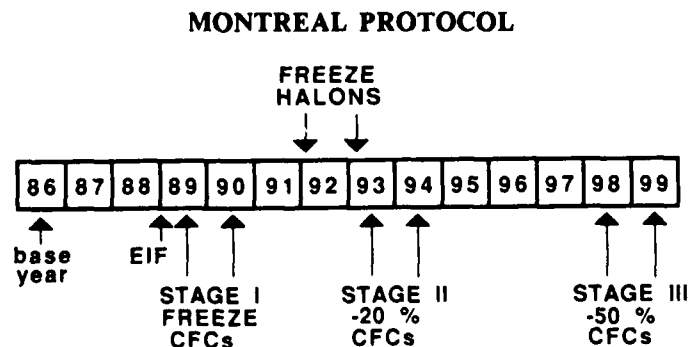


Figure 1. Timetable for Reductions in Consumption.

TIMETABLE FOR ELECTRONIC DESIGNERS AND MANAGEMENT

Using the above timetable as a reference, managers in the electronics industry will need to adopt policies and issue directives as soon as possible so that designers of electronic assemblies will have sufficient time to consider the alternatives and to be ready with their new product which can be cleaned according to the guidelines and which will meet the timetable for reductions in consumption of CFC 113 or other solvents containing this compound.

Major electronics companies are making corporate decisions immediately to begin studying the alternatives and to be prepared with their new designs. These companies are not leaving it to the last minute. They are initiating pro-active plans, not only to meet these goals but to be prepared in time so that they can clean their electronic assemblies properly and in equipment which will be in place for these new products, long before the eventual transition arrives.

These same companies are checking how much CFC 113 or other solvents containing this compound were purchased in 1986. They are establishing their own goals to meet or exceed the timetable for reductions. Otherwise, the day may arrive, perhaps in 1993 to 1994 when the CFC 113 solvent they are presently using is no longer available part way through their production year.

EQUIPMENT ALTERNATIVES

Manual Solvent Cleaning

Cleaning by Hand. Two simple suggestions are offered:

- Eliminate solvent aerosol spray cans containing cleaning solvent from the work place.
- Eliminate the use of open tray cleaning.

Open Top Vapor Degreasers. These machines comprise a very competitive market segment of the solvent cleaning equipment for the electronics industry. Depending on options, prices can range from very low to moderate. Because of the ready availability of low cost solvent defluxers, there are many in use. These are operated manually by hanging the assembly on a hook or placing several in a wire basket.

All manufacturers provide careful instructions on the proper use of their equipment. In addition, there are several excellent documents which highlight equipment design, how to use the defluxer and how to minimize solvent losses.

Reference 3 outlines that in the U.S.A., "All State and Federal Safety Agencies require that ingress/egress speeds must not exceed 11 ft/min" (3.4 m/min). Reference 4 refers to "a slow speed, in the range of 3-7 m/min" (9.8-23 ft/min). Otherwise the vapor line will be disturbed as the basket containing the assemblies is lowered or removed from the equipment. This "piston" effect causes solvent vapors to be pumped out the unit. It is impossible for an operator to manually lower or lift out a basket

containing assemblies at such a slow speed. In tests, the speed of operators was measured and reported to be in the range of 300-1000 ft/min (100-300 m/min).

The following recommendations will reduce solvent emissions:

- Install top covers on open-top vapor degreasers.
- Train operators to keep the covers closed when not in use.
- Install top covers which close automatically when not in use.
- Retrofit automatic hoists to vapor degreasers and program them for proper entry/exit speeds including dwell time to permit evaporation while the assembly is in the vapor zone. The assembly will be dry and more solvent will remain in the machine.
- Study your needs if planning for more vapor degreasers and consider replacing them all by sending all the electronic assemblies through one new in-line conveyorized solvent defluxer. It has been reported that some companies have as many as forty vapor degreasers on their electronics production floor. Each time an additional component is hand soldered to the assembly or each time that solder joint touch-up is performed, the assembly is cleaned once more in the nearest available open top vapor degreaser.

Reducing Losses from In-Line Solvent Cleaning Equipment. Some cleaning solvents have an objectionable odor, others are considered to have a toxicity level at which point workers begin to complain and/or the area must be evacuated. One of the benefits of CFC 113 or other solvents containing this compound is its mildness in the working area. In the past, if assemblies still wet with solvent were permitted to dry at room temperature after exiting from the solvent cleaning equipment, the operators did not find it objectionable. The relatively low evaporation temperature permitted the boards to be dry within a few minutes so that electronic bed-of-nails testing could be undertaken almost immediately.

In order to reduce emissions from such equipment, there are several alternatives:

- Recover the solvent by installing a two stage carbon absorption steam regenerated solvent scrubber to collect the exhaust fumes containing the solvent.
- Replace existing solvent cleaning equipment with newer equipment of the "high-containment" type.

Steam regenerated scrubbers are not only expensive, but it is difficult to properly separate the steam and the solvent properly. With azeotropes or blended solvents, the alcohols may not be regenerated correctly. Chemical balance of the constituents, including stabilizers, in the azeotrope or blended solvent is critical and difficult to monitor, to re-establish and to maintain under proper control or some regenerated solvents may become acidic.

In-line solvent cleaning equipment has generally been of the design which takes the product down a gentle slope into the hot vapor zone where nozzles improve the cleaning effectiveness by spraying solvent at a pressure of about 10-15 PSI (.7-1.0 bar). Then the conveyor gently rises again to the unload end. With the advent of surface mount components with very small spaces between the bottom of the component and the surface of the board, solvent cleaning equipment is now available with higher pressures. However, the higher the pressure, it is normal to expect more spray to come out of the entrance and exit openings of the machine. This results in higher solvent emissions from most equipment.

New equipment is presently available (References 5 & 6) of the ultra high pressure type. Because of the novel design concept, spraying at pressures up to and above 250 PSI (17 bars) is possible without increasing emissions from the entrance and exit openings of the equipment.

Depending on the conveyor speed through the machine, the time that an assembly stays in the unload vapor zone and other considerations, much of the solvent which would normally remain as a wet residue on the assembly on should be allowed to evaporate or should be removed from the assembly while it is still in the machine. High containment solvent cleaning machines, some of which are already in the design stage to meet the desired goals of reducing emissions, will eliminate the need for exhaust ducts and expensive steam regenerated scrubbers with their associated problems.

ELECTRONIC DESIGN - THE FIRST STEP IN THE CLEANING PROCESS

The electronics designer has about 18 important parameters to consider when designing a new product. At the design stage, manufacturability is a low priority. Remember that design is a first step of the soldering and cleaning process.

Many electronic products in the home entertainment category are not cleaned. More consideration should be given at the design stage so that more new products do not require cleaning.

If cleaning is required in order to permit high speed automated bed-of-nails testing, consideration should be given to one of the fluxes whose residues need not be removed. (Reference 7).

The electronic designer has time to implement his new designs within the timetable outlined in Figure 1. Now is the time to begin. He will need to select components which are compatible with whatever cleaning solvent will be adopted for use in the future. The plastic materials, ink markings, etc. must withstand any alternate solvents which are being considered. The selection of components and the solvent adopted will probably dictate a required stand-off height or clearance between the bottom of surface mount components and the board to permit acceptable cleaning under such components.

For example, if some components or open relays are not compatible with the alternate solvent, or water if that is the case, electronic designers will be required to select components that are compatible. They will need to work closely with their buyers

and component suppliers to find components which are compatible. Most probably, they already exist. It may just be a matter of looking for them.

ALTERNATE SOLVENTS

Alternate commercially available solvents, blends or azeotropes of the halogenated family or those containing Fluorocarbon 112 which is not on the agreed list and others which are acceptable in the electronics industry for some products could be adopted, providing components are compatible. Once again, it comes to the selection of the proper parts by the designer.

Because some of these solvents may be considered objectionable if excessive losses occur in the working area, new solvent cleaning equipment should be of the "high containment" type.

Some in-line solvent cleaning equipment might be converted. Before purchasing a new in-line solvent cleaner, inquire from the manufacturer of the equipment whether the machine could be convertible. That is, for existing products which presently require the use of CFC 113 type solvents, cleaning equipment will operate for now with that solvent, but the machine could be converted for another more environmentally acceptable solvent once the new products are designed where the component selection is compatible with that new solvent. In some cases, where electrical heating and refrigerated or cold water cooling is specified in the purchase of new equipment, it may be a simple matter of merely changing the seals for the pumps and access doors and possibly an adaptation of the desiccant dryer for use as a water separator.

In the future, factories will have more than one type of in-line cleaning machine. There will be one for existing products which must continue to use solvents containing CFC 113 and where the expected life of that product makes it uneconomical to redesign it. Side by side that machine will be another machine containing the newly selected solvent for new electronic designs which are compatible with the new solvent.

It should be remembered that the new solvent might be water, the most common solvent on this planet.

THE SEARCH FOR NEW SOLVENTS

Research chemists in the laboratories of solvent producers are searching for alternate solvents which are compatible with present requirements for acceptable cleaning of electronic assemblies. To present a simplistic example, if a CFC compound on the agreed list were to be blended with 20% of another solvent, then meeting the requirements of the period into the mid 1990's will have been achieved. It has been stated that it may take 5-10 years to complete the toxicological studies. Therefore, the solvent producers are conducting studies of many new alternative solvents, combinations, blends, etc. in parallel investigations to meet the goals of reducing emissions of solvents that deplete the ozone layer.

Depending on the chemical nature of those solvents, existing cleaning equipment may need modification or complete redesign depending on the solvency power, operating temperature and other factors.

WATER - THE MOST ABUNDANT SOLVENT IN THE WORLD

Reluctance to Use Aqueous Cleaning

Design Aspects. In the mid 1960's, several factors led some computer companies to adopt water cleaning. Water soluble fluxes would permit lower touch-up rates after wave soldering assemblies where the solderability of the board was a questionable variable. Lower touch-up means lower manufacturing costs as companies achieve rates closer to zero defect soldering. Some are achieving 5-10 defective joints per million (5 -10 ppm) and 95-99% yield on first pass after wave soldering and water cleaning without touch-up.

It must be highlighted that these electronic assemblies were either designed to use water soluble flux and water cleaning or by their simple nature of having mainly dual-inline-packs (DIPs) which are encapsulated in plastic, they were already compatible with water soluble fluxes and aqueous cleaning. The small shoulder on every lead of a DIP was designed to provide sufficient clearance under the component to permit the water to flush the flux residues away.

This stresses the need for proper packaging design before adopting a cleaning method. As another example, stranded wires covered with an insulating material should not be used with water soluble fluxes. It is not possible to ensure that all of the water soluble flux residues are removed. Therefore, the designer must select another kind of wire or attachment method which is compatible with the soldering and cleaning process.

Military Requirements. Because of the type of problem described above, and the need for high reliability, the requirements for military applications have specified only the mildest of rosin fluxes. Specifications require that the solvent to be used for cleaning these flux residues after soldering must not attack the materials used. Therefore, the trend has been to use the mildest solvents which can effectively remove rosin type fluxes.

When an electronics manufacturer is producing military assemblies as well as commercial products, he will clean all of his assemblies in the same equipment. And because of the military products, that equipment is never of the aqueous type.

Until the military specifications are reworded and adequate testing has been undertaken, water cleaning of military assemblies will not be permitted.

Drying Electronic Assemblies. It is essential that an electronics assembly be totally dry before undertaking any electronic testing. Because of the low boiling points and high evaporation rates of solvents, electronic assemblies will become dry very quickly after being removed from any type of solvent cleaning equipment.

Cleaning with water means that drying an electronic assembly is more difficult. What it really means is that the dryer stage of a good water cleaning machine should be designed and selected with the product in mind and the production rate desired which subsequently dictates the conveyor speed. Therefore, to meet the specific drying requirements of the customer, the machine manufacturer will recommend the number of blower modules followed by the required number of dryer modules.

Some equipment manufacturers have been building water cleaning and drying equipment for the electronics industry for 20 years. To adequately dry a given assembly in a specified time, the machine will become longer. While factory space is a premium, proper drying requires adequate time within the machine. It should be pointed out that the selection of a properly designed solvent cleaner which meets the goal of reducing emissions will also need to be longer to contain the solvents in the machine rather than permitting them to evaporate from the assembly after exiting from the machine.

Environmental Disposal of Waste Water. In North America, there are a multitude of federal guidelines and local regulations, both at the state and at the municipal level. While the EPA is strongly promoting the reduction of solvents which deplete the ozone layer, they will be coordinating efforts within other environmental groups to make it easier for the electronics industry to adopt water cleaning with respect to waste water disposal.

This will help the small manufacturer who cannot afford the expensive water purification systems which recirculate the water with a very high purity (References 8 & 9). Most of the large systems are very expensive. However, lower cost water recycling systems will become available as more in the industry consider switching to water cleaning.

Surface Mount Technology. When the electronics industry in Japan began soldering surface mount components to conventional circuit boards, many in the rest of the world said that it would not work reliably. We now know that it is reliable. Then the industry said that there is "absolutely no way that an assembly containing surface mounted components will ever be properly cleaned using anything but a solvent".

However, many companies are investigating cleanliness for surface mount assemblies (References 10 & 11), and some of these investigations are for aqueous cleaning of surface mount assemblies.

Other companies have completed their studies and are already using water soluble fluxes in their wave soldering equipment and achieving reliable quality using aqueous cleaning equipment for surface mount applications (References 12 & 13).

Water Cleanable Solder Paste. Since solder paste for the electronics industry has only been available with rosin flux, cleaning is generally undertaken in solvent cleaning equipment after soldering. The solder paste manufacturers have had water cleanable solder paste for many years for other industries, i.e. the auto body repair market. With more demand to reduce emissions of CFC's, the electronics industry will begin investigations using solder paste where the flux residues are water cleanable.

AQUEOUS CLEANING EQUIPMENT

Water, Saponifier or Neutralizer. The decision to switch to aqueous cleaning depends on the entire process. Whether city tap water or very high purity water is required depends on the electronic design, the choice of flux, the ability to clean the flux residues as well as the desired reliability.

The addition of a saponifier or detergent in the first stage of an aqueous cleaning system is required when removing rosin flux residues.

Neutralizers are rarely needed but are a consideration to neutralize the water soluble flux residues in the first stage of an aqueous cleaning system.

Batch Cleaning Machines. These are ideal for small shops, laboratory investigations, or companies just starting in aqueous cleaning, although some companies will use several to meet higher production rates. They are essentially industrial dishwashers modified for the specific needs of the electronics industry. They are available with special programmable cycles and optional resistivity control which permit the equipment to produce desired cleanliness levels. Optional separate batch dryers are also available.

In-Line Conveyorized Aqueous Equipment. A well designed aqueous machine should be modular for flexibility. This permits the customer to select the proper equipment depending on whether water soluble fluxes are used or whether a saponifier is required when rosin flux residues are to be removed. Additionally, the same machine might contain the required modules to permit cleaning of both types of flux residues. Finally, a modular design permits additional dryer stages to meet those requirements.

In-line aqueous cleaners are available in the small, medium and long variety. The longer ones clean and dry better and/or at faster conveyor speeds. Some are computer controlled.

All aqueous cleaning systems can be environmentally acceptable with the installation a recycling water systems which purify the water before sending it back to the final rinse stage or by neutralizing the waste before disposal. Reference 14 describes such an installation in detail.

SUMMARY

Twenty-four countries have signed an agreement with the intention of reducing emissions of solvents which deplete the ozone layer. Over the next ten years, designers of electronic assemblies, manufacturing engineers, component suppliers, equipment manufacturers and chemical suppliers will work together to produce assemblies which are designed so as to permit cleaning by other methods. This also includes electronics for military applications and these with surface mounted components.

The trend in manufacturing will be to have two fluxers in a wave soldering machine, one containing rosin flux for present electronic designs and the other containing a flux which is required for new designs.

Manufacturing facilities will have two types of cleaning equipment. One will contain their present solvent while the second machine will be used with the new solvent. New equipment will be specified, designed and available for use with present solvents and, once all present designs become obsolete or are redesigned, the equipment can be converted for the new solvent.

The alternate solvent for cleaning after soldering in many cases will be water. If new design guidelines to permit an environmentally acceptable cleaning method are required, companies will choose to study very closely, the most environmentally acceptable solution, water cleaning, due to the problems of other solvents in the workplace.

Solder paste which is compatible with aqueous cleaning will require experimentation and development.

It is the moral responsibility of everyone in the electronics industry to work towards finding alternate cleaning solutions for their products to reduce emissions of solvents which deplete the ozone layer.

REFERENCES

1. "Chlorofluorocarbons In The Electronics Industry - A Use and Substitute Analysis", Part 7, Vol. 3 - "Regulatory Impact Analysis: Protection of Stratospheric Ozone", Docket A-87-20, Dec. 1, 1987, US EPA, Washington, DC.
2. "Montreal Protocol on Substances that Deplete the Ozone Layer", Final Act, 1987, United Nations Environment Programme (UNEP).
3. IPC Standard "Post Solder Solvent Cleaning Handbook", ANSI/IPC-SC-60 April 1987, IPC, 7380 North Lincoln Avenue, Lincolnwood, IL 60646.
4. Commission of the European Communities, "Code of Practice for the Design, Construction and Operation of Chlorofluorocarbon CFC-113 Solvent Cleaning Equipment", Report EUR 9510 EN, Directorate-General XI, B-Brussels, 1984.
5. D.A. Elliott and J. Gileta, "In-Line High Pressure Solvent Cleaning of Surface Mounted Assemblies - Part I", presented at China Lake, California, February 18-20, 1987. Proceedings of 11th Annual Electronics Manufacturing Seminar, p. 7-16.
6. D.A. Elliott and J. Gileta, "In-Line High Pressure Solvent Cleaning of Surface Mounted Assemblies - Part II", paper presented at Nepcon West '87, Anaheim, California, February 24-26, 1987. Nepcon Proceedings, p. 717-723.
7. W. Rubin, "The Development of Soldering Products whose Residues Need Not Be Removed", paper presented at ISHM '87, Minneapolis, Minnesota, September 28-30, 1987. ISHM '87 Proceedings, p. 243-248.

8. I. Goldstein, "Aqueous Cleaning: A Systems Approach", Insulation Circuits, May 1980, p. 31-34.
9. T.V. Tran, "Advanced Membrane Filtration Process Treats Industrial Wastewater Efficiently", Chemical Engineering Progress, March 1985, p. 29-33.
10. K. Bredfeldt, "How Well Can We Quantify Cleanliness for Surface Mount Assemblies?", paper presented at Nepcon West '87, Anaheim, California, February 24-26, 1987. Nepcon Proceedings, p. 165 -172.
11. A.L. Danford and P.A. Gallagher, "SMD Cleanliness In An Aqueous Cleaning Process", paper presented at Nepcon East '87, Boston, Mass., June 9-11, 1987. Nepcon Proceedings, p. 245-255.
12. R. Aspandiar, A. Piyaali and P. Prasad, "Is OA OK?", Circuits Manufacturing, April 1986, p. 29-36.
13. R. Aspandiar, P. Prasad and C. Kreider, "The Impact of Using an Organic Acid Wave Solder Flux on the Cleanliness of Surface Mount Assemblies", paper presented at Nepcon West '87, Anaheim, California, February 24-26, 1987. Nepcon Proceedings, p. 277-289.
14. S.A. Sheldahl and J.S. Horton, "An Environmentally Preferred Alternative to the Use of Chlorinated Solvents for Circuit Pack Underbrush Cleaning", IPC Technical Review, June 1987, p. 15-23.

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Don is the inventor of Electrovert's Lambda Wave and holds several patents. He has published many articles relating to printed circuit soldering and cleaning, a number of which have been published in foreign languages. He has made presentations throughout North America, Europe, and the Far East, and is an active member of the Institute of Printed Circuits.

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THE TRIALS AND TRIBULATIONS OF IMPLEMENTING SURFACE INSULATION RESISTANCE TESTING

by

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ABSTRACT

The trials and tribulations of implementing surface insulation resistance (SIR) testing are described. This covers the boards under test, the chamber, the cable system, the data acquisition and measurement system and the Lotus computer program. Current testing capacity is 12 boards, each with 8 patterns, run for 96 hours. Output is both tabular and graphic.

INTRODUCTION

Telecommunications, a division of Rockwell International, is a manufacturer of microwave and fiber optic communication equipment. Telecommunications makes only a few special components and have all circuit boards manufactured by outside suppliers.

In mid 1985 BELLCORE (Bell Communications Research) made their presence known beyond the marketing suite. BELLCORE, while not a customer per se, does influence the standards and the equipment bought by other Bell operating companies. Therefore, they wanted to know how we make the product, what we are doing to enhance reliability, and how we are controlling these processes. The refreshing part is that they were knowledgeable and cooperative. We now have regular interactive meetings with their Quality Assurance personnel. These meetings have enabled us to better understand their needs and them to understand our processing methods.

One of the significant requirements called out in their specifications was that we employ surface insulation resistance (SIR) testing as a measure of the cleanliness of the circuit boards after the wave solder and wash process.

Because of this requirement and our continuing effort to improve reliability we now have a fully installed and operating automated SIR testing capability. This system performs data acquisition, data filing and display of the results in both tabular and graphic forms. As you will see it was not as simple as it appeared.

SUMMARY OF SIR TEST

The SIR test is a test of the resistance of a dielectric surface bounded by parallel lines of conductors. It is run at elevated temperatures and humidity over an extended period of time. The intent is to evaluate the tendency of contaminants on the board to cause current leakage paths between adjacent circuit conductors. This is a brief explanation of the problem however Emery Gorondy's papers (References 1 and 2.) go into a thorough explanation of the contaminants and their effect on the SIR values. The normal test pattern is an interposed comb pattern and may have various spacing, line widths and lengths of lines. A generic pattern is shown in Figure 1.

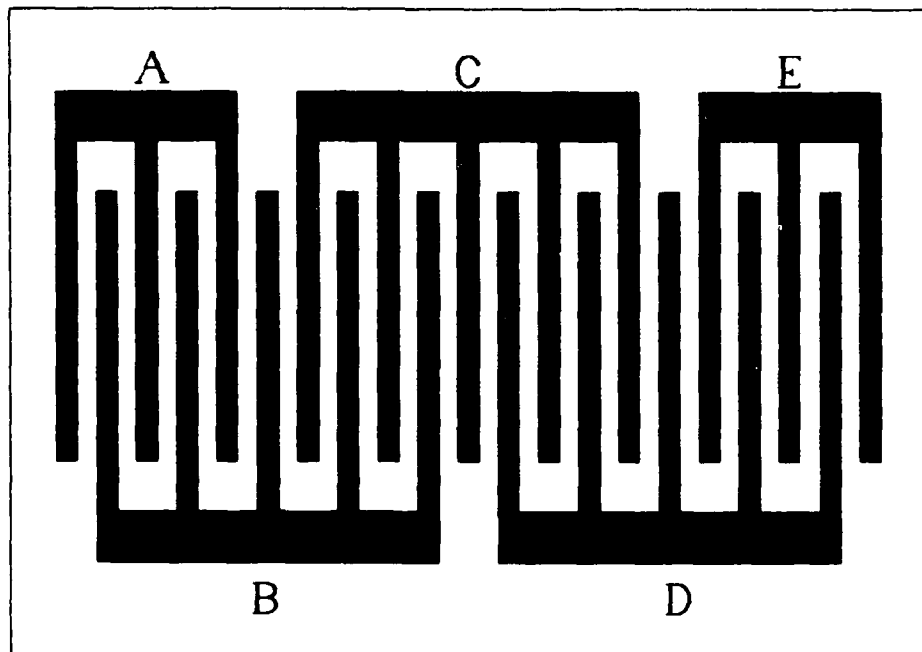


FIGURE 1. Generic Surface Insulation Resistance Pattern.

As SIR patterns are of varying geometries some method must be employed to relate a pattern with many fine lines and close spaces to a pattern with few coarse lines and wide spaces. The units of comparison are the number of "squares".

A little expansion on "squares". On a planar surface, of effectively infinite dimensions, ohms/square is the unit of measure for surface resistance. That is, the resistance across the opposite sides of a square one unit on a side. When the series resistance path is increased by n times and the parallel path width increased by n times the resultant equation is:

$$R_n = \frac{n R_{\text{squares}}}{n} \quad \text{or} \quad R_n = R_{\text{square}}$$

The dimensions drop out and leave only the term "square" or "squares". Schematics of two sizes of "one square" are shown in Figure 2.

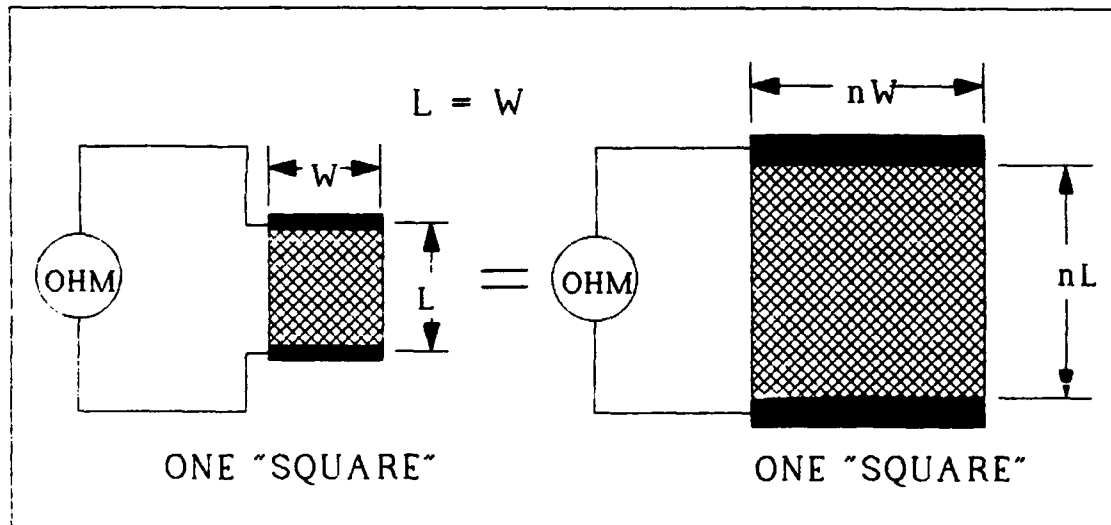


FIGURE 2. Equivalent Squares on an Infinite Surface.

Now how do we arrange squares to change resistance of a circuit? If squares are in a line in series (Figure 3, "ONE THIRD SQUARE"), making the current path longer than it is wide, the resistance increases like resistors in series, and the total resistance is

$$R_{series} = R_{square} \times \frac{l}{w}$$

Conversely, if squares are side by side (Figure 3, "THREE SQUARES"), making the current path wider than it is long, the resistance decreases like resistors in parallel. In this case the total resistance is

$$R_{parallel} = R_{square} \times \frac{w}{l}$$

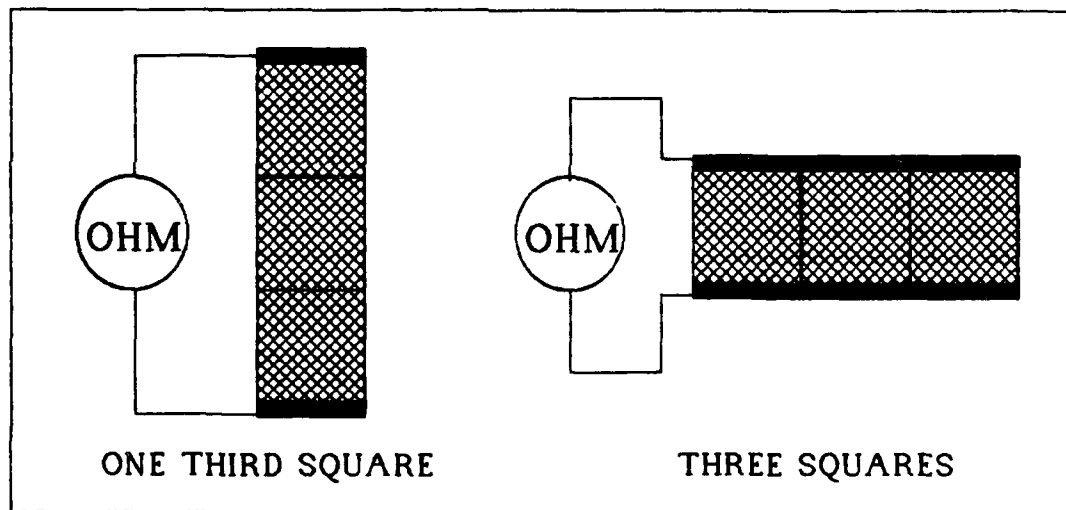


FIGURE 3. Squares in Series and Parallel

As it is necessary to lower the resistance to a value that can be readily measured with standard instrumentation, cabling, etc., the number of squares must be increased by several orders of magnitude. Table 1 details some of the common patterns called out by IPC as well as the one Rockwell is presently using per the BELLCORE requirements.

TABLE 1. Comparison of Various SIR Test Patterns

Pattern Type	Number of Spaces	Length of Line, Inches	Space Width, Inches	Number of Squares	Minimum Resistance Value, x E9
One square	1	1.0	1.0	1.0	337.0
BELLCORE,*	5	1.125	0.050	112.5	3.0
IPC 100043, J1	17	1.0	0.020	850.0	0.4
IPC 100043, J2	17	1.0	0.010	1,700.0	0.2
IPC B-25, A	23	0.625	0.00625	2,300.0	0.015
IPC B-25, B	11	0.625	0.0125	550.0	0.61
IPC B-25, C	5	0.625	0.025	125.0	2.7

* This is the pattern used to meet BELLCORE requirement. All other values in the last column are related to this value.

For a "clean" printed wiring board at the BELLCORE minimum SIR value the resistance for one square would be 0.3 teraohm. The very small currents flowing across a .3 teraohm resistor are beyond the sensitivity of most instruments. With the additional problems of stray currents and crosstalk some other method must be used to get to a reasonable value. The generally accepted method to lower the resistance, when only one value of resistor is available, is to place resistors in parallel.

With that review on squares and the SIR patterns we can return to the actual testing. Since the SIR test is completely invalidated if the test board is not significantly cleaner than the final specification requirement we check the new test boards by running an abbreviated 12 hour test. We use a value of 100 gigaohm (100 x E9) minimum before accepting the boards as test boards for evaluating the process. This gives a margin of 33 times the minimum specification value. More about this later. We then package the board in virgin clear polyethylene bags for transportation to and from the wave solder process. (In this case we prefer not to use an antistatic bag because of the unknown effect of the antistatic agent on the SIR test.) At the wave solder process the board is placed on the conveyor, run through the standard wave solder process, washed in the standard process, dried, and returned to the laboratory for evaluation.

In the laboratory we clean the chamber and female connectors on the backplane, check the DI water supply and initialize the computer program. By holding the board thru the polyethylene bag we are able to load the test boards into the backplane without adding fingerprints or other contaminants. We close the chamber, turn on the computer, turn on the power and forget about the test for 96 hours. Actually, it is a little over 104 hours by the time the final set of readings are completed. Operating temperature is nominally 35°C and 90% RH (relative humidity).

After the 96 hour test is complete the data automatically prints out in both tabular and graphic forms. As we are on a 12 board per week, 104 hour cycle, we have 2 days that the chamber is available for checking incoming boards for cleanliness using the abbreviated 12 hour cycle.

TRIALS AND TRIBULATIONS

Now to our "trials and tribulations"--- When my group, the Material Evaluation Laboratory, received the assignment to setup this test we thought, "No sweat, its just resistance measurement". Were we mistaken. Our first try was with an existing setup that involved an old chamber, boards plugged into a loose connector and testing with a megohm bridge. Nothing passed, not even the bare connectors.

It was evident that significant changes needed to be made. We were fortunate in locating a surplus stainless steel temperature/humidity chamber that was in pristine condition. After we repeatedly cleaned the cable harness we were able to get satisfactory results. Now, the major problem was overtime since testing is required each 24 hours. Also, this is a boring test to run as the operator has to apply a 100 volt bias for 1 minute, then check the resistance. But, we were in business!

It immediately became clear that this was one place where automatic data acquisition would pay for itself. We found several data acquisition systems on the market that were suitable, but the ACRO Systems was capable of communication via either RS-232 or IEEE-488, had modules that had 32 relays per board and was competitively priced. Initially we set up on a HP85 that was available in the lab. The EE in the lab programmed the computer to run the full process and collect data. We then built a backplane that had compliant pin connectors for the boards. The use of compliant pins eliminated the need for soldering and the associated flux insuring that we would have no entrapped fluxes to interfere with the test.

We also used an HP quartz thermometer for wet bulb and dry bulb readings within the chamber. Thus the program not only watched the SIR values but plotted the temperature and via an algorithm the RH. We did have difficulty finding a psychometric chart that was as accurate as the temperature measurement. The actual SIR measurement was with a Keithley electrometer that was programmed (externally by the HP85) to apply the bias voltage then take 5 resistance readings. The HP85 averaged these 5 readings and printed the results. This system was now setup to automatically run and record data on 12 boards, each with two SIR patterns.

Testing went along smoothly for a while. Readings were in the 15 megohm range and valid data was not too difficult to obtain. Also, interferences such as crosstalk, leakage paths, etc. were not a significant problem. However, we were using the IPC "A" pattern, and had trouble with solder bridging during the wave solder operation as this pattern has 6 mil spaces. At times we had to blow away shorts using a soldering iron and a quick burst of nitrogen gas. Needless to say, any unnecessary handling of the test board is bad; this was worse: we were getting good readings, though.

Because of the tendency for bridging and the requirement to match our customers pattern we switched to the recommended "BELLCORE" pattern. It has 25 mil lines on 75 mil spacing, (see Table 1.) The consequences, none; just a different scale on the meter. (Remember, I said we were mistaken in thinking this was a simple measurement.) Since there are only 112 squares vs. the 2300 squares of the "A" pattern we stepped up 2.5 orders of magnitude on the pass/fail criteria. This meant we needed to measure two orders of magnitude past that, which is 300 gigohms (3E11). Fortunately the electrometer would read up to one petaohm (1E15) if the operating mode was changed.

The simplest form of resistance measurement is to apply a known current and read the voltage drop across the resistor as we had been doing. This is known as the SOURCE I, READ V mode. Now we found that at higher resistances the values were in error, would drift and were not repeatable. We changed to the SOURCE V, READ I mode where voltage is applied across the resistor and the resultant current read. Internal operational amplifiers make low current reading possible, however low currents also required more shielding, cleaner connectors, and eventually the elimination of the backplane. (See Figures 4 and 5 for the comparative circuits.)

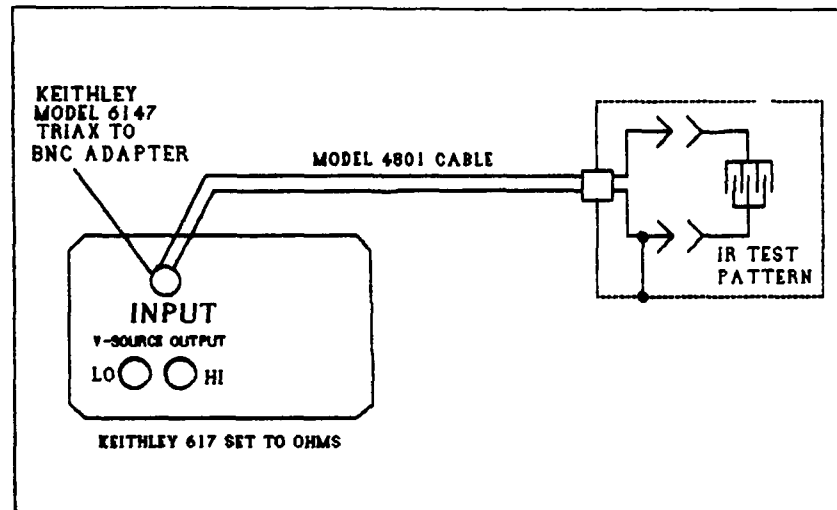


FIGURE 4. Source I, Read V.

In the SOURCE I, READ V mode an external current is applied across the pattern and a high-impedance voltmeter measures the drop across the resistor. The current is then calculated automatically.

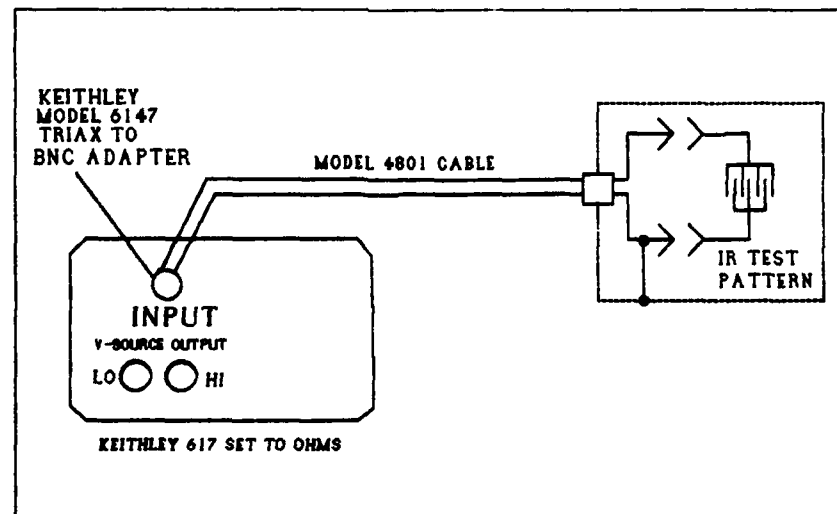


FIGURE 5. Source V, Read I.

In the SOURCE V, READ I mode a potential of 100 volts is applied and the resulting current measured. Resistance is then calculated automatically.

Even though we were getting numbers, an engineering technician in my laboratory started questioning the validity of the results. He began to characterize the system to determine the effect of each item on the resultant measurement. Step by step he disconnected each portion of the system starting at the board and working toward the electrometer. At every change he ran the system as though he was testing boards and checked the results. Finally, after disconnecting the relay modules from the electrometer he was able to obtain values in the teraohm range. This isolated the problem to the relay modules. After cleaning the relay modules in TMS he started getting values up in the teraohm range, (See Table 2).

TABLE 2. Effect of Contaminants on the Relay Module
Printed Wiring Board.

	Mean	Std. Dev.	Maximum	Minimum
Uncleaned relay modules, nothing connected	7.1E10	1.7E10	1.0E11	3.4E10
Cleaned relay modules, nothing connected	1.5E13	1.7E12	1.7E13	1.0E13
Cleaned relay modules, with cable harness and backplane	3.2E12	6.5E12	4.3E12	8.0E11

As the system was reassembled, we found that a conventional backplane introduced parallel leakage paths, so we cut out the area behind the connector which left the connector pins floating free of the backplane. We replaced the ribbon cable harness with individual wires. The two leads that would be energized during a single test, such as A to B in Figure 1, were placed in separate Zipper shielding. Now the system consistently provided values in the teraohm range. The final test was a 96 hour run with test boards installed. After the run and with the boards removed the system was still in the teraohm range. Now our system worked.

The first several runs went beautifully. Then the relays started sticking after about 800 contact closures. We knew it was common practice to guard against contact arcing with inductive loads but these were all resistive and had very low currents. After investigation, we found that the electrometer has a capacitance kick that arcs on "make" and caused the problem. To solve this we added a 100 Kohm resistor between the electrometer and the relay module reducing the inrush and eliminating the problem. As this only added 1E+5 ohms in series it is never seen in the SIR measurement.

Current configuration:

With 5 different sites producing boards our current schedule is 10 boards per week. We have added 12 more relay modules, which is maximum due to the addressing scheme of the ACRO Systems' CPU. We made a modular backplane, designed new test boards and transferred the data handling program to an IBM/PC. Each of these will be addressed individually. (Figure 6 shows a partial schematic of the measuring circuit. Figures 7 and 8 show the system as it is now configured.)

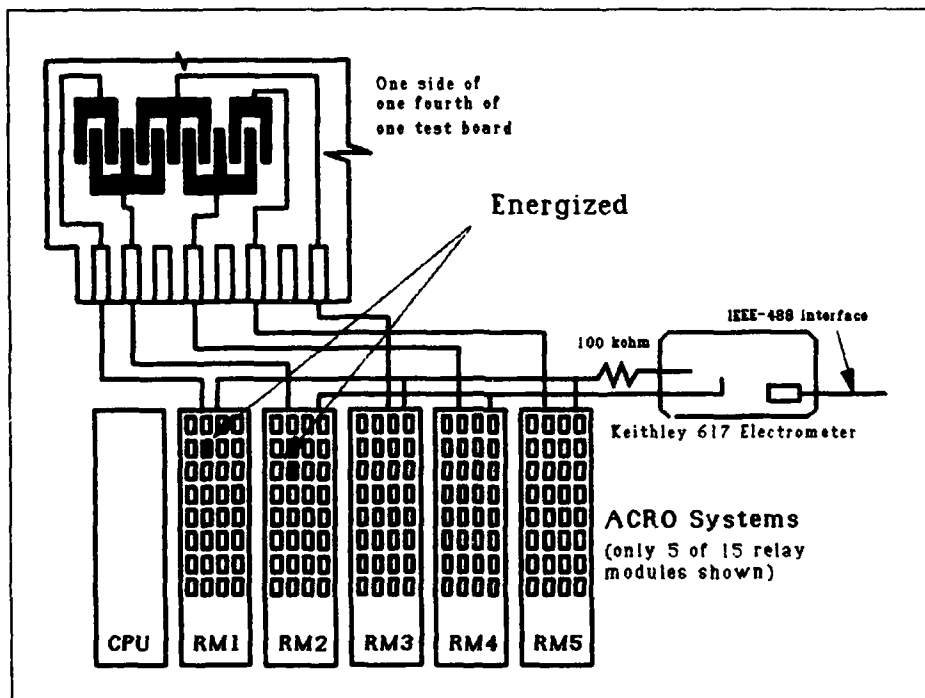


FIGURE 6. Partial Schematic of Measuring Circuit.

Figure 6 shows 5 of the 15 relay modules. The 2 relays that are indicated as energized show how we have kept the connections from the two comb patterns separated. As an example, "A" terminals from the 8 patterns on a board and from the 4 boards on a subpanel (32 total points) go to one relay module. This is repeated for "B", "C", "D" and "E" comb patterns, thus using all relays in 5 relay modules. This is repeated for the other two subpanels.

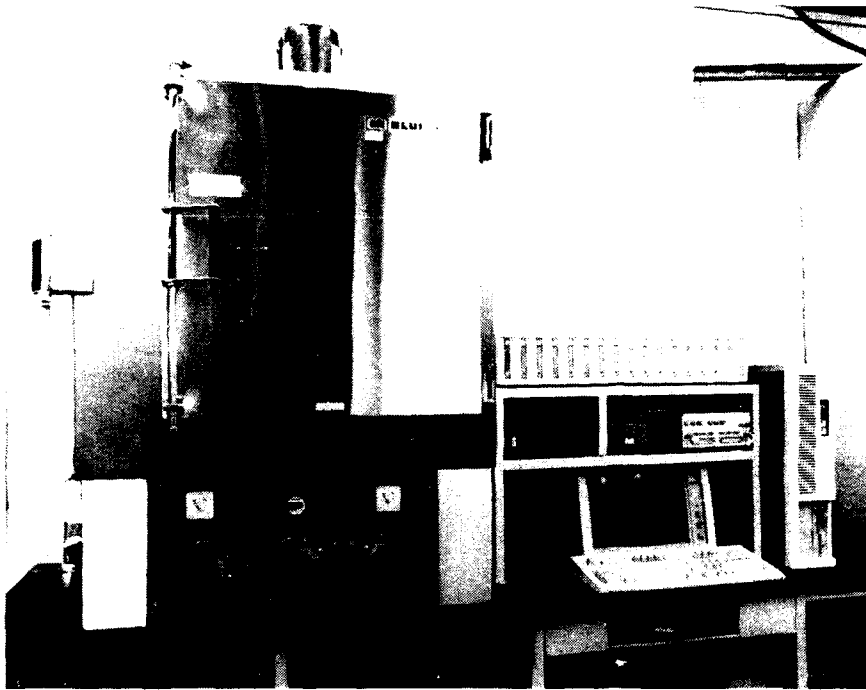


FIGURE 7. Total system

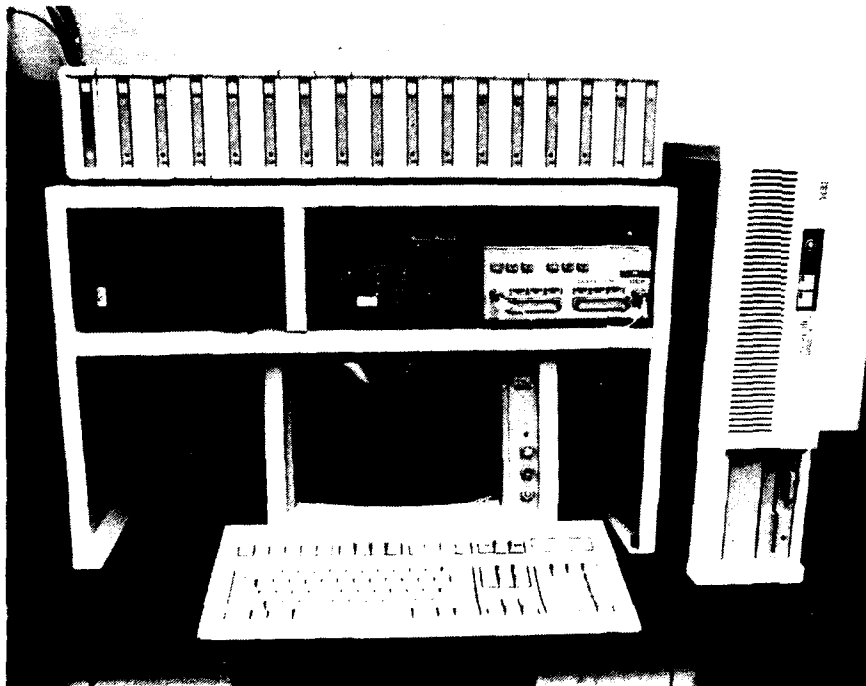


FIGURE 8. Measurement System

Test board: The test board was redesigned to have four (4) separate resistance comb patterns on each side. This give us 16 test points per side, 32 per board or 64 per site each week. We also rotated the patterns 90° so that the circuit traces from the pattern to the edge connectors would not significantly alter the number of squares. Solder mask is applied in a striped pattern (not shown) across conductor pattern in accordance with the BELLCORE requirements. (The current pattern is shown in Figure 9.)

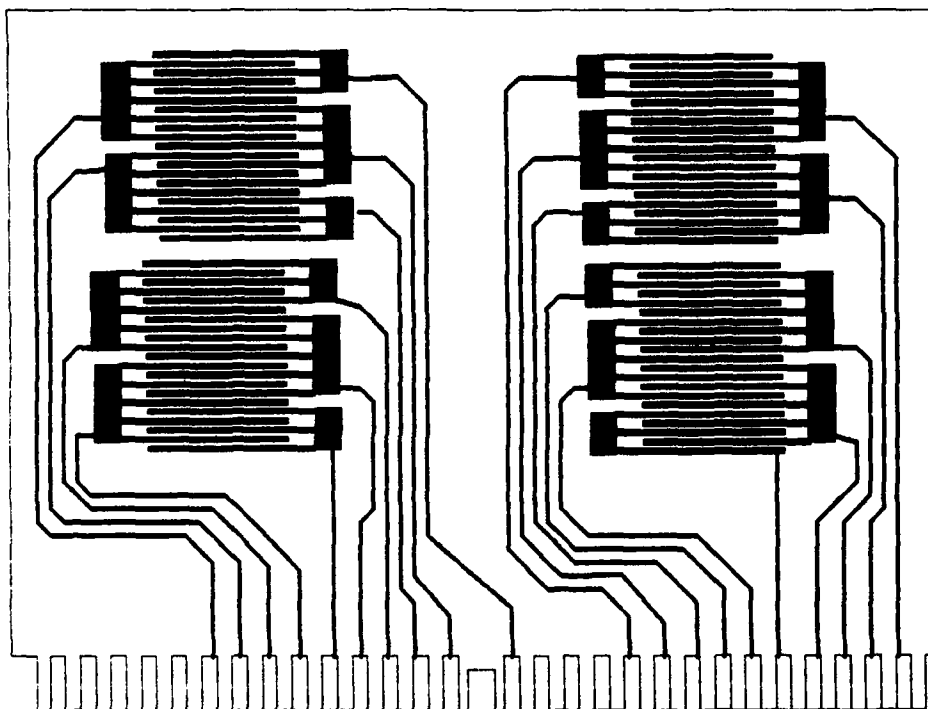


FIGURE 9. Current Configuration of Test Board.

Problems with the test boards are still with us. As I stated in the introduction we do not make boards, we buy them from any of several suppliers. Also recall that we desire a board that tests at 100 gigohms to monitor our process. Only one of our suppliers has been able to furnish boards suitable for use without additional cleaning. To clean boards we have tried isopropyl alcohol, TMS, vapor degreasing, a high pressure car wash spray with detergents and several other materials without significant results.

After hearing a paper at China Lake last year on the synthetic fusing fluid process (Ref. 3), I tried to locate a vendor that used the process but struck out. It seems that, because of potentially tighter restrictions on the use of solvents by the EPA, processes are tending toward the aqueous rather than toward the solvents.

The graph in Figure 10 shows the SIR values of boards as received from three of our suppliers. Note that even those from Supplier A are not completely above the 100 gigaohm minimum for all patterns.

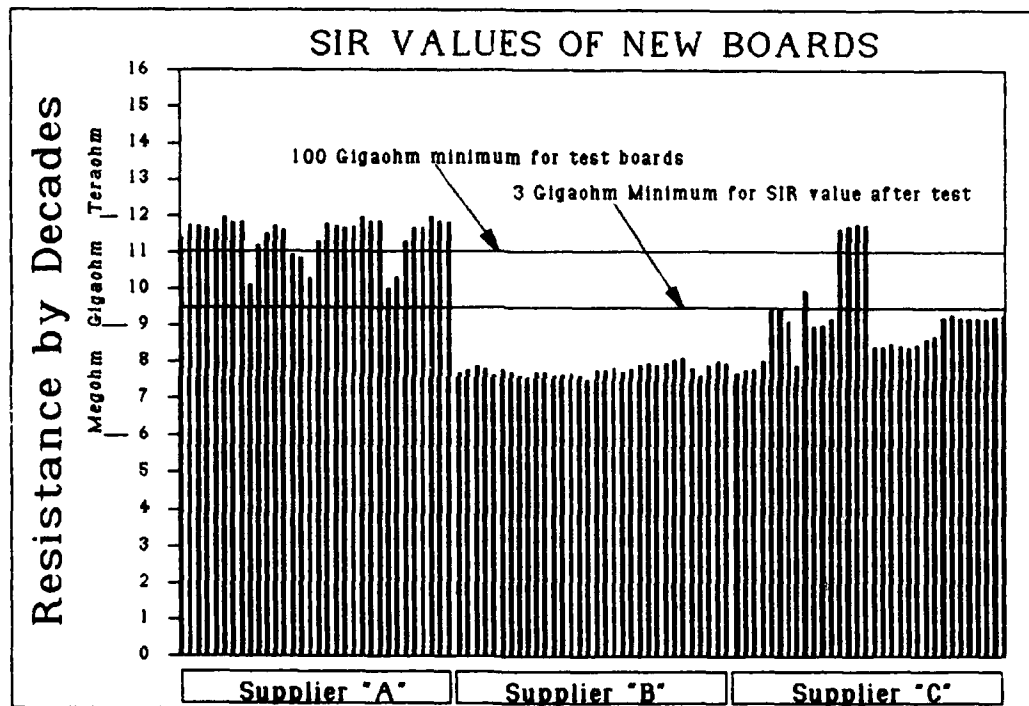


FIGURE 10. Comparative Values on New Boards.

Backplane: The backplane (Figure 11) was redesigned to be a stainless steel plate with space for 3 sub panels. 56 pin connectors were fastened to the stainless steel panel with screws at the ends only. Relief cutouts behind the connectors insured that there were no parallel paths for leakage other than on the bare connector.

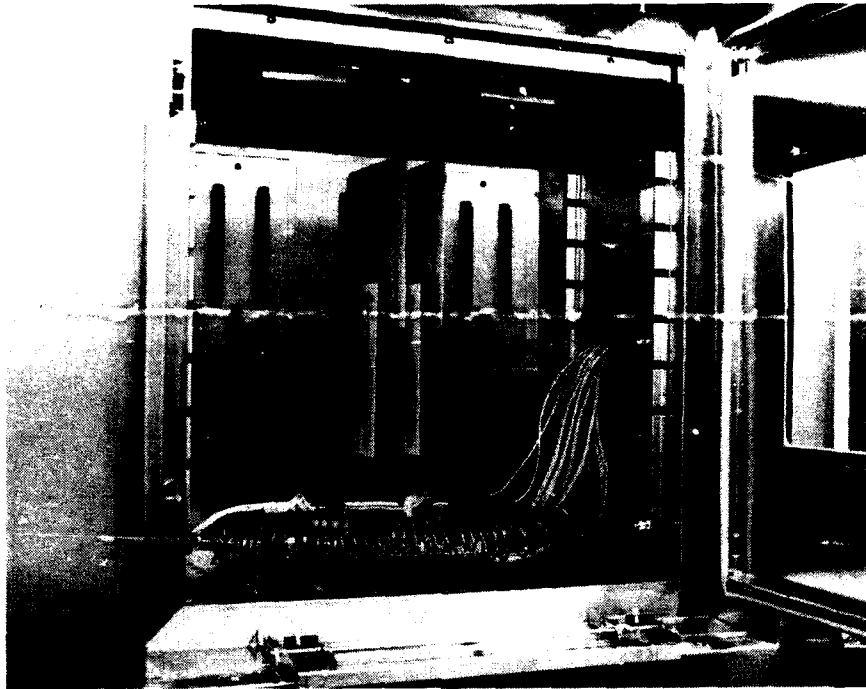


FIGURE 11. Backplane with Test Boards.

There was significant concern that connectors are not satisfactory in this application and that all test leads must be soldered to the board. Why? Admitting that contacts have series resistance it is not significant as the values of the boards under test are in the mega- and giga- ohm ranges. Conversely, since the purpose of the SIR test is to measure the cleanliness of the board, why take a chance of contamination because of additional handling and application of flux to the board.

Program and computer: When the project EE found that we would be dealing with 480 separate relay contacts, 384 measurements and much data manipulation, he realized that we had run out of computing power with the HP 85. He turned to the IBM/AT with Lotus/123 and the Lotus/Measure overlay program. This has worked out well. While it took a lot of time programming the system, most of the effort was spent writing macros that made the program user friendly and totally automated.

FUTURE EFFORT

I am not sure what we would do differently if we had only one unit to make again. If things proceed as they are, and we have to qualify solder masks, inner layers and new suppliers we will have to expand the system. By adding another data acquisition CPU, wiring harness, relay modules and backplane, we could effectively double the size of the system and still use the existing chamber and computer. Our current system would require about \$50,000 to duplicate.

At least one supplier is marketing a stand alone SIR system. With its dedicated firmware computer, specially designed relay banks and internal electrometer, costs should be less than our approach. However, this commercial system will only handle 2 boards of 8 patterns each vs. the 12 we can run.

There has been some discussion about applying 100 volts to the patterns at all times except during the actual measurement. We can do this as we employ form "C" relays; but no decision has been made on this requirement.

We plan to expand the testing to evaluate solder masks, inner layer cleanliness, alternate cleaners and fluxes in the wave solder processes. We are also unsure of the side effect of antistatic agents used in bags, so this evaluation has been added to the agenda.

REFERENCES

- 1). "SURFACE INSULATION RESISTANCE-PART I: THE DEVELOPMENT OF AN AUTOMATED SIR MEASUREMENT TECHNIQUE" by Emery J. Gorondy, E. I. DuPont, Presented at IPC Fall Meeting, September 1984, San Francisco, Ca.
- 2). "SURFACE INSULATION RESISTANCE-PART II: EXPLORING THE CORRELATION BETWEEN STANDARD INDUSTRY AND MILITARY "SIR" TEST PATTERNS-A STATUS REPORT" by Emery J. Gorondy, E. I. DuPont, Presented at IPC 28th Annual Meeting, April, 1985, New Orleans, La.
- 3). "SYNTHETIC ACTIVATED (SA) FUSING FLUIDS AND FLUOROCARBON/ALCOHOL AZEOTROPE CLEANING: THE KEY TO UPGRADED SURFACE INSULATION RESISTANCE AND ENHANCED PRINTED WIRING BOARD RELIABILITY" by Dr. W. G. Kenyon & D. A. Emig, Freon Products Laboratory, E. I. DuPont de Nemours & Company, Inc., Presented at 11th Annual Electronics Manufacturing Seminar, Naval Weapons Center, China Lake, California. 1987

APPENDIX A

Equipment list and comments

Temperature-humidity chamber: BlueM-Humid-flow, Model AC-7502HA-1
As we are using a more sensitive wet bulb/dry bulb thermometer (HP 2804A) we do not use the circular chart recorder supplied. It does not have sufficient resolution to monitor the chamber in the required 90% RH range. The temperature controls are saturable reactors and have no feedback. Because of this we must adjust the temperature, check the HP thermometer, turn the knobs, etc., until proper operating conditions are established. I would recommend some type of closed loop temperature controller.

The chamber is controlled by two heaters, one for air and one for water. To raise humidity the water temperature is raised. To reduce the humidity and supply a "load" on the system the back panel is air cooled with room air. Since we are in an air conditioned environment this works fine. Higher room temperature would require a chamber with a refrigeration system for maintaining a load and condensing excess moisture.

The chamber also had a DI water reservoir and an ion exchange cartridge. Since we have plant DI water we took the chamber out and kept the cartridge as a polisher. (One note, BlueM had the DI cartridge installed so water flowed up through the ion exchange bed, I felt this was wrong and reconnected the system to have water flow down through the cartridge. It makes more sense to me to keep the resin bed compacted.) With this change we consistently get 5 megohm water. Of course, all wettable surfaces must be 300 series corrosion resistant steel.

Backplane and wiring harness: (Figure 11)

Fabricated in house:

- Back plane connector is Viking 2VH28/1AV5
- Wire: 7 strand, 27 gage, Teflon insulated
- Solder for wire to female board edge connector is Alpha WRMA, later cleaned in TMS
- Shielding, 1/4 inch ID braided tin over copper
- Connector to relay module is a standard ribbon cable connector
- Backplane panel and subpanels are of 304 corrosion resistant steel

Relay modules: ACRO Systems:

- 1 ea. 992 CPU (central processor unit) with IEEE-488 interface
- 1 ea. 901 Power supply
- 15 ea. 915 Switching module

Electrometer: Keithley 617, Programmable electrometer.

This is essential. With a standard megohmmeter we would still be in the manual mode. The 617 is fully programmable via IEEE-488 and transfers the data back to the computer via the bus.

Controller (computer): IBM/PS2-30 with a National IB-488 board.

Almost any compatible computer with 640K of RAM should handle the process. Of course the hard disk will make the whole operation much easier.

Software: Lotus/123 and Lotus/Measure.

A program could also be written in Basic or any of several other languages.

Thermometer: (optional) HP 2804 Quartz thermometer.

We could have used something different except we happened to have this unit on hand. One option would be to use a thermometer module for the ACRO System and operate it through the ACRO CPU. This would have required another CPU and power supply as 15 is the maximum modules addressable by the ACRO CPU.

Water conductivity instrument: (optional) Keithley 580 Micro-ohmmeter.

Conductivity is normally measured with an AC Wheatstone bridge. The AC is essential so that the conductivity cell electrodes will not polarize. The Keithley has an alternating polarity pulse mode that simulated the AC. With this we can track the conductivity of the water leaving the chamber. While it is necessary to feed clean water into the system it is also necessary to know how clean the water is in the boiling sump. By monitoring the drain water you can be assured the inlet water is clean and there is sufficient flow so that contaminants do not build up in the boiling sump.

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APPENDIX B

SURFACE INSULATION RESISTANCE TEST									
Material Evaluation Laboratory - ROCKWELL INTERNATIONAL									
Timer :		102:37		Temp. :		35.18 degC			
RH :		89.22 %		Water :		1.882 Mohm			
=====									
Test : After 96				s : SIR<30			12/6/87		
=====									
X1NO-07	1	2	3	4	1	2	3	4	
A1,A2	2.3G*	3.5G	129.3M*	218.1M*	237.6M*	4.3T	7.7T	7.5T	
A3,A4	495.5M*	460.9M*	2.6G*	2.8G*	739.8M*	364.4M*	1.5G*	410.0M*	
B1,B2	8.8G	8.3G	10.2G	9.7G	2.3G*	4.0T	6.0T	197.6G	
B3,B4	4.3G	7.0G	21.7G	44.7G	62.7G	230.1G	314.5G	186.6G	
2NO1-07	1	2	3	4	1	2	3	4	
A1,A2	701.8M*	316.7M*	362.1M*	642.8M*	272.7M*	371.6M*	381.8M*	543.6M*	
A3,A4	452.3M*	634.6M*	613.9M*	964.9M*	914.8M*	785.6M*	841.2M*	916.3M*	
B1,B2	23.1G	33.8G	4.5G	3.2G	2.8G*	3.8G	35.3G	48.9G	
B3,B4	1.3T	2.3T	2.0T	1.8T	150.0G	172.6G	32.8G	38.9G	
2NO2-07	1	2	3	4	1	2	3	4	
A1,A2	2.0G*	27.7G	4.0G	4.4G	534.3M*	2.8G*	290.4G	15.6G	
A3,A4	6.8G	10.3G	7.9G	5.5G	4.9G	2.5G*	6.2G	6.1G	
B1,B2	78.1G	77.3G	53.9G	1.1T	1.0T	612.1G	952.2G	1.1T	
B3,B4	374.0G	867.1G	770.7G	862.1G	1.5T	1.6T	1.7T	417.1G	
X1NO-09	1	2	3	4	1	2	3	4	
A1,A2	11.9G	13.4G	13.7G	21.0G	9.7G	2.0T	3.6T	4.1T	
A3,A4	2.6T	5.3T	5.1T	1.9T	2.5T	4.3T	4.4T	4.1T	
B1,B2	17.8G	7.2G	2.3G*	968.8M*	1.6G*	3.2T	4.9T	4.6T	
B3,B4	4.9T	6.1T	6.2T	4.0T	4.3T	3.9T	3.9T	5.5T	
X1NO-09	1	2	3	4	1	2	3	4	
A1,A2	1.5G*	10.3G	4.6G	2.5G*	1.6G*	3.8T	5.8T	5.9T	
A3,A4	5.6T	6.8T	6.9T	6.7T	6.8T	6.8T	7.1T	7.0T	
B1,B2	229.9G	508.4G	835.2G	1.1T	18*.5G	3.0T	4.4T	6.6T	
B3,B4	6.9T	7.1T	7.2T	7.1T	7.2T	7.5T	7.7T	7.6T	
X1NO-09	1	2	3	4	1	2	3	4	
A1,A2	1.2G*	1.4G*	508.2M*	411.7M*	173.9M*	216.1M*	302.9M*	202.5M*	
A3,A4	323.5M*	796.8M*	671.5M*	1.0G*	1.1G*	573.4M*	1.3G*	309.4M*	
B1,B2	61.5G	216.1G	678.9G	615.0G	272.4G	395.7G	2.1G*	2.5G*	
B3,B4	5.1G	59.0G	88.5G	93.7G	80.0G	127.9G	18.7G	3G.2G	
X1NO-09	1	2	3	4	1	2	3	4	
A1,A2	40.3M*	74.8M*	104.3M*	84.0M*	62.9M*	92.8M*	330.9M*	325.5M*	
A3,A4	46.7M*	87.7M*	38.0M*	52.7M*	10.8M*	163.2M*	827.2M*	1.3G*	
B1,B2	15.1G	116.4G	85.7G	45.6G	35.9G	36.0G	37.9G	62.8G	
B3,B4	32.7G	40.3G	21.3G	22.7G	5.9G	46.2G	70.8G	12.4G	
X2NO-09	1	2	3	4	1	2	3	4	
A1,A2	37.3G	39.1G	17.6G	40.0G	3.1G	12.1G	26.8G	21.9G	
A3,A4	9.7G	10.4G	30.8G	24.1G	2.6G*	42.6G	50.6G	46.2G	
B1,B2	1.2T	1.3T	1.5T	1.5T	148.1G	159.9G	407.5G	493.4G	
B3,B4	5.6G	4.4G	185.4G	772.0G	1.4T	1.6T	1.6T	864.1G	
X2NO-09	1	2	3	4	1	2	3	4	
A1,A2	511.7M*	24.8G	11.4G	7.1G	372.9M*	2.3G*	3.4G	453.9M*	
A3,A4	2.1G*	2.5G*	560.1M*	971.8M*	28.0G	37.8G	22.5G	2.7G*	
B1,B2	719.4G	991.2G	1.0T	1.2T	400.4M*	5.3G	276.3G	32.8G	
B3,B4	31.2G	45.9G	78.1G	540.6G	20.3G	37.3G	53.9G	62.5G	
XATT-01	1	2	3	4	1	2	3	4	
A1,A2	3.2T	3.4T	3.9T	4.0T	2.9T	3.0T	2.9T	2.9T	
A3,A4	3.2T	3.5T	3.7T	3.1T	4.3T	4.5T	4.8T	4.4T	
B1,B2	4.8T	5.0T	5.2T	5.0T	5.0T	5.1T	5.4T	5.1T	
B3,B4	4.9T	5.2T	5.4T	5.0T	5.2T	5.5T	5.8T	5.7T	
XATT-02	1	2	3	4	1	2	3	4	
A1,A2	4.5T	5.7T	4.8T	5.1T	2.7T	4.7T	5.0T	5.1T	
A3,A4	4.8T	4.8T	4.8T	4.3T	3.6T	4.2T	4.3T	3.8T	
B1,B2	5.2T	5.6T	5.9T	5.3T	4.9T	5.4T	5.5T	5.4T	
B3,B4	4.4T	5.3T	5.4T	4.9T	5.2T	5.6T	5.8T	5.2T	
XATT-03	1	2	3	4	1	2	3	4	
A1,A2	3.3T	4.8T	5.2T	4.3T	4.5T	4.7T	4.9T	4.7T	
A3,A4	4.5T	4.9T	4.9T	4.3T	4.5T	4.9T	5.0T	4.8T	
B1,B2	4.8T	5.2T	5.4T	4.2T	3.2T	5.1T	5.5T	5.5T	
B3,B4	4.2T	5.3T	5.5T	5.1T	4.9T	5.3T	5.7T	5.2T	

* = values below minimum, "T" = Tera-, "G" = Giga-, "M" = Meg-

FIGURE B1. SIR Test Results for One Run.

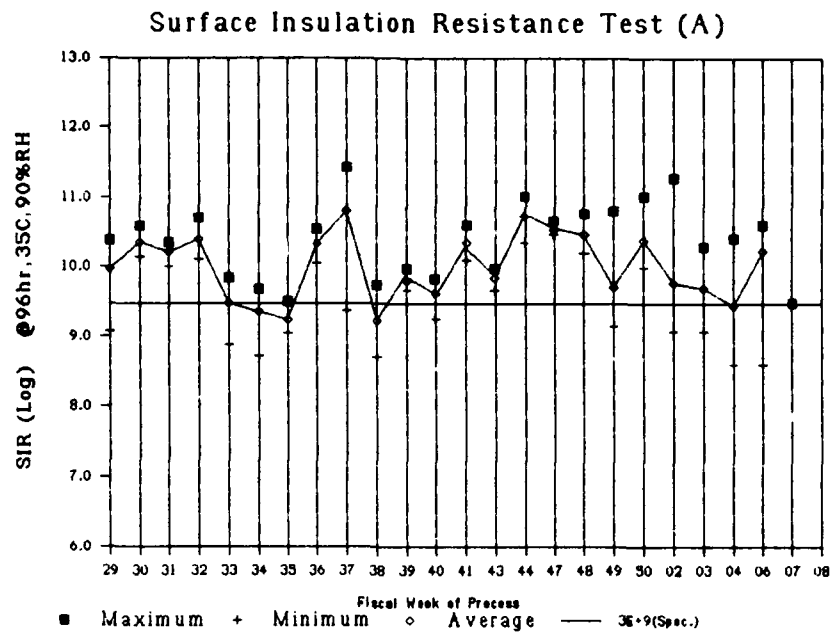


FIGURE B2. Graph of Surface Insulation Resistance Test Results.

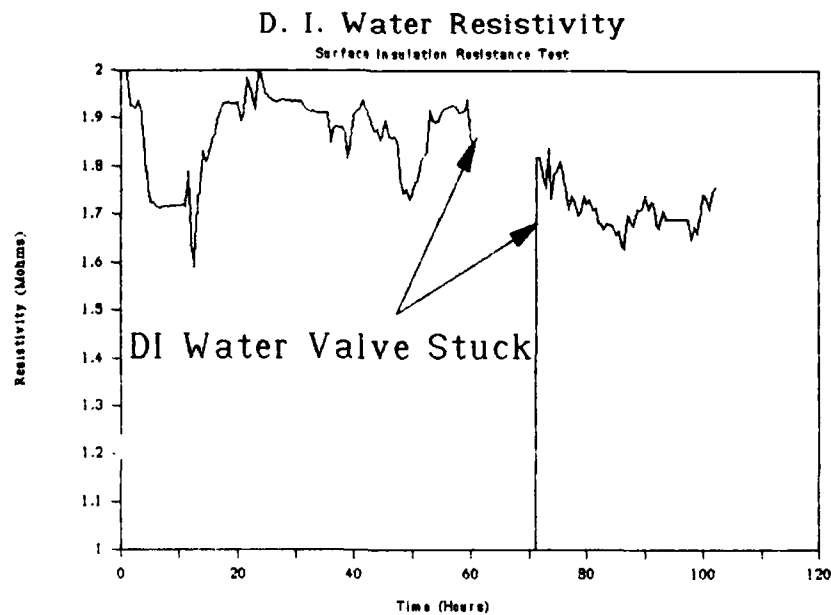


FIGURE E3. D. I. Water Resistivity for One Run.

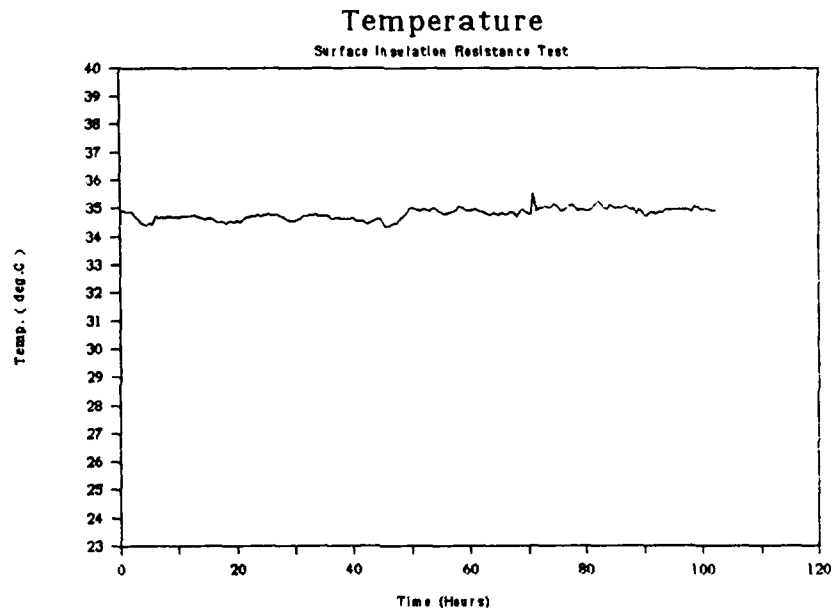


FIGURE B4. Temperature Plot for One Run.

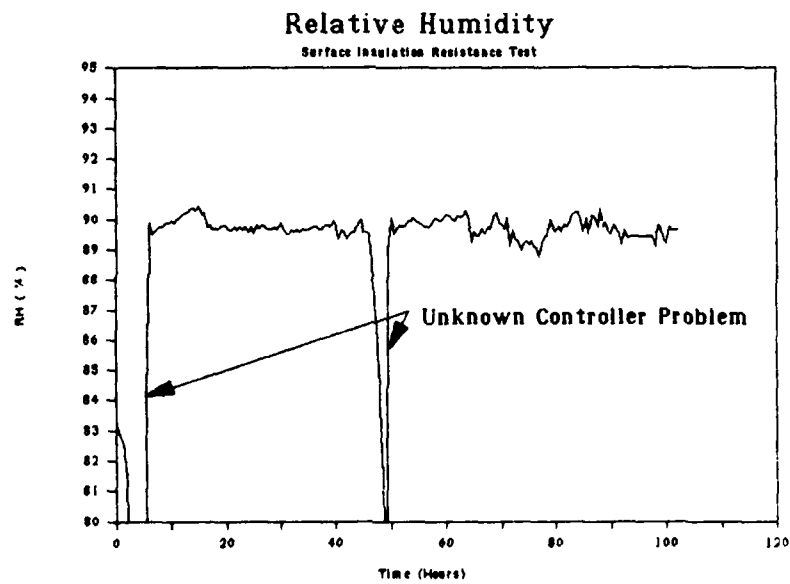


FIGURE B5. Relative Humidity Plot for One Run.

ACKNOWLEDGEMENT:

I would like to thank all of the people who helped put this project together.

Gene Kuntz, Quality Engineer, coordinated the requirements with BELLCORE and did the legwork on getting the artwork for the board made.

Norm Barth, Engineering Technician, was curious about the interaction of the various pieces of the puzzle. He characterized and built the system. Norm is now the system operator and is responsible for checking new boards and running the SIR test on completed test boards.

Weifan Lin, Technical Staff Member EE, handled the electrical measuring system and wrote the Lotus/123/Measure program.

Cheri Neal, MEL Assistant, cleaned many boards in an effort to get suitable test coupons for the various sites.

Debra Cummins, Engineering Technician, did manual testing on Saturdays and Sundays in the days before automation. She has also reviewed this paper and made valuable comments on its organization and content.

And of course the several levels of Management who supported the effort with approvals for capital equipment and time to build the system.

NWC TP 6896
EMPF TP 0003

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**STRATOSPHERIC OZONE: FEDERAL REGULATIONS AND
THE USE OF CHLOROFLUOROCARBONS IN THE ELECTRONICS INDUSTRY**

by

Dr. Stephen Andersen
Senior Economist
U.S. Environmental Protection Agency
Washington D.C.

ABSTRACT

The stratospheric ozone layer shields the earth from harmful ultraviolet radiation that can adversely affect public health and the environment. Rising concentrations of chlorofluorocarbons (CFCs) and Halons have the potential to deplete this layer allowing increased levels of this biologically damaging radiation to reach the earth's surface. This could lead to increases in the incidence of skin cancer and cataracts, substantial crop and aquatic losses, and could contribute to the greenhouse effect. To protect against this threat the United States recently joined numerous other nations in signing the Montreal Protocol that will reduce CFC and halon use worldwide. In addition, the Environmental Protection Agency recently announced proposed domestic regulations designed to adhere to the requirements of the Montreal Protocol. Specifically, the domestic regulations and the Montreal Protocol call for a freeze on CFC use at 1986 levels, followed by a 20 percent reduction in CFC production from 1986 levels by mid 1993, followed by another 30 percent reduction from 1986 production levels by mid-1998. Besides offering environmental benefits, these regulations also provide potentially significant business opportunities for firms in the electronics industry. These regulations will increase the price and reduce the availability of CFC-113 thereby increasing the competitiveness and the size of the market available to substitute products. In addition, major consumers of products previously manufactured with CFCs may become more amenable, if not demand, products manufactured without CFCs. For instance, EPA is currently discussing with the Department of Defense the possibility of having it change its specification for printed circuit boards to encourage the use of non-CFC cleaning methods. Given the regulatory emphasis on the reduction of CFC use nationwide firms may find it advantageous to explore alternative non-CFC cleaning processes.

**Stratospheric Ozone:
Federal Regulations and the Use of Chlorofluorocarbons
in the Electronics Industry**

**By
Dr. Stephen Andersen,
Senior Economist**

**Office of Air and Radiation
U.S. Environmental Protection Agency**

Stratospheric Ozone: Environmental Risk and Regulatory Response

Outline

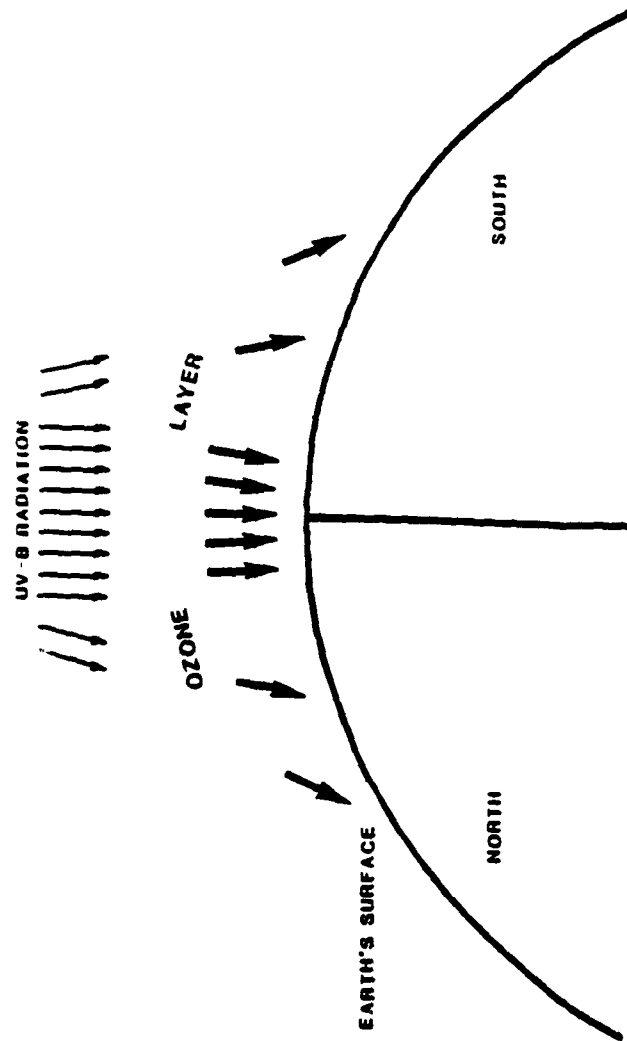
Risks Posed by Depletion of the Ozone Layer

Regulatory Response and the Montreal Protocol

Domestic Response Based on Intensive Research and Analysis Conducted Over Last Three Years.

International Response Marked by High Degree of Cooperation -- Consummated with Recently Signed Montreal Protocol that Limits Production of CFCs Worldwide.

THE OZONE LAYER PROVIDES PROTECTION FROM UV-B



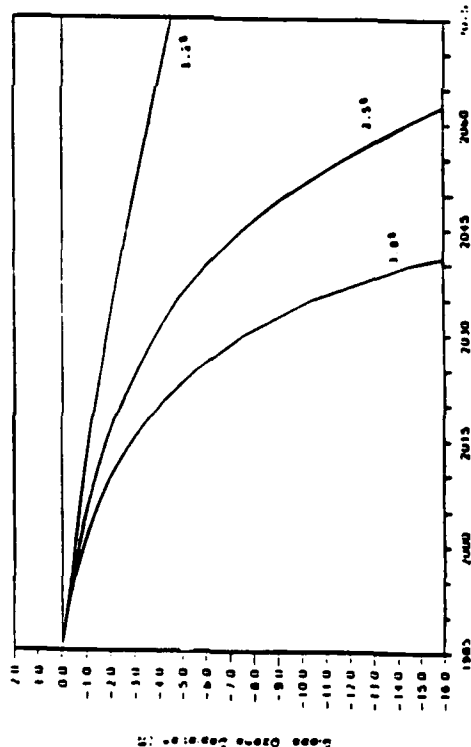
CAPTION: OZONE NATURALLY OCCURS IN THE STRATOSPHERE. SCREENING OUT SO'E OF THE UV-B RADIATION RECEIVED FROM THE SUN. THE OZONE LAYER ALLOWS MORE UV-B TO REACH THE EARTH'S SURFACE THE CLOSER ONE GETS TO THE EQUATOR.

PROBABLE EFFECTS

- Basal cell skin cancer
- Squamous cell skin cancer
- Melanoma skin cancer
- Immune suppression
- Materials degradation
- Tropospheric oxidants
- Global warming
- Crops
- Natural ecosystems
- Aquatic organisms

Analysis Of Risks: Ozone Depletion Effects

Assuming Recent Trends In Trace Gas Emissions Continues, Current Models Predict⁽¹⁾:



ASSUMPTIONS:

CFCs: 2.5% annual growth through 2050; constant thereafter

Methane: 0.017 ppm increase in concentrations

Nitrous Oxide: 0.2% annual growth in concentrations

Carbon Dioxide: NAS 50th percentile (about 0.5% growth)

(1) Based on 1-D models. Analyses by 2-D models suggest that depletion and related effects would be greater for populations above 30 to 40 degrees and less for those near the equator.

Summary Of Effects From Depletion: U.S. Only

SKIN CANCER:

60 Million Cases 1 Million Deaths (For People Alive Now Or Born By 2075)

CROP LOSS:

Likely To Be Substantial

AQUATIC LOSS:

Likely To Be Substantial

CATARACTS:

Increase In Cases

GROUND-LEVEL OZONE:

Increased Background Levels

Analysis Of Risks: Climate Related Effects

CFCs And Changes In Ozone Could Be Responsible For 10-30 Percent Greenhouse Forcing (Depending On Relative Growth Rates). Other Gases - Which Buffer Ozone Losses - Also Add To The Greenhouse Effect.

Possible Effects

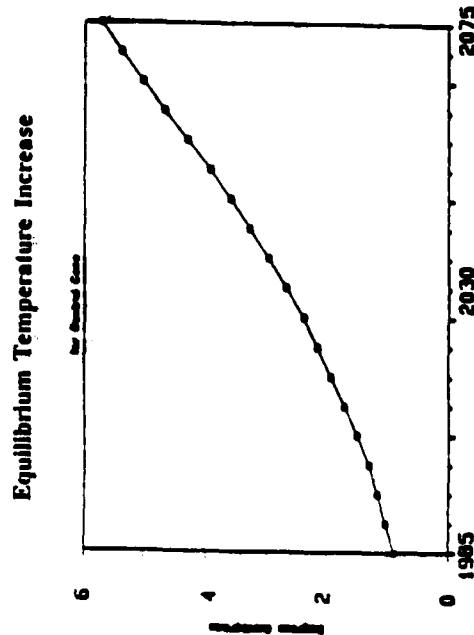
SEA LEVEL RISE:
55 To 190 CM (By 2075)

LOSS IN WETLANDS:
Substantial In U.S. Based On Case Study

DAMAGE FROM COASTAL FLOODING:
Case Studies Support Substantial Losses

EFFECTS ON AGRICULTURE:
Increases Due To Higher CO₂
Possible Losses Due To Shifts In Precipitation

EFFECTS ON WATER RESOURCES:
Shifts Likely But Can't Yet Estimate



Stratospheric Ozone: Regulatory Response

**Domestic Response Based on Intensive Research and Analysis
Conducted Over Last Three Years.**

**International Response Marked by High Degree of Cooperation --
Consummated with Recently Signed Montreal Protocol that Limits
Production of CFCs Worldwide.**

CLEAN AIR ACT, SECTION 157B

“ . . . The administrator shall propose regulations for the control of any substance, practice, process, or activity (or any combination thereof) which in his judgment may reasonably be anticipated to affect the stratosphere, especially ozone in the stratosphere, if such effect in the stratosphere may reasonably be anticipated to endanger public health or welfare.”

Goal: Develop Workable Regulation

- **Ensure Environmental Protection**
- **Minimize Administrative Burdens**
- **Build on Current Producer/User Behavior**
- **Provide Incentives for Innovation/Chemical Substitutes**
- **Minimize Legal Uncertainty**
- **Provide for Lowest Cost Reductions**
- **Allow for Monitoring Compliance and Enforcement**

Montreal Protocol

Terms Of Agreement

Group 1: Cfc-11, -12, -113, -115

- Freeze at 1986 Production Levels Seven Months After Entry Into Force*
- 20% Reduction Starting July 1993
- Additional 30% Reduction Starting July 1998

Group 2: Halon - 1211, -1301, -2402

- Freeze at 1986 Production Levels Thirty-seven Months After Entry Into Force**

* Entry into force January 1989 provided 11 ratifications representing two-thirds of 1986 global consumption.

Proposed Federal Regulations

Regulatory Requirements

- Immediate Freeze on CFC Production and Consumption at 1986 Levels
- Reduction of CFC Production and Consumption to 80 Percent of 1986 Levels by Mid-1993
- Reduction of CFC Production and Consumption to 50 Percent of 1986 Levels by Mid-1998.

Regulatory Options Under Consideration

- Production Quotas
- Production Quotas/Regulatory Fee Hybrid

Upcoming Key Dates

Domestic Timetable

Proposed Regulations Announced on December 1

- February 7, 1988 --- End of Comment Period on Proposed Regulations
- August 1, 1988 --- Final Decision

OVERVIEW OF CFC USE IN THE ELECTRONICS INDUSTRY

CFC-113 USED AS A SOLVENT IN THE ELECTRONICS INDUSTRY
OTHER CFCs USED IN A LIMITED WAY, IF AT ALL

MAJOR USES OF CFC-113 IN THE ELECTRONICS INDUSTRY

REMOVING SOLDER FLUX DURING PRINTED CIRCUIT BOARD ASSEMBLY
DEGREASING WAFERS AND PRINTED CIRCUIT BOARDS
CLEANING MEMORY SYSTEMS, GUIDANCE SYSTEMS, SURFACE MOUNTED
ASSEMBLIES, AND DISPLAY DEVICES

SOME QUESTION OF SHIFT IN USE PATTERN TOWARD MEMORY DEVICES

Implication of CFC Regulations on the Electronics Industry and Potential Business Opportunities

Price of CFC-113 Will Increase

**Availability of CFC-113 Will Decrease as Industry Competes for
Reduced Supply**

**Result --- Increased Interest and Research Into Non-CFC Alternatives
Due to Potentially Large Market**

Implication of CFC Regulations on the Electronics Industry and Potential Business Opportunities

Effect on Markets

Department of Defense

- EPA Discussing a Revision in Specifications with DOD to Encourage Non-CFC Cleaning Methods

Other Government Agencies

- May Revise Federal Purchasing Practices so that Government Buys Products Manufactured Without CFCs

Corporate Response

- Voluntary Shift Away From Products Manufactured Without CFCs Likely Such as Action by McDonalds Corporation

Implication of CFC Regulations on the Electronics Industry and Potential Business Opportunities (cont'd)

Effect on Markets

Consumer Response

- Heightened Consumer Awareness Leading to Reduced Acceptance of Products Processed With or Containing CFCs (Such as Occurred With Asbestos and Chlorinated Solvents).

More Stringent State Regulations Possible

Possible Change in International CFC Market Due to Implementation of the Montreal Protocol

Implication of CFC Regulations on the Electronics Industry and Potential Business Opportunities

These Changes Imply:

Cost Competitiveness of CFC-113 Substitutes Will Increase

**Markets Previously Closed Will Become More Receptive to CFC
Substitutes**

Implication Of CFC Regulations on the Electronics Industry and Potential Business Opportunities

This Regulation Therefore Implies:

**Tremendous Opportunity to Develop New Products and Processes
for Electronics Industry Uses**

**Control Technologies to Reduce and Recycle CFC-113 Use are
Available and Further Opportunities for Innovation Exist**

**Companies Already Have Substitute Products Available and Further
Research is Underway**

NWC TP 6896
EMPF TP 0003

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SURFACE MOUNT TECHNOLOGY

by

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"THE NEW FRONTIER"

In an effort to maximize the amount of "real estate" available on circuit boards, to increase functionality, and to eliminate many of the manufacturing problems associated with traditional thru-hole design, there is an ever increasing trend toward Surface Mount Technology. While this "new" technology holds a great deal of promise toward achieving these goals, it is vitally important that design and manufacturing techniques be optimized in order to build a readily producible, quality product. This paper will discuss these areas of concern.

THRU-HOLE PROBLEMS

The primary "trouble area" of thru-hole design technology is with the plated thru-hole itself. It is not uncommon to have less than desirable quality of hole drilling and copper plating in the hole, subsequently resulting in soldering problems.

If the holes are not drilled smoothly, a condition caused by using dull drills or improper speeds and feeds, the copper plating inside the hole will conform to these peaks and valleys in the laminate material, and not be smooth. This will result in a restriction of flux and solder flow through the board preventing proper solder capillarity to the top side.

This raggedness inside the hole can also cause variations in plating thickness, and areas of exposed laminate. These plating voids allow outgassing from the base laminate during the soldering process resulting in pin holes or blow holes in the solder connection.

A new advance in thru-hole technology is the multi-layer board. While this design does permit greater component density, it has caused a major soldering problem.

A common design practice with these boards is to locate internal ground planes within the multi-layer board. This extra

copper thickness adds a heat sinking effect and can cause a shut-off point for solder flow through the board. Solder quality is effected by this unequal copper load per hole, introducing uneven cooling of the solder resulting in solder surface quality problems. Some causes for this problem are: improper ground plane design, and insufficient heating from inadequate wave soldering machines or poor process control.

Also, multiple cooper inner layers cause a slower than normal cool down rate which results in grainy connections. This grainy appearance is the result of lead-rich dendrites protruding through the solder surface.

A properly designed and fabricated surface mount board should be a viable alternative and help to alleviate these problems.

DESIGN CONSIDERATIONS

In order to produce a reliable, high quality surface mount board, it must initially be designed properly. Items to consider are: component geometry (types) and component surface interface area in relationship to printed wiring board pad area. Along with this, the type of connection must also be evaulated. Typical of these are Butt or "I", Bottom Lead, Round End, Flat End, Castellatation, Gull Wing, "J", "C" and other connections.

Another factor effecting design considerations is that we are presently using a mix of technologies. Typical of these are: (1) Combination of standard thru-hole components and surface mounted components, (2) Thru-hole components modified to be surface mounted, and (3) All surface mounted components.

Manufacturing and soldering processes must be selected based upon the type of board being produced.

First of all, the pads should be designed large enough, regardless of component geometry, to allow for a visible solder fillet external to the component lead or metallized end surface (Figure 1). Provision must be made for the fillet to form in a concave configuration to assist in determining solder wetting.

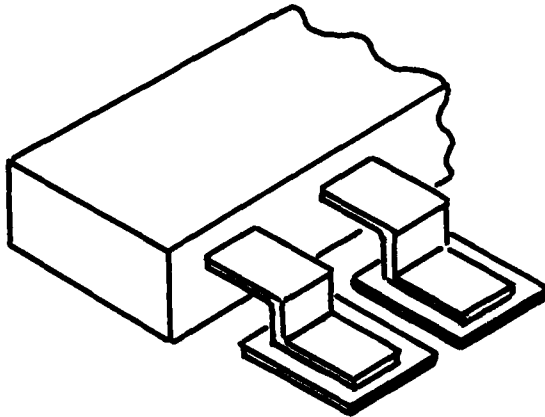


Figure 1

Without visible, external solder connections, visual inspection will not be possible. The alternative is automated inspection processes. While these methods are valid and can provide excellent results, high volume is required to justify their cost and use.

Proper pad sizing and spacing must be determined to provide the correct "footprint" for the component being mounted. Ideally, all of the component lead/end cap to be soldered will be located on the pad, with enough pad exposed around the periphery of the component lead/end cap to allow proper filleting as discussed above.

Pad-to-pad spacing must also be designed to permit adjacent leads or opposite end caps on a component to be located in the correct position on all pads without excessive overhang.

There must also be enough spacing from pad-to-pad and trace-to-trace to provide sufficient surface resistivity to prevent current leakage between adjacent circuitry.

COMPONENT PREPARATION

When preparing components have "C" lead, "J" lead, or Gull Wing terminations, lead forming is an important consideration. It is mandatory that all leads be the same length and formed to the same angles to permit all leads to be in contact with their associated pads, (Figure 2). If there are variations in these dimensions, some leads will be in contact with the pads while others aren't, thus affecting electrical considerations and connection strength.

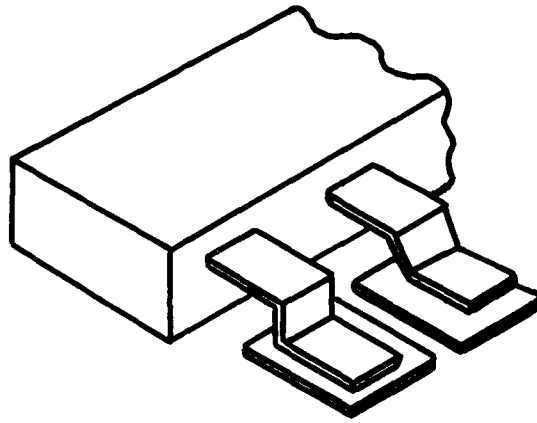


Figure 2

When using "I" or Butt lead terminations, if all leads are not cut to the same length, it is possible when using solder paste in an automated soldering process that solder may not fill the gap between the pads and the shorter leads resulting in questionable solder connections, (Figure 3)

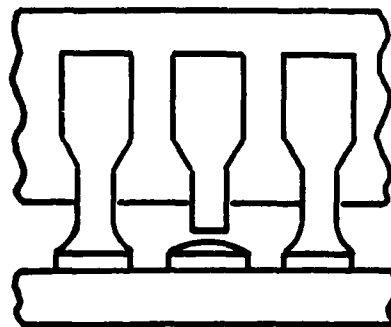


Figure 3

It is also critical with "I" Leads that the ends of the leads be cut square to the pad surface so the tips of the leads will rest flat on the pads.

MOUNTING CRITERIA

The following Mounting Criteria must be considered and specified in order to produce a product which will satisfy mechanical and electrical requirements. These are: component centering, relative positioning between the end or side of the component lead/end cap and the end or side of the pad, component overhang, and parallelism (tombstoning).

Ideally the component lead/end cap will be centered on the pad with an equal amount of pad exposed around all areas of the component to be soldered. As examples, with an SOIC, which has a "Gull Wing" termination, and an SOT-89 which has a "Bottom Lead" termination, with equal spacing around the three sides of the leads, the geometry of the solder fillets will be uniform around the periphery of the leads, (Figure 4).

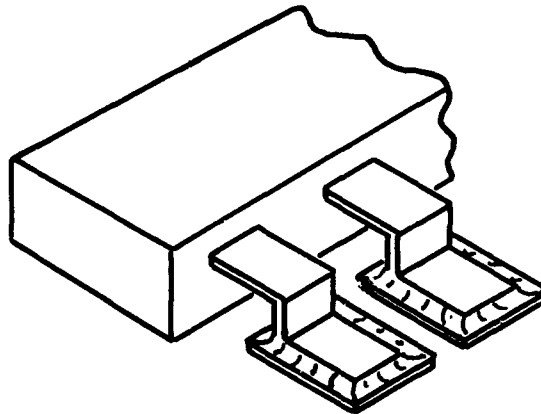


Figure 4

With Chip and Tantalum Capacitors having "Flat End" terminations, cylindrical Melf components, and LCC components having "Castellations", when the component is centered on the pad, ideally the distance from the end of the component end cap to the edge of the pad will be equal to the height of the area to be soldered. This should result in a totally uniform solder fillet, (Figure 5). Since side filleting is not critical on these components, side clearance is not a major concern.

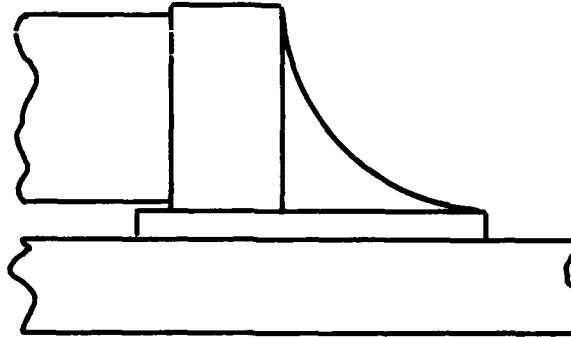


Figure 5

While it is preferred to have components and leads centered on the pads, with any manufacturing process some deviation from optimum is to be expected. As long as design limits are not exceeded, there should not be an excessive loss of quality. Following are some typical suggestions regarding maximum side overhang and minimum front edge clearance.

With components have "J", "C", or "Bottom" leads and with "Gull Wing" or "Flat End" terminations, it is permissible to have a maximum of 25% of lead/end cap side overhang without an appreciable loss of connection strength.

However, Tubular and Castellated components should not extend beyond the side edge of the pad.

Components having leads which extend outward from the component body such as "Gull Wing" and "Bottom Leads" may have the ends of those leads aligned flush with the front edge of the pad. Since there are two relatively long sides soldered to the pad, the connection on the front edge is not critical.

Non-leaded components such as Castellated, Melf, and Chip Capacitors must be mounted a required distance from the front edge of the pad. Distances specified by various requirements arbitrarily vary from .015" to .025". Since the front face of the end cap is the primary connection area, surface area and connection area height should be considered when determining this distance.

The leads of components have "I" type terminations must remain over the pad with a minimum of .010" side and front edge clearance. Since the contact area between the lead and pad is so small, there must be a solder fillet around the entire periphery of the lead.

SOLDER QUALITY AND QUANTITY

A generally accepted definition of Preferred Solder throughout the industry for years has been, "The solder connection should be smooth, bright and shiny, having a concave fillet which flows to a thin feather edge, and the outline of the lead must be discernible beneath the solder.

We have associated smooth, bright, and shiny with proper heating of the solder. A concave fillet with a feather edge denotes proper wetting and a discernible outline permits inspectability. A changing Packaging Technology does not alter the validity of this definition.

When leads are used on Surface Mounted Devices (SMD's), they must still be discernible! Concavity and feathering of the solder still indicate good wetting! While some standards allow convex fillets on Castellated components, how do you explain to production operators and inspectors that this condition is acceptable for one component but rejectable for all others?

One area where differences can be expected is in the surface appearance of the finished solder connections on SMD's. Since some of the soldering processes maintain the solder in a molten state for long periods of time, a granular appearance of the solder can be expected.

What is the proper solder quantity? Using a Chip Capacitor as an example, some companies assembling SMD's allow a maximum solder fillet height of 30% of the component end cap height while others use 50%, and some require 100% coverage, (Figure 6). Who is correct and why?

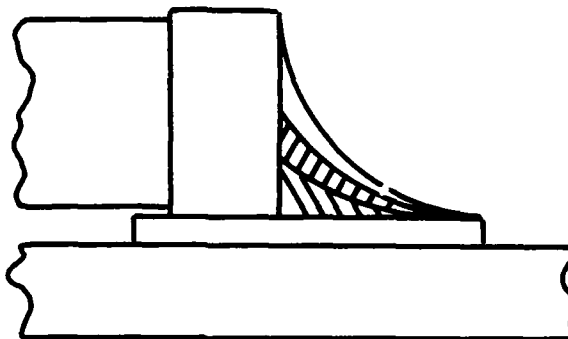


Figure 6

Standards and testing procedures must be developed and approved Industry wide so all manufacturers are using the same "yardstick".

SOLDERING TECHNIQUES

There are many techniques being used for the soldering of SMD's. Typical of these are: Hand Soldering, Wave Soldering, Infra-Red, and Vapor Phase Soldering. Each of these techniques offer benefits and disadvantages which must be thoroughly understood before selecting the method to be used.

Hand Soldering has the advantage of low equipment cost. Since any company performing electronic assembly already has soldering stations in-house, it may only require special tips to adapt those tools for soldering surface mounted components. However, whenever hand soldering is performed, there are many variables in the soldering process. Since SMD's are generally smaller and their alignment more critical than thru-hole components, the soldering process becomes very difficult. Hand soldering is recommended only when the cost of mass soldering equipment cannot be justified.

Wave Soldering has several advantages. It is a mass soldering process which increases productivity and reduces the cost per connection. With proper process control, the solder quality acceptance rate should be maintained at a reasonable level. Also, most companies already have a wave solder machine, so additional equipment will not have to be purchased. However, as component density increases, the solder wave may need to be agitated to eliminate the air pockets which may form in those restricted areas.

Wave soldering also has several disadvantages. Since the components must be on the bottom side of the board during the wave soldering process, they must be epoxied into place. This extra step increases the cost per connection and also reduces the ability to replace components. Another problem is that the liquid fluxes used for oxide removal may be driven beneath the component bodies and be extremely difficult to remove after soldering.

Infra-red soldering machines can be either in-line or batch type. They offer the advantage of being able to provide and precisely control the different temperatures required by the process. Solder paste is used for this process. The machine can be programmed to provide the proper heat to first bake and cure the paste and drive off the volatiles, then with increased heat, activate the flux, and then increase to solder melt temperature.

Since many factors such as component size, density and color effect heat absorption, temperature profiles for each different board must be established and carefully maintained when using this process.

Vapor phase is another mass soldering process which can be either the batch or in-line type. It offers the advantage of even heating of all components and boards and minimizes the risk of overheating since the soldering temperature is 419 degrees F. However, long dwell times are required for this process and the surface finish of the connections could have a granular appearance.

When using solder paste in any process, it must be noted that variations in paste deposition thickness will be required depending on component and pad size and geometry. The use of a common thickness could result in uneven solder quantities in the finished solder connection.

While all of these techniques are being used successfully, each manufacturer must select the one which will satisfy their own requirements regarding productivity, quality, cost efficiency and product design.

TRAINING

Since Surface Mount Technology differs so greatly from the standard thru-hole process, we cannot assume that our present workforce has the knowledge or ability to produce these products. They must be thoroughly retrained regarding the selected process, tools, techniques and required quality levels. To achieve this, formal training programs on all these items must be implemented! The program agendas for this training must include requirements for certification and recertification on a routine scheduled basis.

INSPECTION

As the size, geometry and surface appearance of the solder connections on SMD's will differ greatly from thru-hole connections, total inspection retraining will also be required. It will become mandatory to develop standardized workmanship criteria to assist inspectors in evaluating the quality requirements. Workmanship manuals should be produced using color photography as black and white photos and line art do not provide the detail needed to evaluate these complex connections. Requirements for the certification and recertification of inspection personnel must also be established.

REWORK

Since 100% acceptable workmanship is rarely attainable, rework is a necessary fact of life. Proper tools and techniques must be used to place the product back into the production cycle as safely and efficiently as possible. Typical rework methods are: Hand tools (Single and Dual), Hot Air/Gas, and Infra-Red.

Hand tools with a single heater and tip are generally standard soldering irons with specialized tips which match the geometry of the device being removed. While these tools can be used effectively for components such as chip and tantalum capacitors, component placement becomes very difficult when replacing components having multiple leads.

Dual tools have two heaters and tips which are joined into a single assembly with a hinge at the rear of the handles. This design permits removal and replacement of larger rectangular and square components such as SOIC's and PLCC's, but component placement may be difficult.

Hot Air/Gas reflow rework systems consist of a heater, interchangeable nozzles, board carrier and vacuum pick-up. Air or gas passes through the heater which heats the air to the required temperature. The heated air then passes through the nozzle which matches the geometry of the component being removed. The board is placed into the board carrier which allows precise placement of the component beneath the nozzle. The heated air is directed onto all soldered connections of the component and melts all connections simultaneously. The component is then removed from the board using the vacuum pick-up and raising the heater/nozzle assembly.

The replacement component is then placed into the heater/nozzle assembly which is then lowered until the component contacts the pads. This arrangement permits precise location of the replacement component.

MAGNIFICATION

The majority of surface mounted components are much smaller than the traditional components used for thru-hole technology. This means that magnification must be used to promote efficiency and quality. When selecting magnifiers, the power, type and lighting are very important considerations.

SUMMARY

Surface Mounted Technology is vastly different from previous techniques used for electronic assembly. This paper is not intended to provide solutions to the problems of this new technology. It is intended to raise questions in the readers minds and to encourage industry-wide standardization of design and quality requirements and the development of tools and processes to permit the efficient production of quality products.

NWC TP 6896
EMPF TP 0003

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A NOVEL APPROACH TO MANUFACTURING SURFACE MOUNT ASSEMBLIES

by

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Abstract

Implementing surface mount technology (SMT) into military systems has not progressed as rapidly as expected. One of the major reasons is the lack of availability of MIL SPEC surface mountable components. Therefore, if one is to realize the benefits of SMT, manufacturing processes must be developed that allow inserted components to be mounted on the same printed wire board (PWB) with surface mount components (SMCs).

Honeywell's Ordnance Division has developed manufacturing processes which allow SMCs to be mounted on both sides of the PWB and inserted components to be mounted on one side of the same PWB. The surface mount solder reflow and wave soldering is performed in a single-step solder system. This simplifies and reduces the number of manufacturing process steps for this type of surface mount assembly (SMA).

This paper describes three major types of SMAs and their complexity levels. Definitions of the SMA types and complexity levels are necessary for selecting production equipment and developing SMA processes. Assembly process limitations are directly related to the SMA type and complexity level. SMA layout guidelines and processes from solder deposition to cleaning are discussed. Full scale engineering development (FSED) hardware has been fabricated using the single-step solder process for SMAs with both SMCs and inserted components on the same PWB. The single-step solder process offers an excellent solution to fabricating electronic assemblies where SMCs and inserted components are mounted on the same PWB. Plans to expand and enhance the first generation SMA fabrication processes to accommodate higher complexity levels are discussed.

Introduction

Implementing surface mount technology (SMT) into electronic products can produce significant benefits. The following list shows some of the key areas where benefits can be achieved:

Size and Weight Reduction

- Approximately 50% board area required

- Either smaller or fewer cards
- Double-sided assemblies

Reduced Lead Capacitance and Inductance

- Increased switching speeds
- Noise reduction

Total Automatable Assembly

- Assembly cost savings for production

SMT applications in military products usually require the use of components that meet military specifications (MIL SPEC). Unfortunately, there is a lack of availability of MIL SPEC surface mount components (SMCs). Therefore, realization of SMT benefits today requires that surface mount assemblies (SMAs) be fabricated using both inserted components and SMCs.

The manufacturing processes for SMAs are mainly driven by component types and component mounting (i.e., components mounted on one or both sides of the printed wire board). When developing manufacturing processes for SMT, it helps to identify the universe of SMAs. The universe of SMAs was determined by types of SMAs (Type 1A, 1B, 2A, 2B and 3) and complexity levels (I, II and III). See reference Figure 1. The types of SMAs are determined by component types (i.e., SMCs only or mixed SMCs and inserted components) and component mounting (i.e., components mounted on one side of the PWB or components mounted on both sides of the PWB). The complexity level is driven by the lead pitch of the integrated circuits mounted on the PWB. The universe of SMAs as described shows 15 classifications of SMAs.

There is a high probability that manufacturing processes developed for a certain set of SMAs may not be optimum for another set. For example, manufacturing processes developed for SMAs with complexity levels I and II will not be adequate for complexity level III.

There are many approaches to developing manufacturing processes to fabricate SMAs using both inserted components and SMCs. One approach is to form the leads of the inserted components and mount them on the surface of the PWB using conventional SMC assembly processes. This approach is not very practical when there is a large variety of inserted components to be mounted on the PWB. Another approach commonly used is the two-step solder approach. In this approach, SMCs are attached to the PWB using a solder paste, which reflows at approximately 250°C (i.e., higher temperature than 183°C so it does not reflow when exposed to subsequent wave soldering) and the inserted components are mounted using conventional wave soldering. This approach is not optimum when considering overall manufacturing costs that result from the lack of minimization of process steps, reduced cycle time, reduced work-in-process and reduction in floor space, equipment and people.

Honeywell's Ordnance Division has developed manufacturing processes that can be used to fabricate type 1B, 2A, 2B and 3 SMAs of level I and II complexity. See Figure 1.

SURFACE MOUNT ASSEMBLY	COMPLEXITY LEVEL (INTEGRATED CIRCUIT LEAD PITCH)		
	I	II	III
	.040" - .050"	.020" - .025"	< .020"
TYPE 1 ● A SMCs ON 1 SIDE OF BD ● B SMCs ON BOTH SIDES OF BD			
TYPE 2 ● A SMCs AND INSERTED COMPONENTS ON THE SAME SIDE OF THE BD ● B SMCs ON BOTH SIDES OF THE BD AND INSERTED COMPONENTS ON 1 SIDE OF THE BD			
TYPE 3 SMCs ON THE BOTTOM SIDE OF THE BD AND INSERTED COMPONENTS ON THE TOP SIDE			
	ASSEMBLIES TO BE ADDRESSED		FUTURE ENHANCEMENT OF PROCESS TECHNIQUES

FIGURE 1. Universe of Surface Mount Assemblies.

The approach is a single-step solder approach. The manufacturing processes were developed to allow inserted components and SMCs to be mounted on the PWB. Solder reflow of SMCs and wave soldering of inserted components are accomplished in one operation with a single-step solder system. Process simulation has shown a reduction in cycle time and work-in-process over the two-step solder approach.

TECHNICAL DETAILS ON SMA PROCESSES

The block diagram (Figure 2) shows the process steps utilized by Honeywell Ordnance Division to produce surface mount assemblies incorporating single-step soldering. Each operation is detailed below:

- **Bake-Out Base Board** – This operation is performed to drive out moisture, and is done regardless of assembly methods. Typical bake-out is 12-16 hours at 80°C. The step is omitted in the case of ceramic or porcelainized steel substrates.
- **Dispense Epoxy and Place SMC, (solder side)** – This step is accomplished using a component placement machine equipped with an epoxy dispensing syringe. The epoxy is dispensed in small doses and, immediately following the proper component, is placed over the dot and into proper solder position.
- **Cure Epoxy** – The epoxy used is typically Ablestick 77-1 or 77-1LTC. The epoxies are cured between 80°C (LTC) and 140°C, depending on formulation. Typically, a small conveyORIZED reflow oven is used, although a batch, or box oven can suffice for this purpose. These low-temp epoxies are used to avoid oxidation temperatures.
- **Print Solder (top, or component side)** – A solder paste, typically 63Sn/37Pb, is deposited onto the top side component land areas of the PWB using an AMI Presco 8115 screen printer. The most common method of solder printing used is screen printing, using different screen thicknesses and mesh counts for various solder wet print thicknesses. For SMA Type 1 and 2, Level I and II, Table 1 shows the correct screen thickness for the various component mixes experienced. It should be noted that this data is not valid for complexity Level 3 devices, as the close lead spacing forces solder deposition to stainless steel solder masks, or a combination of solder plating and mask printing. To further complicate this situation, a mixture of tall chip capacitors (.060" and greater) combined with Level III complexity devices on the same PWA can make selective solder dispensing on tall components necessary, to realize correct solder fillet volumes in accordance with military specifications.
- **Insert Through-Hole Components** – This step is typically accomplished on semi-automatic systems, which sequence, cut and bend, insert leads through the PWB, and finally cut and clinch the leads on the solder side of the board. The only difference between this operation and standard through-hole board population is the layout considerations involving spacing between leads requiring clinching and backside SMCs, which are now epoxied in place on the solder side of the PWB. Caution must be exercised to avoid allowing cut and cinch tooling to strike the body of surface mounted components.

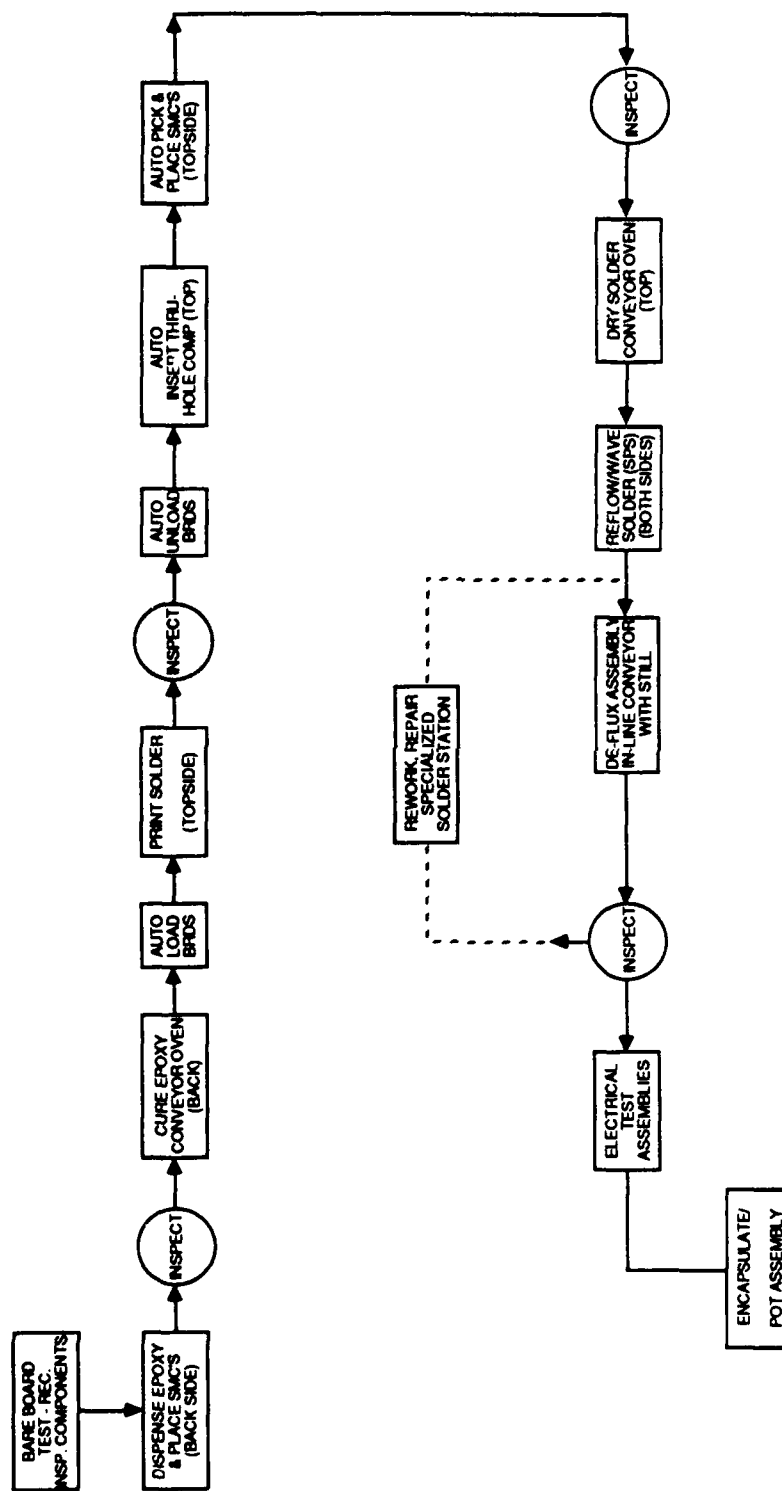


FIGURE 2. Assembly Process Flow Diagram for Type 2 Board.

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TABLE 1. Summary of Solder Screen Evaluation.

SCREEN TYPE		THICKNESS WET	REFLOWED THICKNESS	COMMENTS
80 MESH SS	12.0 MIL THICK	10.0 - 11.0 MILS	7.6 - 9.0 MILS	ACCEPTABLE SOLDER FILLETS AND SOLDER VOLUME FOR TALL SMC's. POOR PRINT RESOLUTION - SHORTING TO ADJACENT TAB OLB SITES, GOOD FOR OTHER SMC's.
	10.0 MIL THICK	9.0 MILS	5.0 - 7.0 MILS	FAIR TO GOOD RESOLUTION - ACCEPTABLE FILLETS & SOLDER VOLUME. GOOD FOR MAJORITY OF SMC WORK. POOR FOR HIGH I/O COUNT TAB DEVICES.
106 MESH SS	9.0 MIL THICK	8.0 MILS	4.0 - 6.0 MILS	GOOD PRINT RESOLUTION. GOOD FILLET SIZE AND VOLUME. ACCEPTABLE OVERALL FOR MOST TYPES OF DEVICES. ACCEPTABLE FOR COMPLEXITY LEVEL II TAB OLB.
	6.0 MIL THICK	6.0 MILS	3.0 - 4.0 MILS	EXCELLENT PRINT RESOLUTION. POOR FILLET SIZE - NOT ENOUGH SOLDER VOLUME FOR MOST SMC's. ACCEPTABLE FOR COMPLEXITY LEVEL II TAB OLB.
120 MESH SS	8.0 MIL THICK	8.0 MILS	4.0 - 6.0 MILS	EXCELLENT PRINT RESOLUTION. GOOD FILLET SIZE - CORRECT SOLDER VOLUME FOR VARIOUS SMC's, MIXES MARGINAL FOR LEVEL II TAB OLB.

- **Place SMCs (top, or component, side)** — This operation is similar to that described for backside SMC placement. However, due to devices of higher complexity levels being mounted onto this surface of the board, "part-to-pad" alignment vision systems are employed to ensure that close lead spaced devices are placed into the wet solder past on the conductor pads. As complexity level increases, this type of placement system becomes necessary and more sophisticated than standard x, y, theta, mechanical offset corrections system.
- **Solder Drying** — This operation is listed as optional for mixed technology assemblies because the infra-red/convection combination of solder paste heating does not require dried solder paste. When using vapor-phase soldering, this is necessary because of the rapid rate of temperature rise inherent in these systems. Also, certain solder paste manufacturers specify drying to drive off printing vehicles present in their products. The inclusion of this step in a process must be empirically determined.
- **Single-Pass Soldering** — This machine is the cornerstone to successfully producing Type 2 and 3, Level I and II complexity SMAs with a single-solder process, and is therefore reported in specific detail as follows.

The Hollis SPS System configuration (Figure 3) shows the elements of interest that require monitoring and control. This system can be subdivided into the following sections:

1. Finger Conveyers — 2 sets
2. Wave Fluxer, Flux Knife, Flux Density Controller
3. Infrared Preheaters — 2 sets
4. Dual Solder Waves
5. Wave Solder Hot Air Knife
6. Secondary Infrared Heaters — 2 sets
7. Surface Mount Hot Air Knives — 3
8. Cooling Fans — Set of 4

Each section has a number of controllable parameters to realize fully controlled solder profiles. These are discussed below.

- **Finger Conveyers** — This machine has two separately adjustable conveyer sections. The adjustments are made for board, or if desired, pallet width; the adjustments are two hand cranks. Belt speeds are controlled and displayed (0-10 fpm) on the front control panel.
- **Wave Fluxer** — The wave fluxer is motor driven and adjustable. The flux density controller automatically maintains the specific gravity of the given flux by adding solvent or fresh flux as required. The flux air knife evenly distributes a thin layer over the backside of an assembly. The pressure and angle of air is adjustable.
- **Infrared Preheaters** — The purpose of the top and bottom preheaters is to slowly raise the board temperature prior to wave soldering, thus minimizing or eliminating thermal shock to electronic components. The preheaters have dial-type power

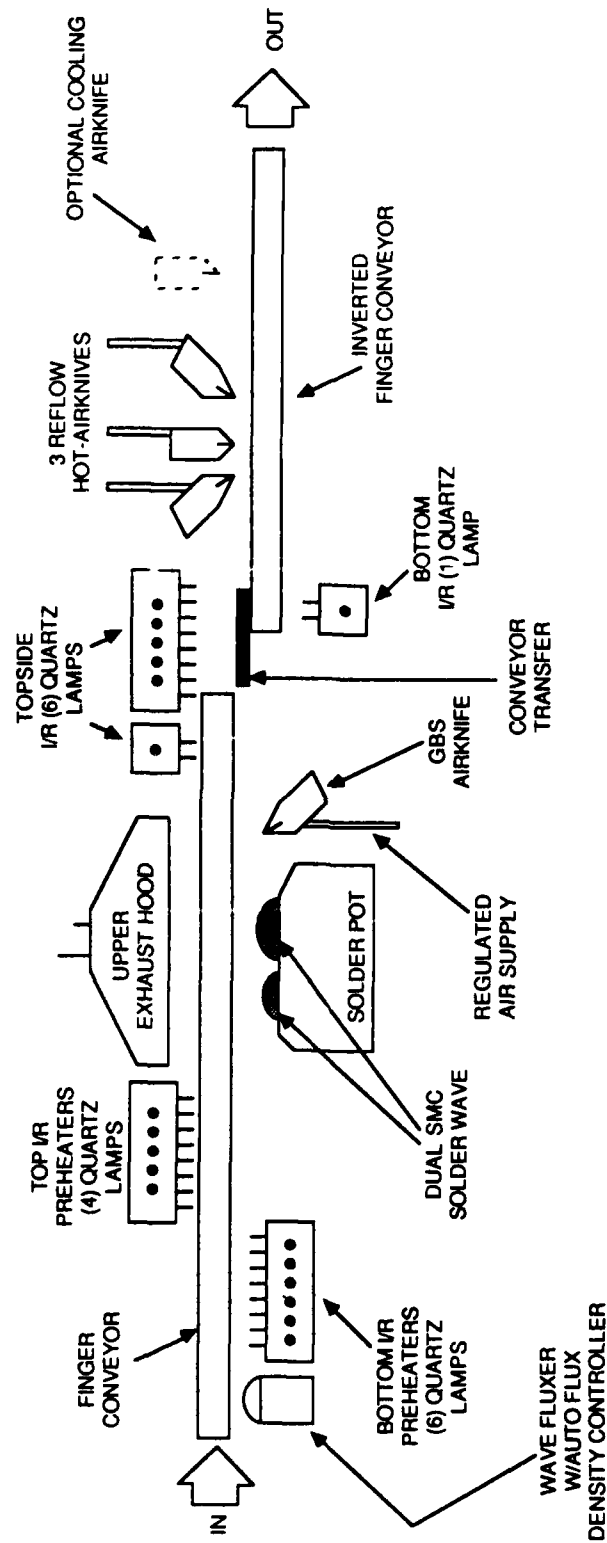


FIGURE 3. Diagram of Single-Pass Soldering System (SPS).

settings and feedback through thermocouples to a digital display on the operator control panel. Thus, preheating assemblies can be precisely controlled; an advantage not found on vapor phase type systems.

- **Dual Solder Waves** – The first wave is a narrow, energetic “chip-wave” which forces solder onto the pad areas of SMCs, soldering the backside chip components. The second wave is a smooth “Z-wave,” which refines and completes all backside soldering, including through-hole leads. The option of oil intermix is present, although this has not been explored. Both waves can be controlled for temperature, wave height, wave pump speed, and oil intermix, if desired.
- **Hot Air Knife** – A heated air knife supplies a pressurized hot air stream against the back of the assembly. The purpose is to debridge any close solder joints, as well as to shape all fillets for correct solder volume. The knife is adjustable for temperature, air pressure, angle of air delivery, and distance of airjet nozzle to back of board. This feature precludes the need for angling the entire conveyor assembly, as in standard wave soldering. The populated board therefore remains flat to ensure SMC soldering success.
- **Secondary IR Preheaters** – The purpose of these quartz lamps is to further increase assembly temperature to initiate solder paste reflow. The heaters are controlled as previously detailed. Both top and bottom heaters are present.
- **Hot Air Knives 2, 3, 4** – The three remaining air knives provide controlled temperature and pressure—convective heating to the top of the assembly to complete solder paste reflow and alleviate shadowing problems by providing thermal energy under and around top-side SMCs. These knives are also angle adjustable, and provide digital temperature readouts.
- **Cooling Fans** – Forced air cooling is available after all solder operations are completed. This feature has not been investigated, due to limitations per military specifications.

To simplify the procedure of parameter control, a form containing all process information is utilized. This is an easy method of noting process variable modifications.

Refer to Table 2 for an example of this form and parameters for three different board constructions. Included are a typical FR-4 glass epoxy board, a copper/invar/copper polyimide laminate board, and a porcelain enameled steel board.

A. Design of Test Vehicles

Three types of PWB constructions were fabricated and used to evaluate the single-step solder process.

- 1) FR-4 Fiberglass-Epoxy Boards
- 2) Cu/Invar/Cu (Polyimide) Constrained Boards
- 3) Porcelainized Steel Core Boards

TABLE 2. SPS Machine Parameter Data Sheet.

BOARD TYPE		FR-4 PWA	Cu/IN/Cu PWA	PEB PWA
SOLDER PASTE		SC3301 63/37	SC3301 63/67	SC3301 63/37
CONVEYOR SPEEDS ft/min				
GBS III		4.0	4.0	4.0
GBS III		4.1	4.1	4.1
PREHEAT TEMPERATURES °F				
GBS	BOTTOM	1.6	2.2	2.0
	TOP	1.6 230°F	2.2 220°F	2.0 220°F
SPS	MODULE 1	1.2	1.6	1.2
	MODULE 2	.4	1.0	.4
	MODULE 3	8.0	8.0	8.0
ANGLES		AIRKNIFE PARAMETERS		
AIRKNIFE 1		55°L	55°L	55°L
AIRKNIFE 2		90°	90°	90°
AIRKNIFE 3		90°	90°	90°
AIRKNIFE 4		90° (OFF)	90° (OFF)	90° (OFF)
FLOWRATES		PSI/SCFM		
AIRKNIFE 1		47.5	47.5	47.5
AIRKNIFE 2		35	35	35
AIRKNIFE 3		35	35	35
AIRKNIFE 4		35	35	35
TEMPERATURE °F		SP/TC		
AIRKNIFE 1		725°F	735°F	750°F
AIRKNIFE 2		735°F	735°F	735°F
AIRKNIFE 3		735°F	735°F	735°F
AIRKNIFE 4		OFF	OFF	OFF
DISTANCES (X ₁)		.200"	.200"	.200"
A/K2 TO REF. (X ₂)		.500"	.500"	.500"
A/K3 TO REF. (X ₃)		.500"	.500"	.500"
A/K4 TO REF. (X ₄)		.500"	.500"	.500"
ASSEMBLY TYPE		TYPE II B	TYPE II B	TYPE II B
TRANSFER				
REGISTRATION SHIFT				
FLUX		KENCO 333	MIL (RMA)	
FUSING				
BD. SCORCHING		NONE	NONE	NONE
RAIL TEMP. °F				
CABINET AIR TEMP. °F				
COMMENTS:		ACCEPTABLE FILLETS BOTH SIDES; BACKSIDE PADS FILLETS STILL BULBOUS MAY NEED PAD MODIFICATION	ACCEPTABLE FILLETS BOTH SIDES; BACKSIDE FILLETS BULBOUS MAY NEED PAD MODIFICATION	THICK FILM LEACHING EVIDENT; DUE TO % SOLIDS IN CONDUCTOR MAY NEED PAD MODIFICATION

These board types were chosen because of their various desirable properties with respect to commonality and/or reliability.

The electronic circuit design and layout were performed on a computer-aided-design (CAD) system. The electronic design allows all assembly types, regardless of component mix, to be assembled, soldered and tested in the same manner, varying only in the number of components on a given size of the board. The component layout for this board is shown in Figure 4. The electronic component list is given in Table 3. The redundancy of circuit design for one circuit on this board allowed an "either-or" assembly sequence, so that Type 2 and Type 3 SMAs could be realized merely by substituting surface mount components (back side) for through-hole components. This allowed all electrical test probing to be done from one side, using conventional probe fixturing.

This universal design allows each board construction (FR-4, Cu/In/Cu, porcelain steel) to be assembled as either a Type 1, Type 2, or Type 3 SMA. This results in 12 permutations of test specimens. Once completed, these units were environmentally tested.

After fabrication, the PWAs were submitted to visual inspection by Quality Assurance personnel. The accept/reject criteria employed for component solder joints conformed to DOD-STD-2000. These criteria were also used at each environmental test interval to determine if any degradation occurred due to exposures.

B. Environmental Testing

In order to determine the reliability of the SMAs fabricated by the aforementioned set of processes, an environmental test plan was instituted to subject a group of SMAs to the conditions detailed in Figure 5. Each group of SMAs was electrically tested at the specified intervals, and a sample of these units was visually inspected at intervals for signs of solder joint degradation.

A summary of the environmental test results is given in Table 4. Wherever possible, probable failure causes were listed. From these results, certain interferences on individual component's limitations with respect to the single-step soldering process can be made. These are given in the following section under component limitations.

C. Design Guidelines and Process Limitations

In review of the data collected, certain statements can be made about board/component layout and limitations of certain components with respect to single-step soldering.

- **Component Land Area (Pad) Design** – For SMCs, component solder pads were generated based on the following equations:

$$1) PL = 1/2 H_{\text{comp}} + (ET + .005")$$

$$2) PW = CW + .005"$$

$$3) PS = PL - 2 (ET + .005")$$

where

PL = Pad Length

PW = Pad Width

PS = Pad Separation

H = Height (thickness)
of component

ET = Dimension of End
Termination

4172-11-B

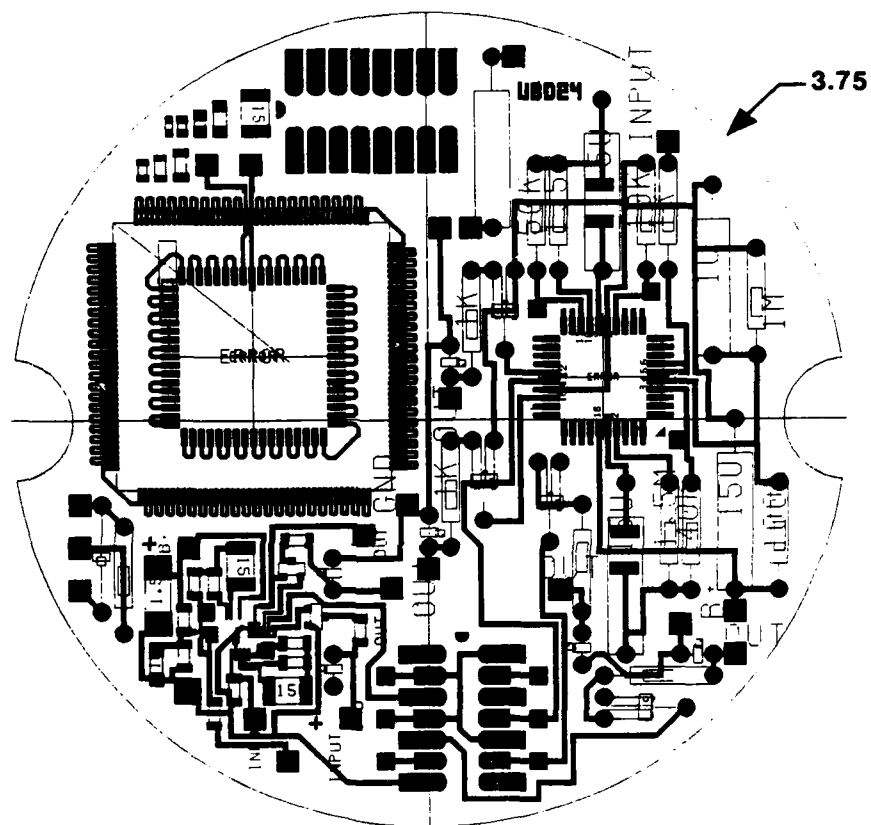


FIGURE 4. Component Layout.

TABLE 3. Electronic Component List of Test Vehicle.

DESCRIPTION	COMPONENT TYPE	QTY/BOARD
DUAL TIMER - 40 I/O LCC	SMC (.040" PITCH)	1
DUAL TIMER - TAB PKG.	SMC (.020" PITCH)	1
DAISY CHAIN - 172 I/O LCC	SMC (.025" PITCH)	1
LF 147 QUAD OP-AMP - 14 PIN TAB PKG.	SMC (.020" PITCH)	1
LF 147 QUAD OP-AMP - 14 PIN DIP	THRU-HOLE AXIAL	1
74LS74 "D" FLIP-FLOP - 14 PIN SOIL	SMC	1
54LS74A "D" FLIP-FLOP - 14 PIN DIP	THRU-HOLE AXIAL	1
2N2222A - TO 52	THRU-HOLE AXIAL	0-4
2N2222A - SOT 23	SMC	2-6
ZENER DIODE, 4.7V	THRU-HOLE AXIAL	1
ZENER DIODE, 4.7V	SMC (MELF)	1
RESISTORS: 1.5 M Ω	SMC & THRU-HOLE AXIAL	4
1.0 M Ω	SMC & THRU-HOLE AXIAL	2
100 K Ω	SMC & THRU-HOLE AXIAL	4
50 K Ω	SMC & THRU-HOLE AXIAL	2
40 K Ω	SMC & THRU-HOLE AXIAL	2
10 K Ω	SMC & THRU-HOLE AXIAL	2
1 K Ω	SMC & THRU-HOLE AXIAL	8
CAPACITORS: 180 μ F TANTALUM	AXIAL THRU-HOLE	1
15 μ F TANTALUM	SMC & THRU-HOLE AXIAL	2
1 μ F TANTALUM	SMC & THRU-HOLE AXIAL	2
.15 μ F MONOLITHIC	SMC & THRU-HOLE AXIAL	5
1000 p F MONOLITHIC	SMC ONLY	2
.01 μ F MONOLITHIC	SMC ONLY	2

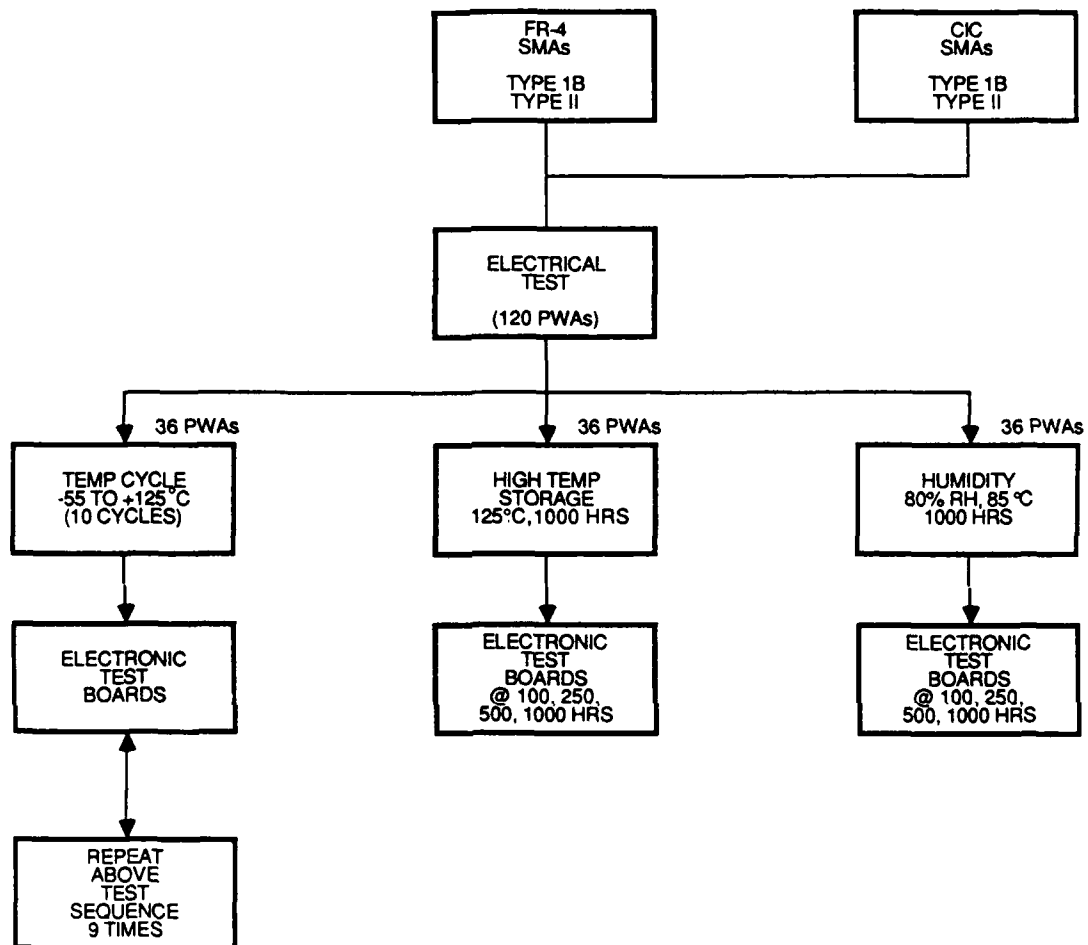


FIGURE 5. Flow Diagram of Environmental Testing.

TABLE 4. SMT Assembly Environmental Test Results.

GROUP #	TEST	RESULTS	CAUSE/ COMMENTS	ASSEMBLY TYPE
1	HIGH TEMP STORAGE		-	-
	AFTER 100 HOURS	NO FAILURES	-	-
1	AFTER 250 HOURS	NO FAILURES	-	-
1	AFTER 500 HOURS	NO FAILURES	-	-
1	AFTER 1000 HOURS	BD #65, OSC. #1, LCC CKT.	AXIAL CAP (TANT)TERM.	I1A FR-4
		BD #116, OSC. #1, LCC CKT.	AXIAL CAP (TANT)TERM.	I1A FR-4
2	TEMP/HUMIDITY (85°C/85% RH)		-	-
			-	-
2	AFTER 100 HOURS	NO FAILURES	-	-
2	AFTER 500 HOURS	NO FAILURES	-	-
2	AFTER 1000 HOURS	NO FAILURES	-	-
3	TEMP CYCLING -55°C TO + 125°C			
	AFTER 10 CYCLES	BD #119, OSC #1, LCC CKT	CRACK IN CHIP-CAP	I1B FR-4
	AFTER 20 CYCLES	NO FAILURES	-	-
	AFTER 30 CYCLES	NO FAILURES	-	-
	AFTER 40 CYCLES	BD #89, 172 VO LCC, 3 LEADS (VISUAL)	ELECTRICALLY ACCEPT	I1B FR-4
	AFTER 50 CYCLES	NO FAILURES	-	-
	AFTER 60 CYCLES	BD #8, OSC #1, LCCC CKT.	CASTELLATION CRACKED	I1B FR-4
	AFTER 70 CYCLES	BD #8, OSC #2, LCCC CKT.	CASTELLATION CRACKED	I1B FR-4
		BD #118, OSC #1, LCC CKT.	CAUSE UNKNOWN	I1A FR-4
	AFTER 80 CYCLES	BD #29, OSC #2, LCCC CKT.	CASTELLATION CRACKED	I1B FR-4
	AFTER 90 CYCLES	BD #27, OSC #1, LCC CKT.	CAUSE UNKNOWN	I1B FR-4
	AFTER 100 CYCLES	NO FAILURES	-	-

These formulas were generated empirically for surface mount devices on the top (component) side of a PWB, and are based on successful results for reflow soldering components placed into printed solder paste. These pad geometries were also utilized on the back (solder) side of these PWBs, where SMCs were epoxied in place and run through solder waves. The visual criteria employed to inspect the solder fillets indicated that backside fillets on SMCs were bulbous, or excessive in solder volume. As a result, further work in this area will center on optimizing solder fillet volume and shape for backside components. The modification to be investigated will focus on pad width and extension of pad length beyond end termination.

- **Component Orientation**

- Backside SMCs such as chip capacitors, resistors, and metal electrode face-bonded diodes should be oriented so that the end terminations are perpendicular to wave direction.
- Components with gull wing leads, such as SOICs, SOTs and Flatpacks (where permitted) should be processed so that their length runs parallel to wave direction, to avoid bulbous fillets.
- Leaded or leadless chip carriers, Quad Packs, and devices with lead pitch less than .040" should be mounted on the top side of the PWB, as these components exhibit best solder fillets when solder is printed to a controlled thickness, as opposed to non-selective molten solder contact.

- **Component Limitations**

- Polycarbonate Capacitors (both axial and surface mount), by nature of construction cannot survive the temperatures of either vapor phase soldering or single pass soldering. These components should be avoided.
- Solder sealed electrolytical capacitors (axial) have displayed a tendency to separate lead from component body due to solder slug reflow during SPS processing. A recommendation is to procure these types (10Sn/90Pb) of components, if necessary, with high temp solder alloy in lieu of Sn 63 solder sealed ends.
- Card Edge Connectors — During soldering, certain edge connectors have been observed to "craze" in the process as a result of the construction materials used in their manufacture. This phenomena is not unique to this system, but is a function of heating the connector above its maximum rated temperature. A solution to this problem is to specify solder temperature to vendors supplying these components. An alternative solution is to shroud these components using a stainless steel or aluminum foil, as this will divert direct heat from top infrared lamps and stop nitrogen knives from damaging components. However, as density of circuits increases, this method may become prohibitive and add extra manual operations.
- Termination finish of chip capacitors, resistors, etc., should be specified in procurement to have nickel/tin plated end terminations to avoid termination leaching, regardless of soldering method or machining used.

In review of the results of environmental testing, the failures observed were predictable (i.e., solder castellations cracking on FR-4 board cores) in most cases. The incidence of axial capacitors and termination shorting was also not a new phenomena, as this has been observed in past processes. In summary, this process sequence did not cause any failure mechanisms unique to this method of assembly.

CONCLUSION

Surface mount assembly manufacturing processes, which were developed using a single-step solder approach, offer an excellent solution for fabricating type 2 and 3 SMAs (i.e., mounting inserted components and SMCs on the same PWB). The single-step solder approach minimizes process steps, reduces cycle time and reduces work-in-process. SMA test vehicles were fabricated and exposed to environmental testing. Environmental testing revealed failures resulting from the coefficient of thermal expansion mismatch between leadless ceramic chip carriers and epoxy glass print wire boards. Environmental testing did not reveal any failures which could be attributed to the single-step solder process. The single-step solder surface mount assembly manufacturing processes are presently being used to fabricate full scale engineering development hardware for military products.

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Obtaining Wave Solder Parameters for Types II and III Surface Mount Assemblies

by

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ABSTRACT

Two different wave solder machines were evaluated to optimize wave soldering parameters for Types II and III surface mount assemblies. Specifically, to establish a bottom side chip cap preheat rate of less than 2°C/sec while maintaining a temperature differential from last preheat to first wave of less than 100°C. Both wave soldering systems were able to fulfill these requirements, although differences in the two machine designs significantly affected the tolerance and variation of the data. Original production parameters were modified to achieve these results.

INTRODUCTION

The purpose of this study was to optimize wave soldering parameters for Types II and III surface mounted assemblies. Type II surface mount technology is mixed surface mount devices (SMDs) top and bottom, and through hole components. Type III technology is defined by through hole components top side and bottom side mounted SMDs. Specific process goals were to obtain a chip capacitor preheat rate of less than 2°C/second and a maximum temperature differential from last preheat to first wave of less than 100°C (Reference 1). This criteria was established by Murata-Erie and AVX, two chip capacitor vendors, as key variables to successfully wave solder bottom side mounted chip caps. The rationale is that smooth even preheating minimizes thermal shock and microcracking, which may effect component capacitance values.

There are many advantages in using surface mount designs such as greater printed wiring board (PWB) density, automated assembly and increased circuit performance. Unfortunately, due to the unavailability of some surface mount parts, a combination of through hole and surface mount must be considered. In these cases, the wave solder machine can be used to solder all components in a single pass.

EXPERIMENTAL DESIGN

Two different wave solder machines from the same vendor but with different configurations were evaluated in this paper. Both machines have a chain conveyor, foam fluxer, dual wave and pallet tooling. Machine A is nine years old and has a larger preheat section which consists of two "jet driers" (forced hot air blowers) and two retrofitted IR quartz plate preheaters for an effective length of 62" (see Figure 1). As will be pointed out later, a larger preheat zone is advantageous in attaining the desired thermal characteristics.

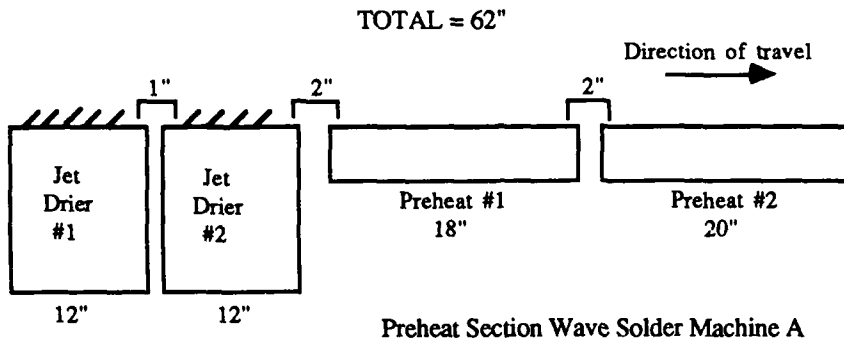


Figure 1

Machine B is one year old and has three 23" IR preheaters with one of those mounted for top side heating (see Figure 2). This wave machine also contains a single vibratory wave system which claims to eliminate the need for the dual wave approach. This is an advantage since the solder contact time is significantly reduced and should minimize chip cap termination leaching.

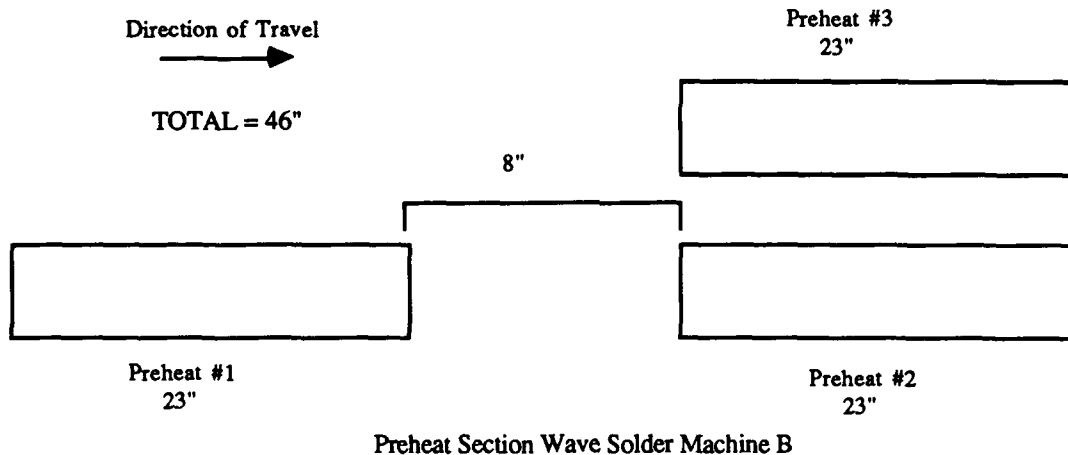


Figure 2

One test board was used throughout the experiment. It was an 8 layer PWB measuring 8" x 9" x .062". The PWB had 0.010" (30AWG) thermocouple wires bonded in five locations (see Figure 3). These are:

<u>THERMOCOUPLE</u>	<u>LOCATION</u>
1	Inside chip cap on bottom side of PWB
2	Top of SOIC on bottom side of PWB
3	Leading edge on bottom side of PWB
4	Top of through hole IC on top side of PWB
5	Leading edge on top side of PWB

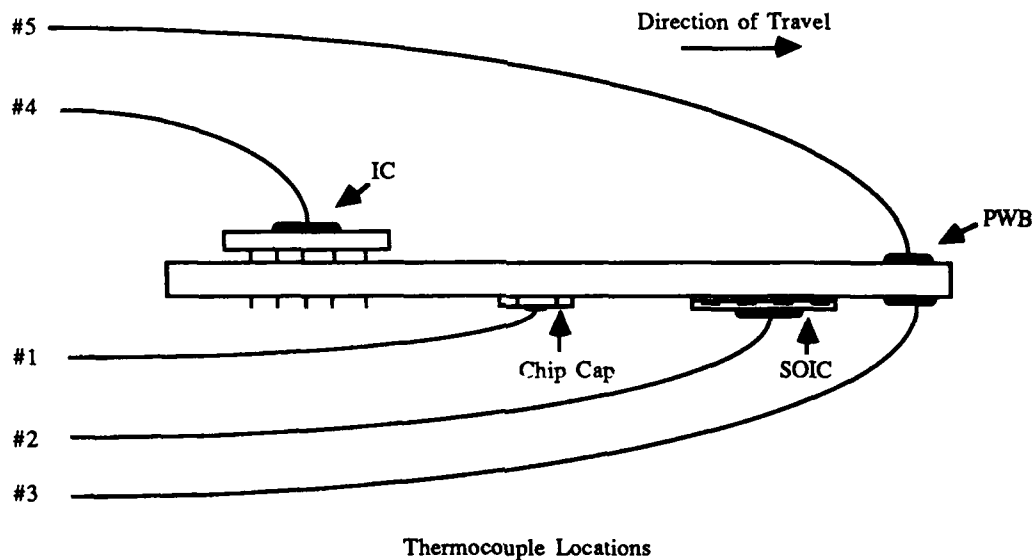


Figure 3

The thermocouples were bonded in place with a black, thermally conductive, epoxy adhesive. Care was taken to minimize the amount of adhesive used. An experiment consisting of submerging a test board into boiling water revealed that a small amount of adhesive induced a thermal lag of only 1°C during heating and 5°C during cooling compared to a bare thermocouple. Relatively large amounts of adhesive caused temperature differentials of 10 to 20°C.

The five thermocouples were plugged into a sophisticated data logger that recorded temperatures from all five type K thermocouples simultaneously. Temperature readings were taken at one second intervals over a 400 second period.

After each run, the data logger was plugged into a personal computer and the data downloaded via the RS232 port. The data logger software displayed maximum temperatures, maximum rates of change, thermocouple locations, a graph of thermal profiles and individual data points. This data is available for each of the five thermocouples at each one second interval over the testing time span of 400 seconds. Temperature rates of change have been calculated for points of specific interest using this detailed data.

RESULTS

Tables 1 and 2 itemize parameters and results of each of the nine runs. They are labeled Board 1 through Board 10 (Red Board 7 was removed due of a computer malfunction). The first eight rows are the machine settings and the next twelve rows are data taken off the data logger profile programs. The definitions of each measurement criteria are as follows:

1. Average rate of change: The arithmetic mean of the rates of temperature change (°C/sec) as measured at thermocouple 1.

Note: Does not include plateaus.

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2. Temperature drop between last preheat and solder pot: The amount of chip cap cooling occurring while PWB travels from the last preheat to solder contact as measured at thermocouple 1.
3. Maximum temperature on top PWB surface before wave: The PWB temperature measured at thermocouple 5 immediately before solder contact. Standard is approximately 104°C (220°F) for wave soldering (Reference 2).
4. Rise between lowest temperature after last preheat and solder: One of the critical criteria for wave soldering chip caps. The difference between the lowest temperature after preheat and the peak of initial solder contact. This includes temperature drop from definition #2.

Note: The maximum turbulent wave temperature recorded on thermocouple 1 was never 260°C (500°F). The average maximum initial solder temperature used was 230°C (446°F). This is the initial solder temperature used as referenced in the literature.
5. Total preheat time: The time measured on the data logger which recorded preheat time.
6. Solder Contact Time: Amount of time recorded over both solder waves as measured at thermocouple 3.
7. Cooling Rate: The average asymptotic cooling after the final solder wave.
8. Total average preheat rate: The overall average from beginning to end of preheat including plateaus in between.
9. Maximum temperature on top PWB surface after wave: The maximum top board temperature, usually occurring 2 to 3 seconds after wave, recorded on thermocouple 5.

The following paragraphs are brief descriptions of each run:

Machine A

Board #1: These are the original wave solder parameters when this study was initiated. Several problem areas were apparent right away. First, the average slope for Jet Drier #1 was too high (3.2 versus 2.0°C/sec.). Both of the preheat sections were too intense and not very smooth. The profiles also discovered a burnt out heating element on Jet Drier #2. This was later corrected by the third run. All other characteristics looked acceptable. The slope of preheat #2 was below 2.0°C/sec., and the temperature differential between the last preheat and first solder wave was 102°C, which is close to the 100°C criteria. Other pertinent information, such as preheat time, solder contact time and maximum top PWB temperature was acceptable.

Board #2: This run was conducted at higher preheat temperatures to evaluate if the delta between preheat and the solder pot could be reduced to below 100°C. The delta was lowered to 83°C, but at a cost of preheat slopes of 3.3 to 2.2°C/sec. Obviously, there is a trade off between preheat rate limitations and the temperature delta between preheat and the solder pot. It was also dramatically evident that a significant amount of cooling was occurring between the last preheat and first wave (22.5°C). This was due to the travel over the nonheated space, approximately 5", between the preheat and the solder pot. This was contributing to the high delta values. An evaluation was started to test reflectors in an effort to minimize thermal losses after preheat.

Board #3: The heating element in Jet Drier #2 was fixed and an average rate of 1.4°C/sec was recorded. The preheat was reduced, but high slopes were still recorded on Jet Drier #1 and Preheat #1. Additionally, the

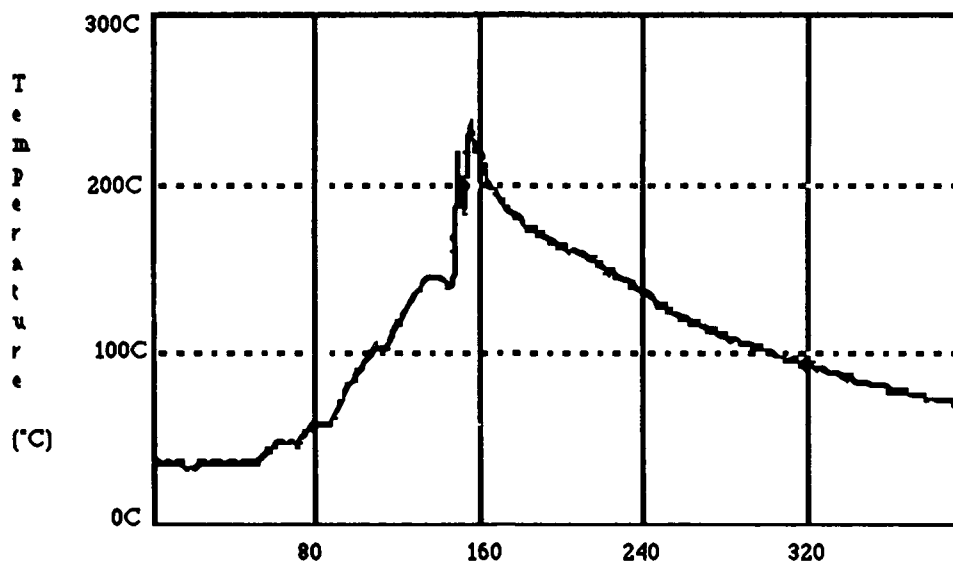
maximum top side board temperature was above the 355°F (179°C) melting point of SN62 solder (Reference 3). This is significant since any top side mounted SMDs previously soldered to the board would reflow.

Board #4: This is the best set of parameters for machine A (see Figure 4). The Jet Drier #1 setting was reduced to #5 on the dial. This created a smoother rate over both Jet Driers. Both preheat rates were acceptable; preheat #1 was slightly over 2.0°C/sec., but some minor adjustments could get it at 2.0°C/sec. An aluminum reflector was added between the last preheat and solder pot, which reduced the temperature drop from 17.2°C to 7.8°C. This helped keep the overall delta between preheat and solder to 88°C. Maximum top board temperatures remained below 179°C, so top side SMDs would not reflow.

TABLE 1. Machine A Results

	LOCATION	TRIAL #	BOARD 1	BOARD 2	BOARD 3	BOARD 4
S	Jet Drier #1 (Setting)		High	High	High	#5
E	Jet Drier #2 (Setting)		High	High	High	High
T	Preheat #1 (°C)		500	600	550	550
T	Preheat #2 (°C)		540	640	590	590
I	Preheat #3 (°C)		N/A	N/A	N/A	N/A
N	Reflector (Y or N)		N	N	N	Y
G	Conveyor Speed (FPM)		4.0	4.0	4.0	4.0
S	Omega Wave (Y or N)		N/A	N/A	N/A	N/A
M	Ave. Slope Jet Drier #1 (°C/sec)		3.2	3.1	3.2	1.2
E	Ave. Slope Jet Drier #2 (°C/sec)		*	*	1.4	1.2
A	Ave. Slope Preheat #1 (°C/sec)		2.6	3.3	2.7	2.3
S	Ave. Slope Preheat #2 (°C/sec)		1.6	2.2	1.7	2.0
U	Dip between last preheat & pot (°C)		10.5	25.5	17.2	7.8
R	Max. top board temp. (°C) before wave		105	132	123	117
E	Δ Rise between preheat & 1st wave peak (°C)		102	84	92	88
M	Total Preheat time (sec)		87	87	87	87
E	Solder contact time (sec)		4.1	4.1	4.1	4.1
N	Cooling Rate (°C/sec)		.77	.72	.77	.74
T	Total ave. preheat rate (°C/sec)		1.4	1.7	1.6	1.4
S	Max top PWB temp after wave (°C)		177	186	191	174

*-Burnt out element N/A-not applicable



Time (seconds)
Thermal Profile for Thermocouple 1
Figure 4

Machine B

Board #5: Since this is a new machine, preliminary wave solder parameters were chosen similarly to the actual product parameters. The short preheat zone made it difficult to achieve a 2°C/second preheat while attaining a high enough board temperature to have less than 100°C delta between preheat and the wave. The second preheat zone was too steep and the total preheat time was 68 seconds compared to the machine A of 87 seconds.

Board #6: All three preheat temperatures were lowered and aluminum foil reflectors were added. The differential between the average preheat slope of preheat 1 and preheat 2 progressively work toward each other until finally at Board 10 they are both the maximum 2°C/second. The added reflector helped minimize the temperature drop between the last preheat and wave solder pot. The top side heating unit setting was reduced because 195°C top board temperature would reflow top side mounted SMDs. Finally, the conveyor speed was reduced to 3.5 feet/minute from 4.0 feet/minute to increase the amount of preheat time to 78 seconds from 68 seconds.

Board #8: The top side preheat unit setting was lowered to decrease the average slope of the second preheat zone as well as lower the final top board temperature to 176°C, which is below the solder reflow point.

Board #9: This run utilized the single vibrating wave system instead of the standard dual wave approach to SMD wave soldering. The vibrating system does not affect any parameters except solder contact time. When the conveyor speed was reduced on Board #6, the solder contact time increased to 4.7 seconds from 4.1 seconds. With the vibrating system, the solder contact time was reduced to 3.3 seconds. This is advantageous since it reduces bottom side component temperatures and leaching of chip cap terminations.

Board #10: This is the last run for the machine B and probably the best (see Figure 5). Preheat #1 and #2 are exactly 2.0°C/second, the delta between last preheat and first wave is 98°C, and the retrofitted reflector

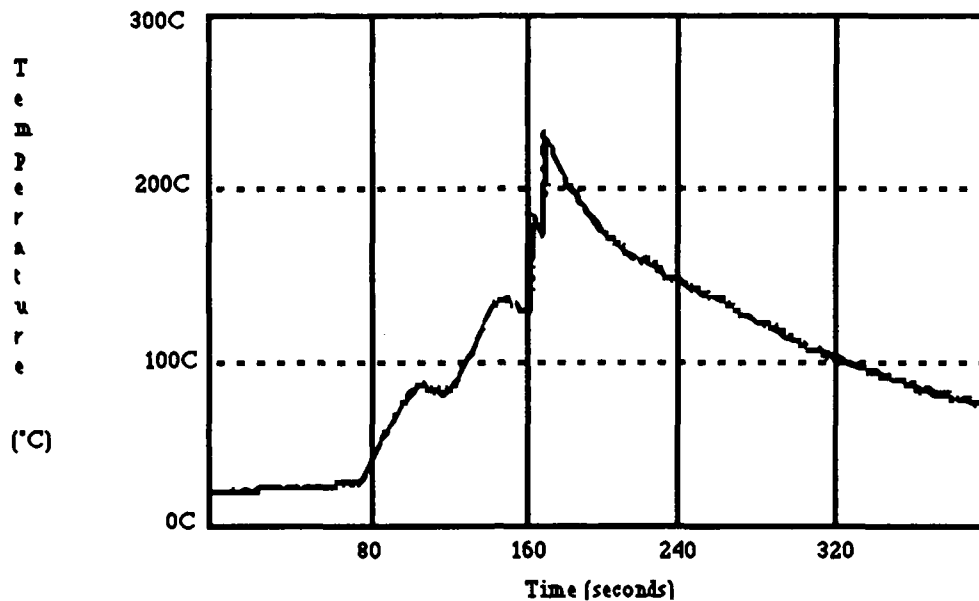
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reduced the temperature drop to 6.1°C. Problem areas remaining are the solder contact time was relatively high 4.7 seconds without the vibrating wave and the final top board temperature exceeded solder reflow temperatures (6°C).

TABLE 2. Machine B Results

	LOCATION	TRIAL #	BOARD 5	BOARD 6	BOARD 8	BOARD 9	BOARD 10
S	Jet Drier #1 (Setting)		N/A	N/A	N/A	N/A	N/A
E	Jet Drier #2 (Setting)		N/A	N/A	N/A	N/A	N/A
T	Preheat #1 (°C)		371	343	343	343	371
T	Preheat #2 (°C)		371	343	343	343	371
I	Preheat #3 (°C)		371	343	200	200	150
N	Reflector (Y or N)		N	Y	Y	Y	Y
G	Conveyor Speed (FPM)		4.0	3.5	3.5	3.5	3.5
S	Omega Wave (Y or N)		N	N	N	Y	N
M	Ave. Slope Jet Drier #1 (°C/sec)		N/A	N/A	N/A	N/A	N/A
E	Ave. Slope Jet Drier #2 (°C/sec)		N/A	N/A	N/A	N/A	N/A
A	Ave. Slope Preheat #1 (°C/sec)		1.9	1.6	1.7	1.6	2.0
S	Ave. Slope Preheat #2 (°C/sec)		3.2	2.7	2.1	1.8	2.0
U	Dip between last preheat & pot (°C)		10.0	2.2	7.7	6.7	6.1
R	Max. top board temp. (°C) before wave		122	152	99	101	126
E	Δ Rise betwn preheat & 1st wave peak (°C)		91	87	115	117	98
M	Total Preheat time (sec)		68	78	78	78	78
E	Solder contact time (sec)		4.1	4.7	4.7	3.3	4.7
N	Cooling Rate (°C/sec)		.75	.80	.76	.72	.72
T	Total ave. preheat rate (°C/sec)		2.0	1.6	1.4	1.3	1.5
S	Max top PWB temp after wave (°C)		N/A	195	176	170	185

N/A-not applicable



Thermal Profile for Thermocouple 1
Figure 5

DISCUSSION

Equipment design plays a significant role in whether or not these specific wave solder parameters are attainable. For example, the machine A has a 62" preheat zone compared to the 46" preheat zone of the machine B. The longer preheat zone made it easier to reach the desired thermal profiles. Additionally, top side heating does not seem to aid in this style of preheating. A slow even heat is desired, not a rapid, concentrated heat soak. Top side heating also obviously registered some of the highest maximum top board temperatures, which would reflow previously soldered top side SMD components.

A slower conveyor speed can compensate for a short preheat zone, but then the solder contact time increases as well (See Board 6). A two stage conveyor system would satisfy these requirements. The first stage could transport the product over the preheat while a second stage is used to speed up the product over the solder pot. In this way, two different conveyor speeds could be accomplished without impeding product flow. Or, one could buy a custom machine with an extra long preheat zone. Most standard wave solder machines do not have long preheat zones. Many vendors are decreasing overall size of the machines and the preheat zone is getting smaller but more powerful. For example, a new wave solder machine recently purchased has a smaller preheating zone than that of machine B. However, as previously mentioned, the vibrating wave of machine B could be used to minimize solder contact time when using slower conveyor speeds.

Another equipment design consideration is an air knife, which was not available for this experiment. This tool is used to remove excess solder shorts caused by low temperature wave soldering. Lowering the solder pot temperature will facilitate meeting the 100°C rise from preheat to first solder contact criteria. The problem is that the propensity for creating solder shorts increases as the solder temperature decreases (Reference 4). This is a result of the increased solder surface tension. The patented air knife theoretically blows off much of the excess solder shorts leaving a smooth shaped fillet. Some users have had some preliminary success using this low temperature soldering technique.

The thermal profiles on machines A and B were stepped between the preheat and soldering zones. This is a result of dead zones between preheating units. Preliminary work with simple reflectors exhibited promising results. If more efficient reflectors can be developed to even out the plateaus, it would be easier to meet the thermal profile demands. One vendor claims to have developed a surface coating that reflects 99.4% of near IR wave lengths. This reflector technology has already been implemented on some European wave solder machine designs. Samples for testing are being supplied for the machine A.

SUMMARY

This effort successfully acquired thermal profiles specific to wave soldering bottom side surface mounted devices for the two wave solder machines. The specific process goals were to obtain a chip cap preheat rate of less than 2°C/second and a temperature delta of less than 100°C between the last preheat and first wave.

Modifications of the original wave solder parameters were performed to achieve these goals on the machine A. Among these changes were:

- lowered Jet Drier #1 setting
- increased Preheat #1 and #2
- added reflectors.

The purpose of adjusting the preheater settings was to decrease the heating rates in some areas while increasing it in other areas. The added reflectors helped smooth out stepped areas between preheaters and the solder pot.

Machine B was also able to meet the soldering process criteria. This machine, as a result of a shorter preheat zone, had more difficulty in meeting these goals and has less room for error. On the other hand, the machine B's single vibrating wave feature exhibits potential for decreasing bottom mounted SMDs solder exposure.

CONCLUSIONS

- Reflectors do help smooth out irregular preheat plateaus.
- Top side heating does not help achieve smooth long preheat rates.
- Long preheat zones do help reduce preheating rates of change.
- Slower conveyor speeds do compensate for a short preheat zone, but they also significantly increase solder dwell time.

Finally, some topics that need future attention to evaluate potential process improvements are:

- Vibratory surface mount soldering to help reduce solder exposure time.
- Low temperature soldering using air knife technology to reduce thermal rise.
- Efficient preheat reflectors to smooth out stepped profiles.

BIBLIOGRAPHY

1. Murata Erie North America, Inc. Surface Mount Components Catalog and Application Manual, Catalog No. 61-07 (1986) pg. 26.
2. Howard Manko, Soldering Handbook for Printed Circuits and Surface Mounting, Van Nostrand Reinhold Co., N.Y. 1986.
3. International Society for Hybrid Microelectronics (ISHM), Surface Mount Technology, by Barbara Roos-Kozel, Silver Spring, Maryland, ISHM, 1984, pg. 117.
4. Howard Manko, Soldering Handbook for Printed Circuits and Surface Mounting, Van Nostrand Reinhold Co., N.Y. 1986.

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PLACEMENT AND SOLDERING OF HIGH LEAD-COUNT, HIGH DENSITY
COMPONENTS

by

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ABSTRACT

The advent of VHSIC (Very High Speed Integrated Circuit) and other technologies has created unique problems not only in manufacturing and packaging the components, but assembling them onto PWB's. The high density of leads per package area make hand soldering extremely time-consuming, yet mass soldering techniques such as wave, vapor-phase, and heater-bar cannot readily be incorporated without solving the alignment problems associated with fine lead pitch. This paper presents a "proof-of-concept" in which an alignment tool is used to place a 3-inch square, 332-lead package prior to vapor-phase soldering. This approach can successfully be utilized as an alternative to expensive vision placement systems.

INTRODUCTION

There are significant design advantages to utilizing high density packages. These include increased speed of data transfer, and reduction of size and weight of the final assembly. However, the very high-density, high lead-count components become difficult to solder efficiently because of the necessary alignment accuracy. Conventional mass soldering techniques such as wave, vapor-phase and heater-bar are often replaced by hand soldering, although the task becomes inefficient and extremely time-consuming. In order to successfully utilize mass soldering techniques, alignment must be insured through vision systems or special tooling. The process evaluations presented in this paper include the development of an alignment tool used to accurately place and vapor-phase solder a high-density component. In addition, producibility issues are

discussed in order to insure the smooth transition from design to manufacturing.

PACKAGE AND TOOL DESCRIPTION

The package used as the "proof-of-concept" in this study is approximately 3-inches square and contains 332 leads. Two complete sides and half of the two other sides have leads on a 50-mil pitch. The other half of the two sides have leads on a 25-mil pitch. The leads are gold plated and formed such that the stress relief radius extends from the top of the package, much like any standard quad-pack. The package is mounted onto a PWB, as depicted in Figure 1. In order to accurately align the leads of the package with the corresponding pads on the PWB, a tool was designed and fabricated.

The aluminum tool was designed to utilize existing tooling holes in the PWB for accurate alignment. The main body of the tool was designed to accommodate each lead in a cut-out. This would insure that the delicate leads were in proper formation prior to alignment and placement onto the PWB. In addition, the cut-out would isolate each lead from the ones that surround it and prevent bridging during the soldering process. A vacuum mating plate was also fabricated for handling the package without stressing the leads or damaging any of the internal circuitry. Figures 2, 3 and 4 illustrate the tooling concept.

PROCESS EVALUATION

Two methods of providing the necessary solder were evaluated: solder paste and fused solder (eutectic 63/37 Sn/Pb). Vapor-phase soldering was used in both instances. Table 1 provides a matrix of the process evaluations.

Table 1. Matrix of Process Evaluations.

	Solder Paste	Fused Solder
Screen Parameters	80-mesh 45 degrees	N/A
Thickness	8 mils	8-10 mils
Solder Type	Sn/Pb 63/37	Sn/Pb 63/37
Vapor Phase Parameters	419 F (215 C) 10 s dwell time	419 F (215 C) 10 s dwell time

Solder Paste Process

The metal screen was made from a right-reading positive of the outer-layer PWB artwork. As indicated in Table 1, it was an 80-mesh, 45-degree screen. Eutectic Sn/Pb solder paste was screened onto the PWB pads. The tolerance maintained in paste-to-pad alignment was ± 2 mils. This was done, of course, to minimize bridging. After screening, the PWB was placed in an oven at 60 C (140 F) for 30 minutes to remove the volatiles from the solder paste, thus minimizing the formation of solder balls. Once the paste was dry, the fixture was used to accurately place the leads of the component onto the PWB pads. This was done by aligning the tooling pins on the fixture with the tooling holes on the PWB. The fixture and assembly were exposed to a 10-second dwell in the primary vapor zone of a vapor-phase soldering system, followed by a 1-minute dwell in the secondary vapor zone prior to exiting. After cooling, the fixture was removed and the assembly was vapor-degreased in Freon TES.

Fused Solder Process

8-10 mils of Sn/Pb solder was manually added to the pads of

the PWB. Granted, this is not an efficient method of adding solder, but it was done to evaluate the use of fused electroplating, or fused paste that was screened onto the pads. In this instance solder paste could not be applied and fused because the tooling holes in the PWB were out of alignment with the holes in the screening tool, preventing accurate screening of solder paste. This fact will be explored further in the "Producibility" section of this paper.

Again, the placement tool was used to accurately align the leads of the component with the PWB pads. The soldering and cleaning was accomplished using the same processes as before.

RESULTS

The leads were inspected after cleaning. The most prevalent defects which occurred were insufficient and skipped solder joints in the assembly which utilized fused Sn/Pb. This was due to the inconsistencies within the solder which did not provide uniform reflow conditions; the fixture alone was not able to create enough pressure during reflow to make up for the inconsistencies in the topography of the fused Sn/Pb. This indicates that the method of solder application must be more planar in order to provide the necessary quality. The preferred methods of application would be solder paste, solder preforms, or plating 8-10 mils of Sn/Pb without fusing. Environmental testing was performed only on the assembly which successfully utilized solder paste.

Mil-Std-883 was used as the guideline for testing. 100 temperature cycles from -55 to 125 C (-131 to 257 F) were followed by 20g vibration in all three axes. Photographs were taken before and after each test. The package did not exhibit any lead detachment or microcracking at 200X magnification. To evaluate production capability, throughput data comparing hand to vapor-phase soldering was analysed. The results are given in Table 2.

Table 2: Comparison of Throughput Data

Process Variable	Hand (hr)	Tool (hr)
Tinning	Same	Same
Install onto PWB	0.13	N/A
Screen paste	N/A	0.12
Dry paste in oven	N/A	0.5
Install into fixture	N/A	0.25
Install fixture to PWB	N/A	0.25
Solder leads onto PWB	2.51	0.12
TOTAL	2.64	1.24

As indicated, there is a significant increase in production capability using the new method. The implementation cost (design and fabrication of necessary tooling) is easily offset by the cost savings in assembly.

IMPLEMENTATION: PRODUCIBILITY ISSUES

The following guidelines are recommended to insure successful implementation:

- 1) To insure reproducibility of solder paste alignment, tooling holes should be targeted on PWB artwork diagonally from each other.
- 2) Leads on packages should be supplied with a fused Sn/Pb finish. Pretinning by hand is time-consuming and inefficient; attempting to pretin in a solder pot creates

extensive bridging.

3) An analysis should be performed to minimize the fixed implementation costs. This involves optimizing the method of solder application (preforms, plating, or paste) as well as the manufacturing process flow. If plating is the chosen method, shelf life is decreased due to oxidation. This method should be chosen only if boards will be stored in proper conditions for short periods of time. Factors affecting the decision are company-dependent since the variables of quantity, schedule compliance, resource availability, and suppliers are not constant.

An example of the applicability of this "proof-of-concept" is mixed technology boards. The process flow would include the application of solder paste, automated placement of conventional SMC's, drying the paste, placement of high lead-count components using the properly designed alignment tool, mass vapor-phase soldering, then applying conventional PTH components by hand.

CONCLUSION

As hardware design specifications become more sophisticated, the need to utilize "superchip" technologies will increase. With these technologies come increased I/O requirements leading to high-density, high-lead count packages. To insure the ability of efficiently soldering these packages, producibility guidelines must be implemented along with accurate alignment techniques. The technique discussed in this paper provides a cost-effective alternative to vision placement systems or manual soldering while insuring proper alignment.

NWC TP 6896
EMPF TP 0003

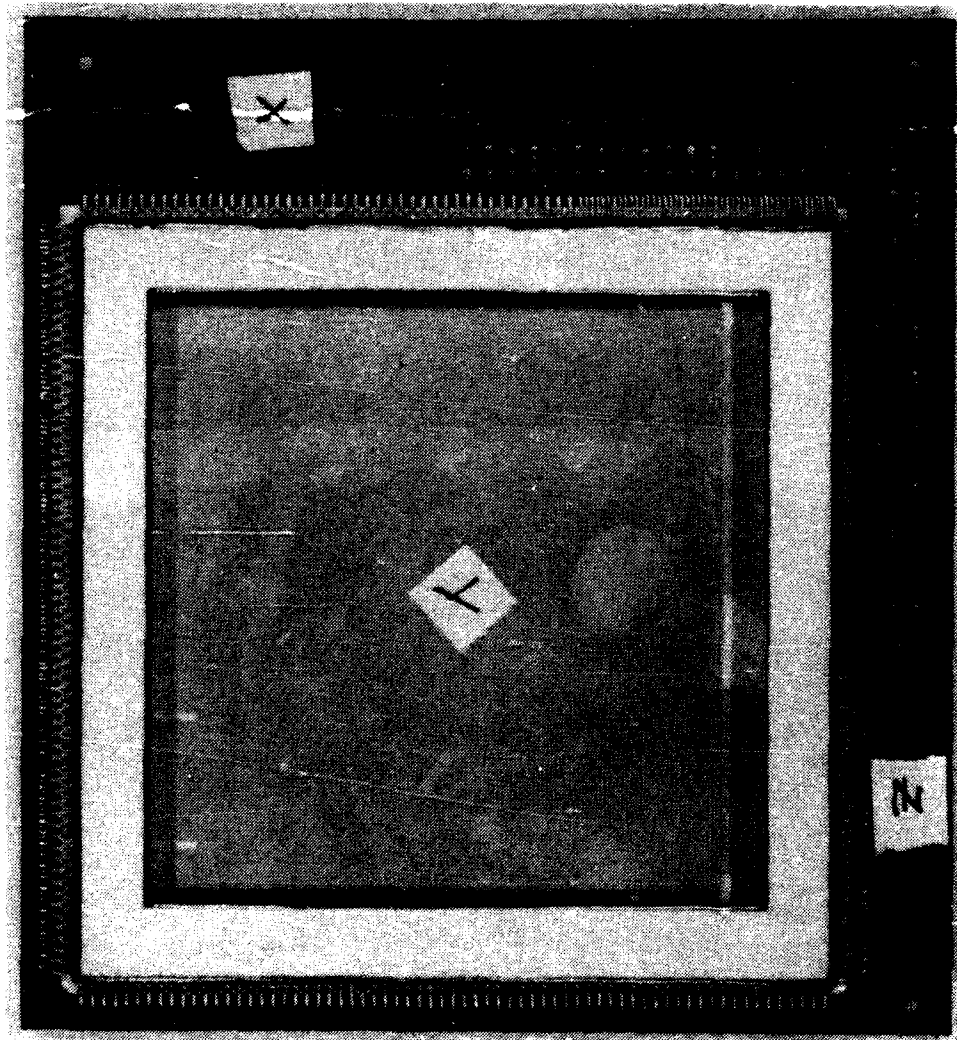


FIGURE 1: 332 Lead Package
Mounted on PWB.

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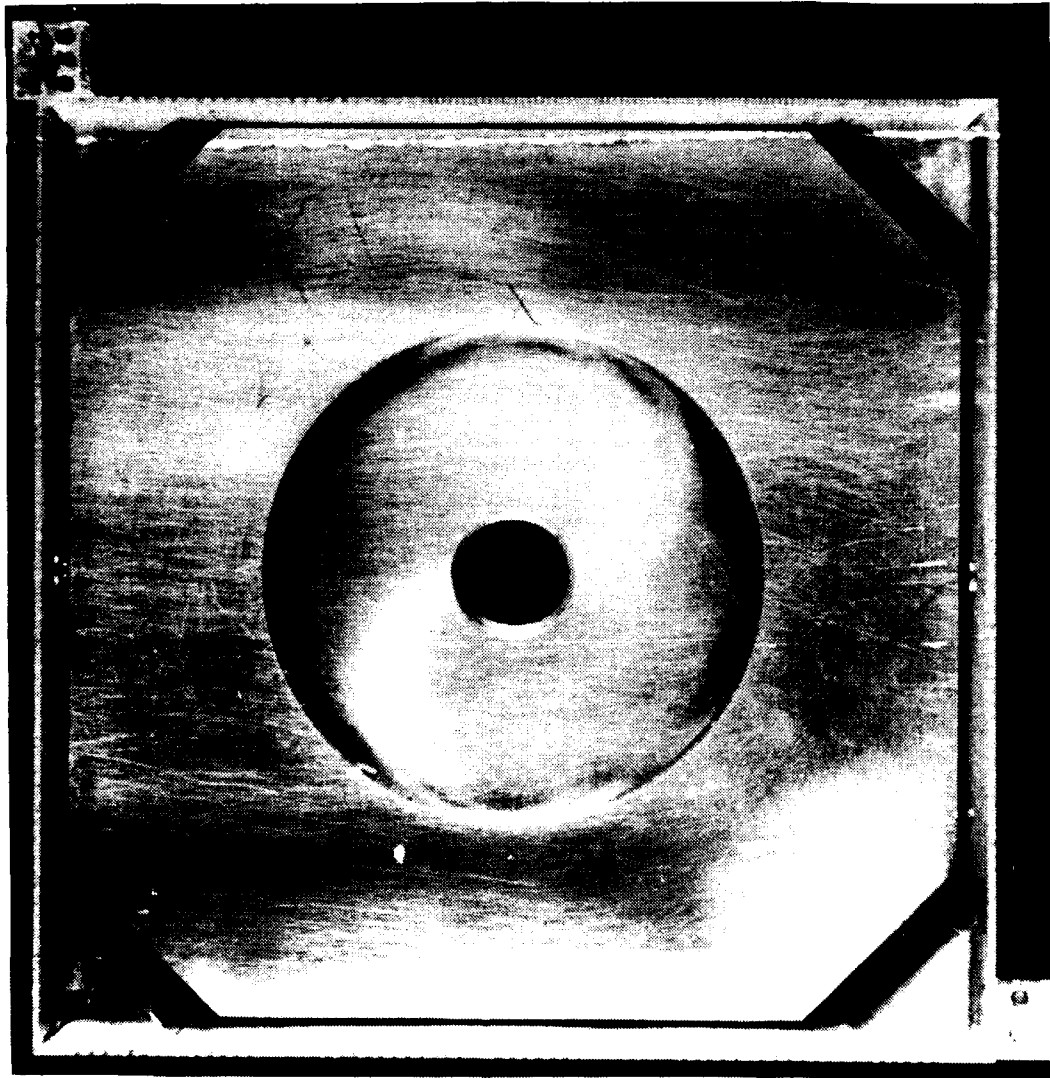
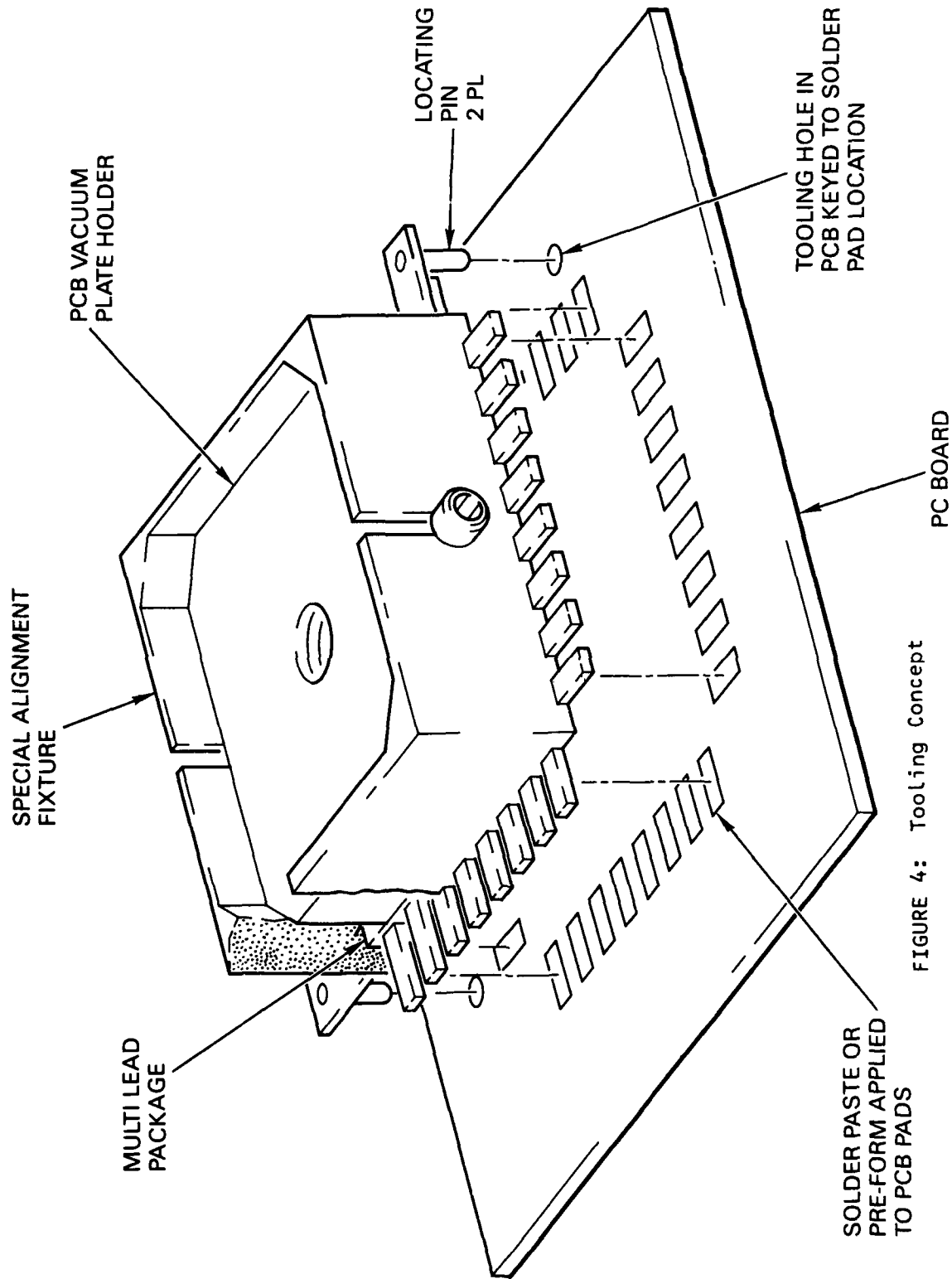


FIGURE 2: Fixture and
Vacuum Plate



FIGURE 3: Side View of Fixture.
Note Notched Cut-Outs.



NWC TP 6896
EMPF TP 0003

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SOLDER JOINT FAILURE IN LEADLESS CERAMIC CHIP CARRIERS

by

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ABSTRACT

This report describes a Control Data Corporation (CDC) Government Systems Operation's (GSO) research and development effort to improve the quality and reliability of solder joints associated with Leadless Ceramic Chip Carriers (LCCC). A detailed discussion of the effect of thermal cycling on the LCCC solder joint integrity and requirements to improve solder joint quality/reliability is addressed.

CDC GSO has been researching the design and manufacture of surface mount assemblies for the past six years. Recently, the effect of coefficient of thermal expansion (CTE) mismatch between LCCCs' and substrate materials on the LCCC solder joint integrity has been studied. The problem and the requirements for improvement have been defined. Several process/design options to improve LCCC solder joint quality and reliability in densely populated Circuit Card Assemblies (CCA's) have been evaluated, and a solution has been developed and implemented in production. This report contains results from various experiments performed to gain knowledge of LCCC solder joint reliability. Although CDC GSO conducted these research activities primarily to improve reliability of military CCAs, this technology can be used for commercial applications requiring high reliability.

INTRODUCTION

The newly developed Surface Mount Technology (SMT) with direct attachment of Leadless Chip Carriers (LCC) to Printed Wiring Board (PWB) provides a promising solution to the ever-increasing demand for high performance, smaller and lighter electronic systems, and offers the most cost effective means of manufacturing. When the successful commercial LCC technology was applied to Military electronic systems, where the CCAs are subjected to severe cyclic variations in a thermal environment, degradation in the quality, reliability and life expectancy of the solder joints was observed during exposure to thermal cycling tests. This paper discusses results from research studies which included various experiments performed to understand the effects of thermal cycling on the LCCC solder joint integrity; it also defines the problem and suggests solution requirements to improve solder joint reliability.

The purpose of the study was to correlate solder joint thermal fatigue life with solder fillet size and reflow techniques. The resulting analysis revealed two major factors in determining solder joint fatigue life for a given LCCC/PWB design: (1) CTE mismatch; and (2) solder joint configuration (various combinations of parts thicknesses, drying, and reflow sequences).

During the past ten years, major improvements in the placement of leadless components and mass soldering technology have been made. More research is needed to develop high fatigue strength joining materials, CTE and impedance-controlled substrate materials, improved component packaging technology, and high-density multilayer Printed Wiring Boards to meet the ever-increasing need for higher reliability in military electronics.

BACKGROUND

Two major attributes of the relatively new surface mount technology are increased functional density and reduced cost. The LCC packaging technology possesses both of these attributes. However, to capitalize on the improved density and cost, new assembly processes had to be evaluated and developed. Direct attachment of leadless components to PWB pads is the most effective means of assembly as well as providing the shortest connection between the active component circuit and the active PWB circuit, an essential requirement for high speed circuit performance.

The use of Surface Mount Technology (SMT) with Leadless Chip Carriers (LCC) was a natural design approach to achieve higher performance, lighter, smaller and less expensive electronic assemblies. During the past ten years, assemblies with surface mount LCCs have taken the lead in commercial electronics as the most successful approach for high density packaging in electronic systems. The concepts of Designing for Assembly (DFA) were evolving at the same time as robotic placement cells and new mass soldering methods; thereby providing even greater opportunities for cost economics when using the LCC packaging technology.

During field use of military electronic equipment, especially in airborne applications the CCAs experience cyclic variations in the thermal environment. These variations are caused by external factors, e.g., ambient temperature variations, as well as internal operational factors, e.g., system on/off cycles. In military applications, cyclic variations in the thermal environment are usually very severe and tests to simulate these temperatures variations can range from -55°C to $+100^{\circ}\text{C}$. Reliability problems develop as the solder joints undergo repeated cyclic strains induced by the thermal expansion mismatch between the PWB and the LCCC.

The design of the CCA's studied meets the requirements for a Navy Standard full ATR configuration. The 6 x 9 inch CCAs are densely populated with 0.050 pitch 20, 28 and 32 pin LCCCs and fine-pitch VLSI carriers. The heat sink is mounted either between two CCAs or just on one side of a single CCA. The cross-overs and connectors are soldered after bonding the heat sink and are mechanically fastened to the CCA. A typical module is shown in Figure 1.

EXPERIMENTAL APPROACH

The experimental portion of this study involved CTE measurements of the multilayer PWBs, soldering LCCCs to PWBs using various reflow methods, thermal cycling combined with periodic visual inspection, and failure analysis procedures. Each of these areas is discussed in the following paragraphs.

The materials used for this experimentation included .050 pitch 18, 20, 28 and 32 pin LCCCs, 6 x 9 inch (10) layer polyimide/glass test PWBs (Figure 2), heatsinks, and Sn63/Pb37 solder paste compatible with Federal Specification QQ-S-571. A typical test module is similar to the one shown in Figure 1. The PWB pad configuration for LCCCs is shown in Figure 3.

CTE Measurements

A test PWB was divided into quadrants and sectioned into .375 x .375 inch coupons. Each coupon was serialized and seven coupons from each quadrant were randomly selected for CTE measurement to allow a more accurate indication of the variation at different locations on the PWB. Measurements of CTE were made in X and Y direction using a Du Pont Model 1090 B Thermal Analyzer.

Thermal Profile of Soldering Processes

The thermal profiles of LCCC solder joints during vapor phase soldering (VPS) and hand soldering were measured using Chromel/Alumel thermocouples attached to the solder pads on the PWB. A conveyORIZED VPS machine, HTC, model IL-24, was used with 3M Fluorinert fluid (boiling point 419 °F) to vapor phase solder LCCCs. Hand soldering was performed using an 18 w soldering iron with a cone tip.

Component Preparation

The LCCCs were tinned twice using RMA flux and a wave solder machine to remove gold plating on the pads followed by cleaning using Freon TMS. The gold contamination in the solder bath was maintained at less than .5 % per military specification WS-6536-E. All LCCCs were inspected at 10 X for wetting, coverage and bridging.

Solder Paste

The solder paste, Sn63:Pb37 RMA flux, used in this study was inspected per current CDC procedure which includes tests for viscosity, particle shape, particle size, solder ball reflow, solder wetting, and metals content.

Solder Paste Printing

A controlled amount of solder paste was applied to the pwb using a semiautomatic "de Haart" printing machine equipped with two squeegees called flood and wipe, made out of hard durometer rubber (Figure 4). The squeegee pressure was controlled to produce optimal printing results.

LCC Mounting and Soldering

This study involved evaluation of five solder joint configurations and three soldering processes. The matrix of the variables is shown in Figure 5. Each of these variables is discussed briefly in the following paragraphs.

1. Process - Hand soldering

LCCC packages were soldered to the pwb using an 18 w soldering iron with a cone tip, RMA flux (MIL-F-14256) and Sn63:Pb37 wire solder (QQ-S-571). The idle tip temperature was maintained at 750 °F. After soldering, the assembly was cleaned in an in-line cleaning system using Freon TMS to remove flux residue.

2. Process - Solder paste mount and VPS

The procedure is outlined in Figure 6. The LCCCs were mounted directly on the last layer of the unreflowed solder paste on the pwb pads. A drying cycle of 75°C for 15 minutes was performed to evaporate volatile solvents in the solder paste, thus reducing the chance for solder balls during the reflow process, and the assembly was soldered using a conveyORIZED HTC model IL-24 VPS machine. After reflow, the assembly was cleaned in an in-line cleaning system using Freon TMS to remove flux residue.

3. Process - Flux mount and VPS

The procedure is outlined in Figure 7. The required amount of solder paste was applied to PWB pads, dried at 75°C for 15 minutes, and reflowed using VPS machine. RMA flux paste (MIL-F-14256) was applied to the last layer of reflowed solder paste on the pwb pads, LCCCs were mounted and soldered using the VPS machine. The solder paste held the LCCCs in position during soldering. The assembly was cleaned in an in-line cleaning system using Freon TMS to remove flux residues.

4. Solder configuration - .010 inch thick solder paste, VPS

The solder paste was applied in two steps: stencil .006 inch thick paste, dry at 75°C and reflow in VPS machine and stencil .004 inch thick paste.

5. Solder configuration - .012 inch thick solder paste, VPS

The solder paste was applied in two steps: stencil .006 inch thick paste, dry at 75°C and reflow in VPS machine and stencil .006 inch thick paste.

6. Solder configuration - .014 inch thick solder paste, VPS

The method of applying .014 inch thick paste was the same as the above iterative method. The solder paste was applied in layer thickness of .006, .004 and .004 inches.

7. Solder configuration - .016 inch thick solder paste, VPS

The solder paste was applied in layer thickness as of .006, .006 and .004 inches.

Thermal Cycling Test

The thermal cycling tests were performed using a Thermotron environmental chamber set to provide the test specimen CCA temperature profile shown in Figure 8. The temperature extremes of the profile were controlled between -55°C to +100°C with a 1.5 hour cycle time and 15 minutes dwell time at each limit.

Visual Inspection

To determine the thermal fatigue life, all LCCC solder joints were inspected at 55 X for solder joint shape and surface appearance after assembly and after 25, 50, 100, 150, 200, 250 and 300 cycles. Metallographic and Scanning Electron Microscope/Energy Dispersive X-ray (SEM/EDX) analyses were also used to determine the effects of temperature cycling.

For the purpose of this study, a description for three solder joint sizes and three stages of solder joint degradation were developed. Even though not technically rigorous, these definitions were adequate for trained inspectors to collect data that could be analyzed in graphical form thus yielding useful analytical results. The solder joint size is a direct function of the amount of solder paste applied to the pwb. Three stages of solder joint degradation were defined as stress mark, stress crack, and crack, and will be discussed at length in the paragraphs below.

RESULTS AND DISCUSSION

Coefficient of Thermal Expansion

The average CTE values of the ten layer polyimide/glass pwb in the X and Y directions, measured between 40 and 110 °C, were found to be 18 PPM/°C and 17 PPM/°C, respectively. The CTE mismatch between the pwbs and the LCCCs (average CTE of the ceramic package = 6 PPM/°C) is approximately 12 PPM/°C, and causes stresses greater than the maximum shear stress of both solder when joints in circuit card assemblies are exposed to the temperature extremes (-55°C to 100°C) used in this study.

Soldering Thermal Profile and Grain Structure

The thermal profiles of the soldering operations, VPS and hand soldering, are shown in Figure 9. The LCCC solder joints made using hand soldering cool very rapidly (approximately 120°C per second) and those reflowed using the VPS reflow method cool very slowly (approximately 1°C perth cond). The grain structures of solder joints, corresponding to these two methods of heating, are shown in Figure 10.

In the hand soldering process, only the solder, the solder pad on the PWB and the contact area of the LCCC are elevated in temperature, while the surrounding region of comparatively very large mass is relatively cold. This cools the solder joint very rapidly producing very fine solidification structure with an uniform distribution of tin and lead concentration.

In contrast, the VPS process raises the temperature of the entire CCA to 419°F, allowing all the solder to reflow. The CCA cools as it travels on the conveyor to return to ambient temperature. The slow cooling rate due to the very large mass of the CCA produces a coarse solidification microstructure and produces joints having a surface texture characterized as slightly rough, grainy and striated. It is generally considered that an alloy of coarse microstructure is inherently weaker than one of the same constituency but with a finer grain structure.

Voids in Solder Joint

X-ray analysis was used to evaluate CCAs for voids in the solder joints. The paste mount process (apply LCCC's directly on solder paste while tacky and then reflow) produced a large number of voids relative to the flux mount process (reflow solder paste, mount LCCC's on tacky flux and reflow). It was found that the overwhelming majority of large (> 0.0005 inch) voids were located between the LCCC pads and pwb solder pads, while the fillets near the LCCC castellations contained very few small voids. It was also observed that the application of the required amount of solder by "multiple stencil and reflow" process (Figure 6 and 7) minimizes formation of entrapped voids.

It is generally considered that voids in solder joints are produced by gasses generated due to decomposition of the flux during heating and reflow and represent a source of solder joint weakness. The voids may form nucleation sites for fatigue cracks and speed up failure.

Three Stages of Solder Joint Degradation

A stress mark, shown in Figure 11, is the earliest indication of failure during temperature cycling and is characterized by the appearance of several faint lines extending across the surface of the fillet near the castellations. The surface of the solder joint changes to a grainier, non-uniform condition due to internal changes such as grain coarsening and slippage of eutectic colony boundaries occurring in the microstructure of the solder.

Upon continued thermal cycling, stress marks evolve into stress cracks as shown in Figure 12, and are characterized as relatively more pronounced (and greater in number) lines on the solder surface. The lines have developed to an extent that the microscope light casts shadows in the crevices created. Observation at high magnification reveals that the solder has begun to cleave with some lateral shift of material on either side of the crack. This type of degradation may be detected as an intermittent electrical open during rigorous vibration.

Figure 13 shows the condition defined as a totally electrically open crack, in other words, a catastrophic solder joint failure. It is seen that the solder has completely separated with noticeable lateral shift of material on either side of the crack. This joint may appear intermittently open at moderate vibration levels or with rapid thermal change.

Cross Sections

Numerous solder joints having various stages of degradation after thermal cycling were cross sectioned for study. Figure 14 shows one such cross section. The sample reveals coarse microstructure at the crack tip with Pb-rich (alpha) and Sn-rich (beta) phases. The strain produced by the CTE mismatch among the three materials (LCCC, pwb and Sn63:Pb37 solder) during thermal cycling increases local coarsening of the microstructure in the solder, which, in turn, increases the tendency towards crack formation in the weak lead-rich (alpha) region. The coarsest microstructure represents the highest strain areas in the solder joint. It is believed that this is the same failure mechanism, strain-induced grain coarsening, reported by Yenawine and Wolverton.¹

The cross sections of solder joints that displayed no outward appearance (stress marks or stress cracks) of degradation after thermal cycling did, however, show evidence of the beginnings of solder joint cracks. These observations show where the shear forces first affect solder joint integrity and led to the conclusion that the solder joint failure usually begins at a point farthest from the fillet surface, under the LCCC, and proceeds toward the front edge of the LCCC. With continued thermal cycling, the crack then proceeds upward (approximately 50° to 60°) to the surface of the solder fillet, thus completing the solder joint failure.

Thermal Cycling Results

The size of the LCCC package itself is another factor that heavily influences the thermal fatigue life of solder joints. It was observed that for a given solder fillet size, solder joints on a 32-pin rectangular LCCC failed before those on a 28-pin square LCCCs, and those solder joints on a 28-pin square LCCCs failed before those on a 20-pin square LCCCs. It was also observed that the solder joints on the corner pins were the first to degrade, then the next toward the center, and so forth.

Hand soldered joints, with their inherently fine grained structure, exhibited relatively better thermal fatigue life than VPS joints. However, when compared to the number of thermal cycles required for long term reliability, the improvement over the performance of the coarse-grained joints produced by the vapor phase process is inadequate. The flux mount process minimized formation of entrapped voids, and apparently improved strength of the solder joint. However, this process modification also did not significantly improve thermal fatigue life of the LCCC solder joints. The solder fillet size was the most significant factor in determining the thermal fatigue life for a given LCCC/pwb design. The small solder joints degraded and cracked first, medium joints cracked next, and the large (bulbous) joints cracked last. The bulbous fillet, produced by 0.016 inches of solder paste, showed an increase in thermal fatigue life.

Thermal cycling tests are currently being performed on LCCCs soldered to a pwb with a Copper/Invar/Copper (CIC) constraining layers (average CTE = 13 PPM/°C). Preliminary test results show a significant increase in the thermal fatigue life.

CONCLUSIONS AND RECOMMENDATIONS

As a result of this study, it is concluded that two major factors determine solder joint thermal fatigue life for a given LCCC/pwb design, namely, the relative TCE's and the solder joint size/shape. The bulbous (large) fillets increase thermal fatigue life of the solder joints. However, for a CCA design with a three-to-one or greater CTE mismatch, it is concluded that, any solder joint on an LCCC, regardless of package size, fillet size, or reflow techniques, will show significant degradation in quality, reliability and life expectancy when the CCA is applied in a thermal cycling environment.

The following considerations need examination to assure solder joint reliability of CCAs which are applied in severe cyclic thermal environments:

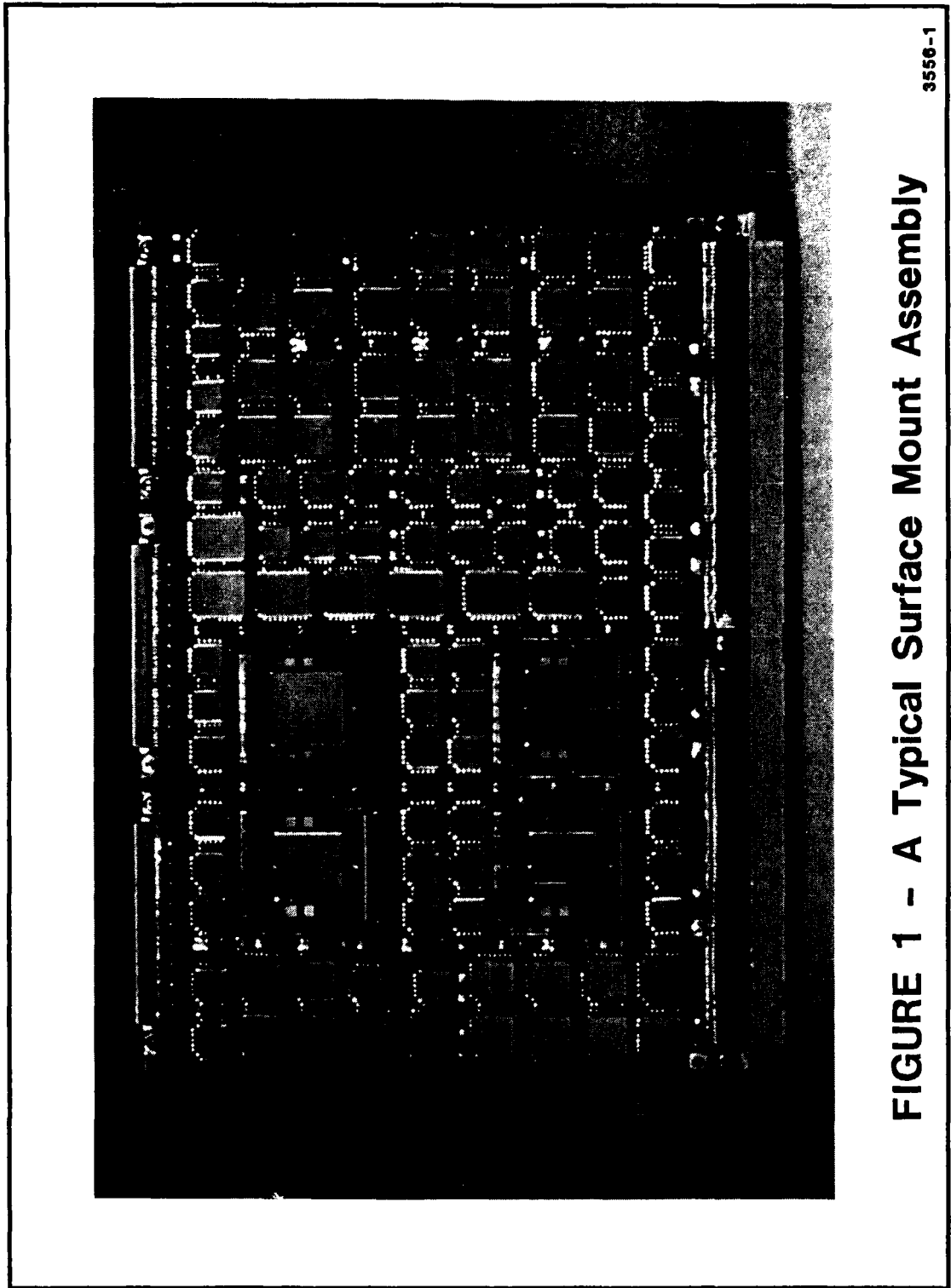
1. A strain-accommodating interface for interconnecting LCCCs to pwbs.
2. Minimization of TCE mismatch between the LCCC and pwb.
3. Fatigue strength of joining materials.

ACKNOWLEDGMENT

The authors wish to thank R. Kraus, R. Thomas, S. Axdal, F. Chen, D. Jeranson and J. Dierke for helpful technical assistance.

REFERENCE

1. Roy Yenawine, Mike Wolverton, Alan Burkett, Barbara Waller, Bill Russell and David Spitz. "Today and Tomorrow in Soldering" 11th Annual Electronics Manufacturing Seminar, 18-20 February 1987, Sponsored by Electronic Manufacturing Program Office and Soldering Technology Branch, Naval Weapons Center, China Lake, Ca.



3556-1

FIGURE 1 - A Typical Surface Mount Assembly

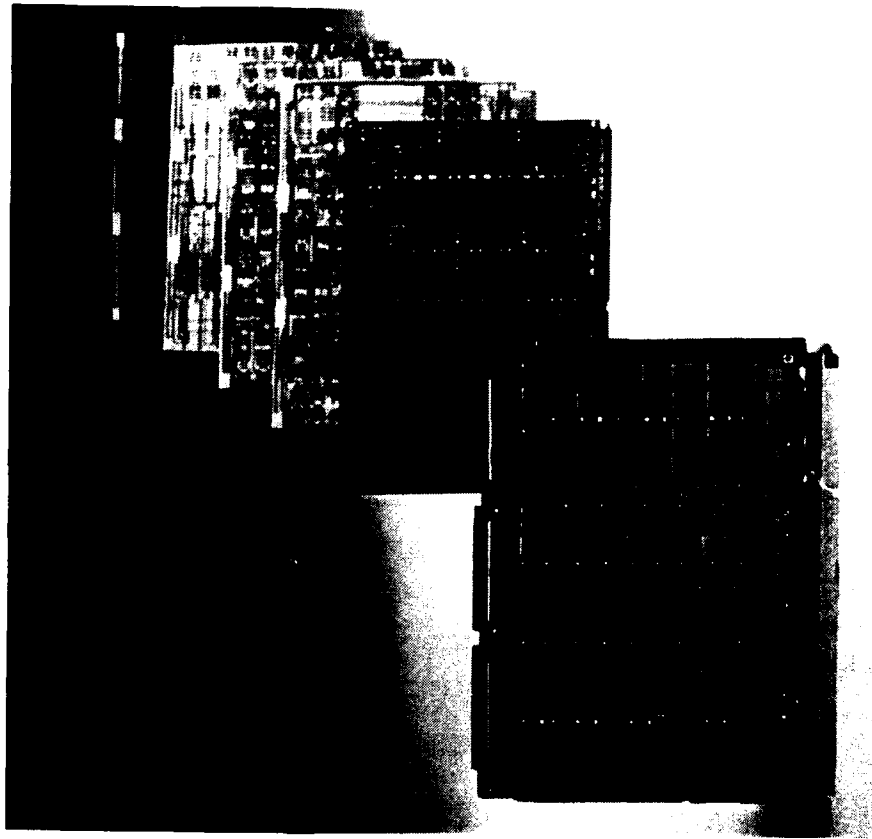
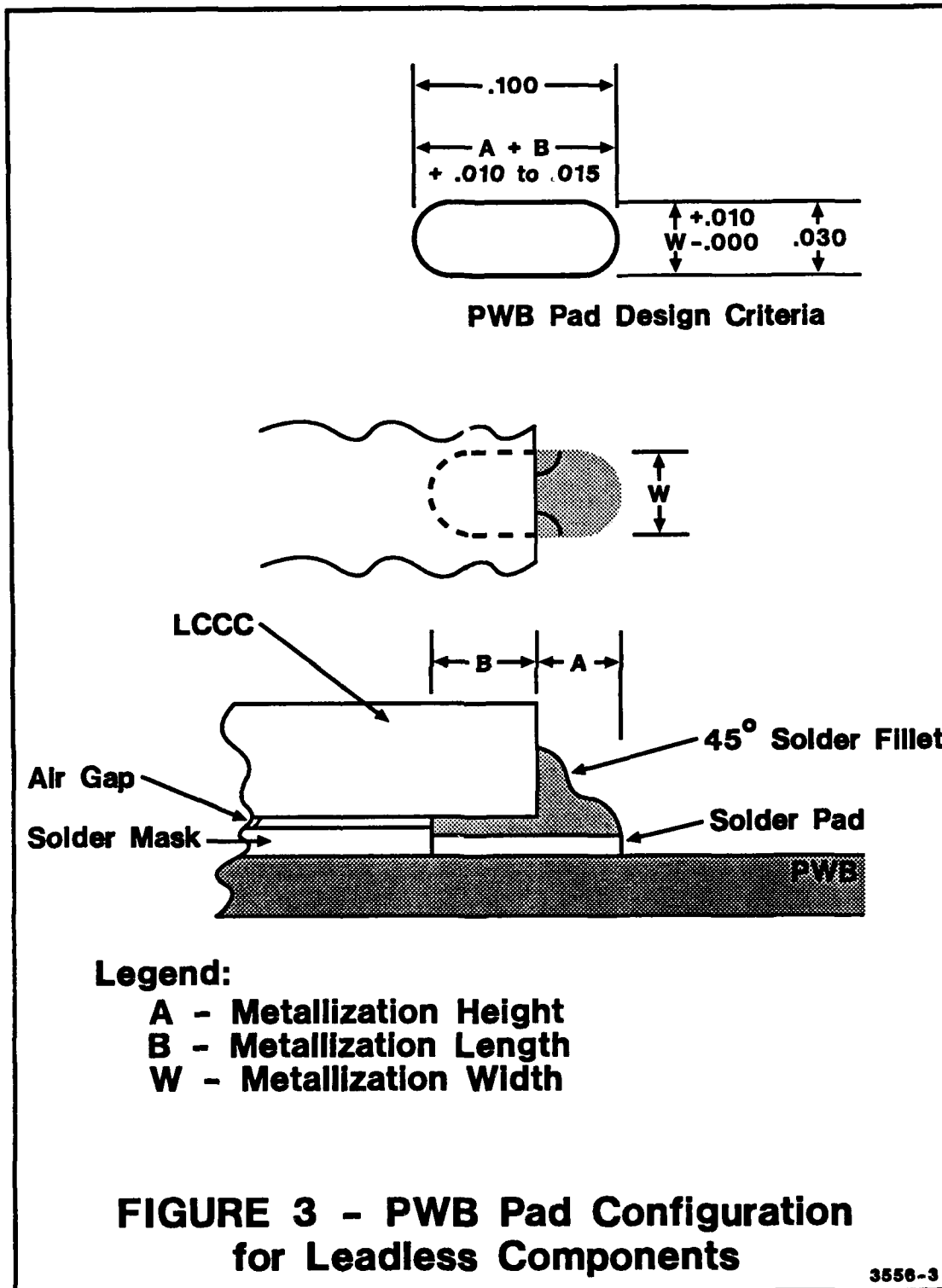


FIGURE 2 - Polyimide/Glass Multilayer PWB

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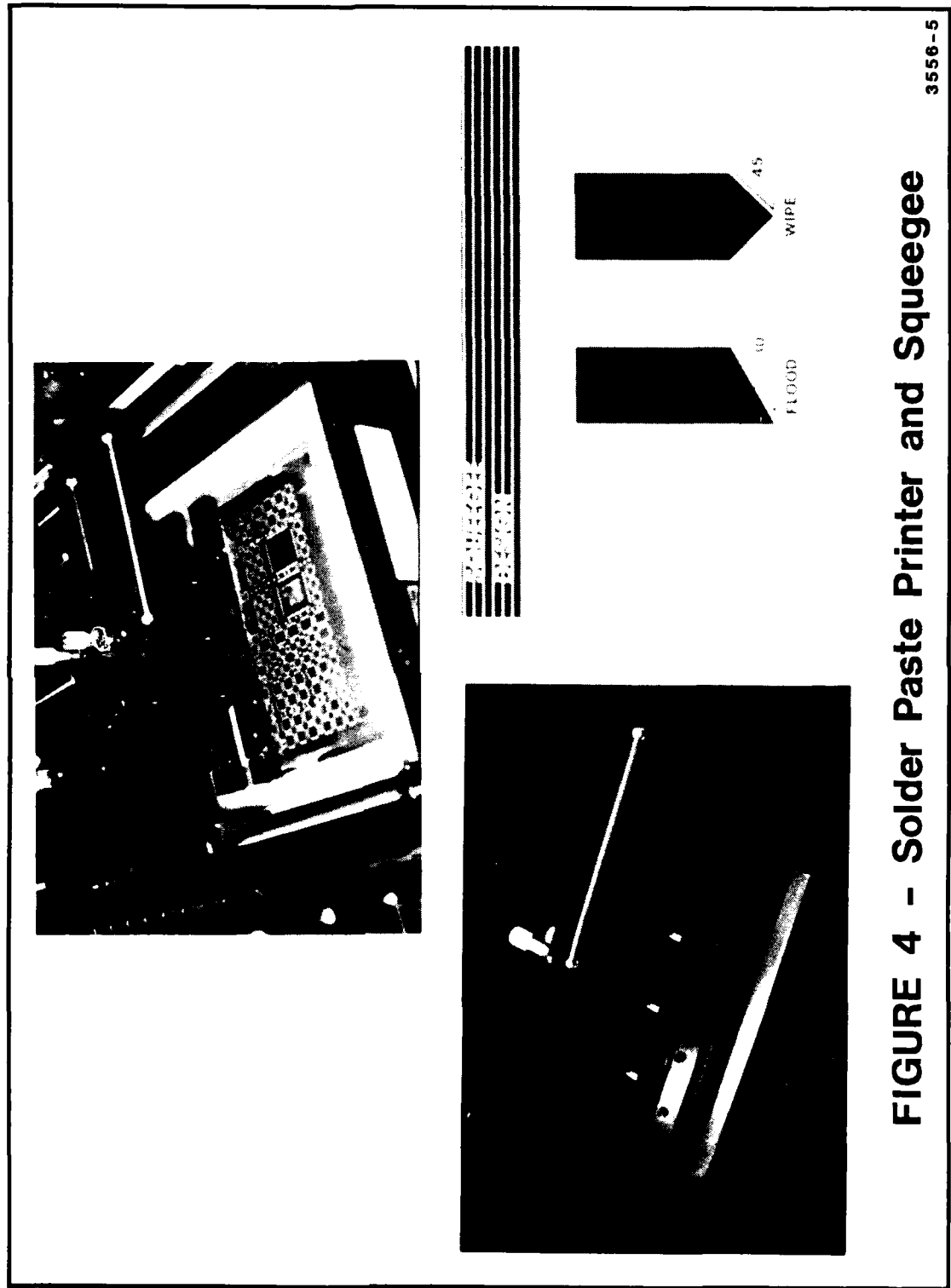
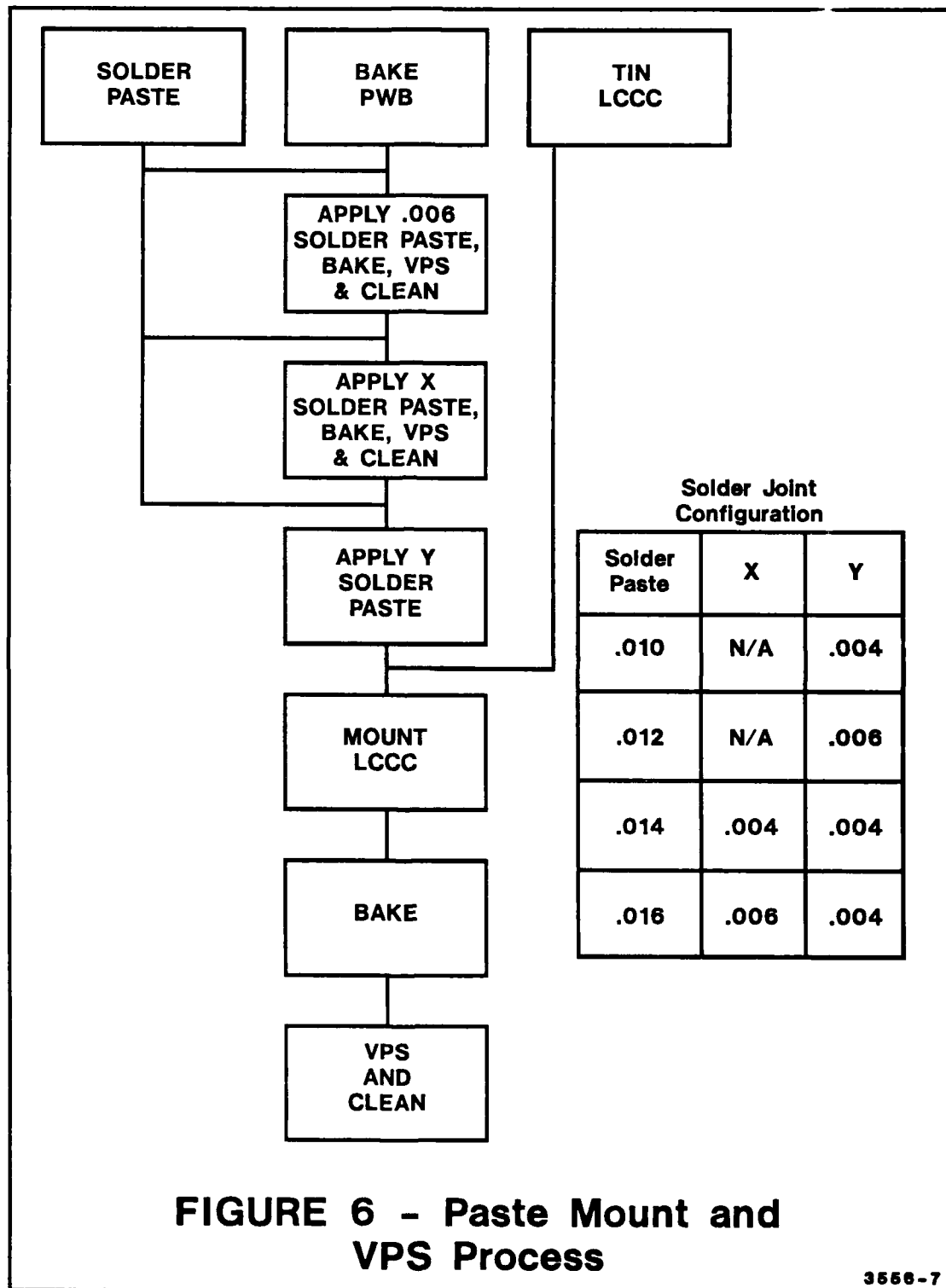


FIGURE 4 - Solder Paste Printer and Squeegee

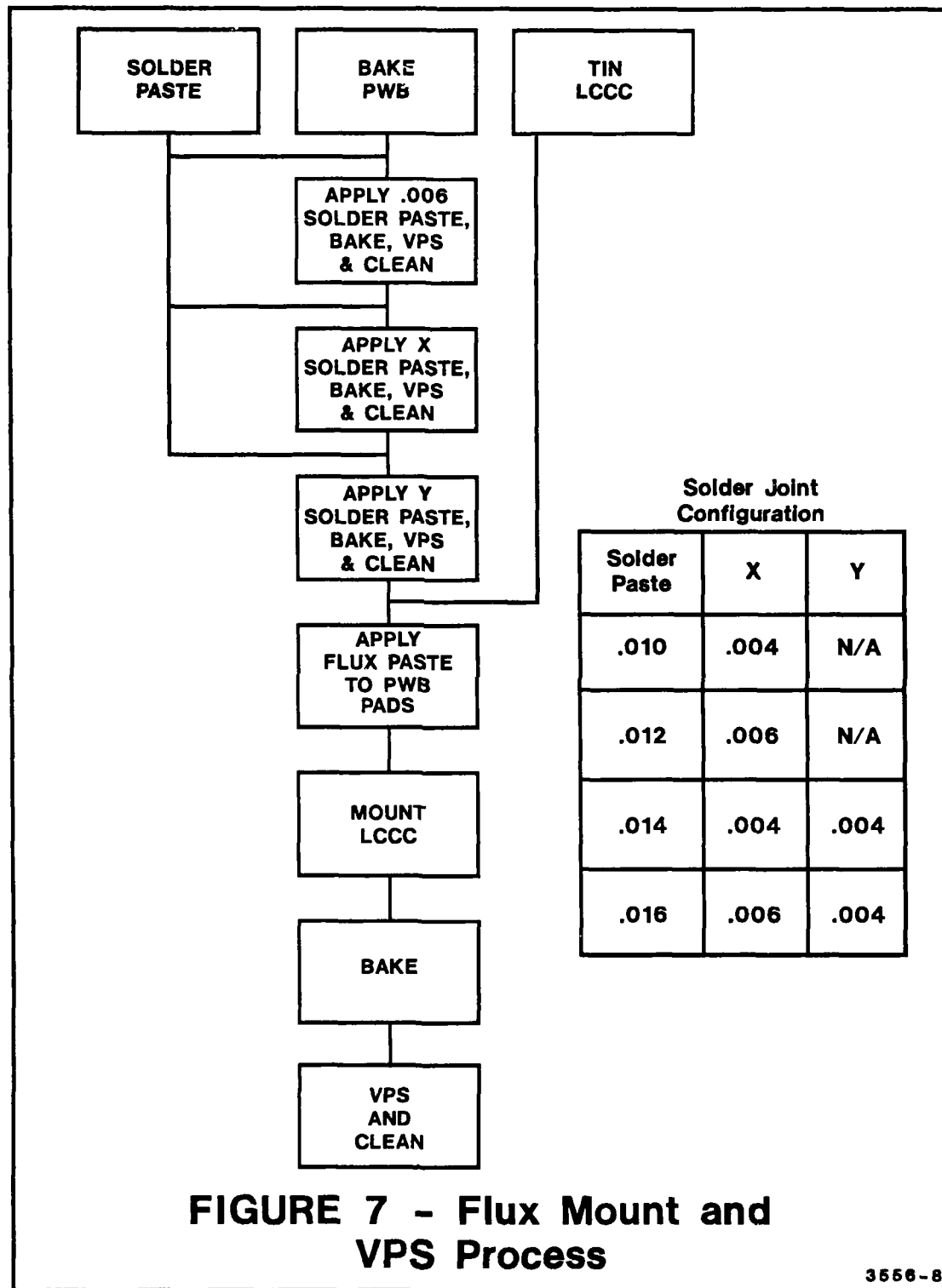
Solder Joint Configuration					
Soldering Process	Wire Solder	.010 Thick Solder Paste	.012 Thick Solder Paste	.014 Thick Solder Paste	.016 Thick Solder Paste
	Hand Solder				
	Paste Mount and VPS	X	X	X	X
	Flux Mount and VPS		X	X	X

FIGURE 5 - LCCC Soldering Variables Matrix

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3556-7



3556-8

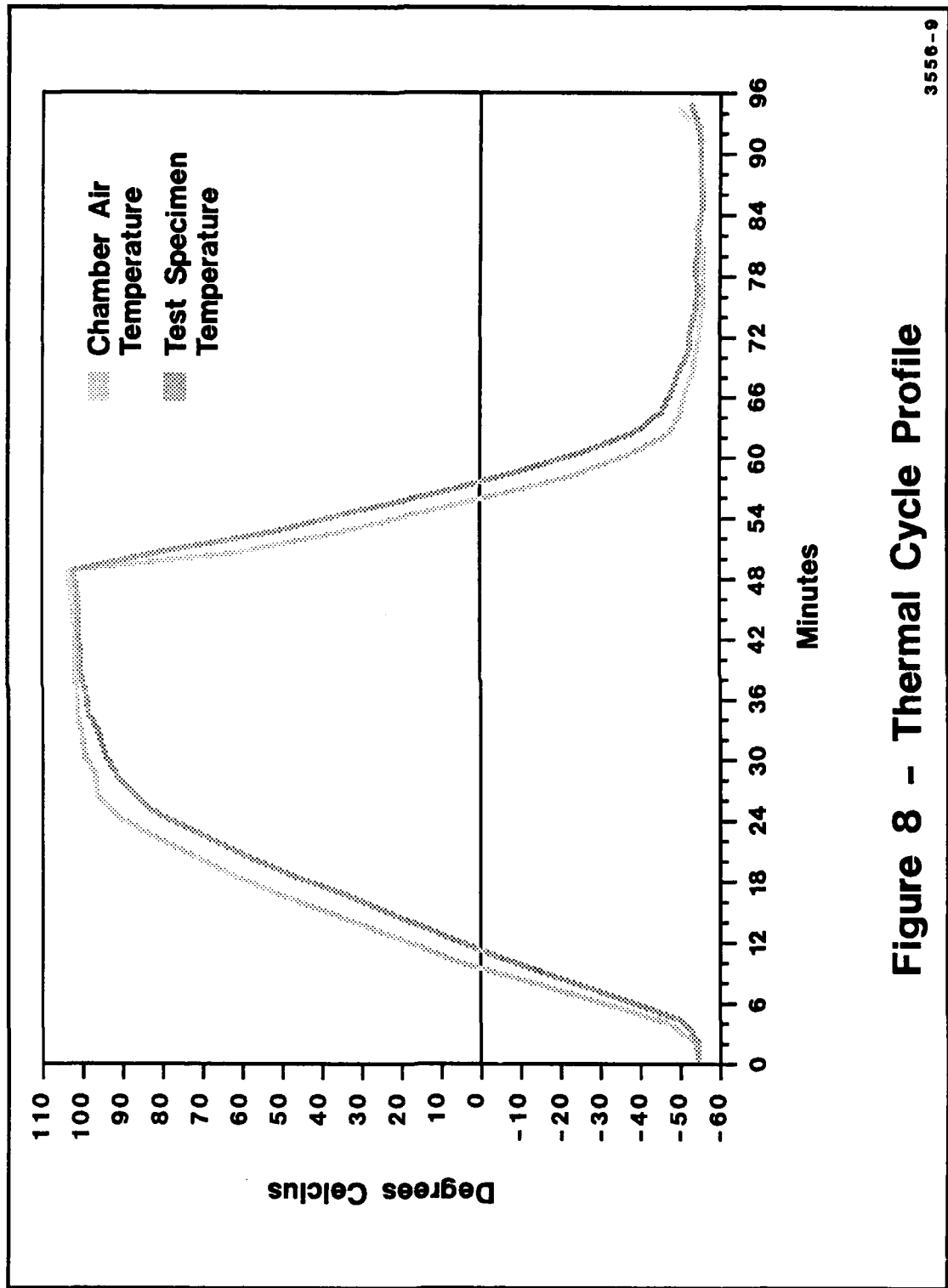


Figure 8 - Thermal Cycle Profile

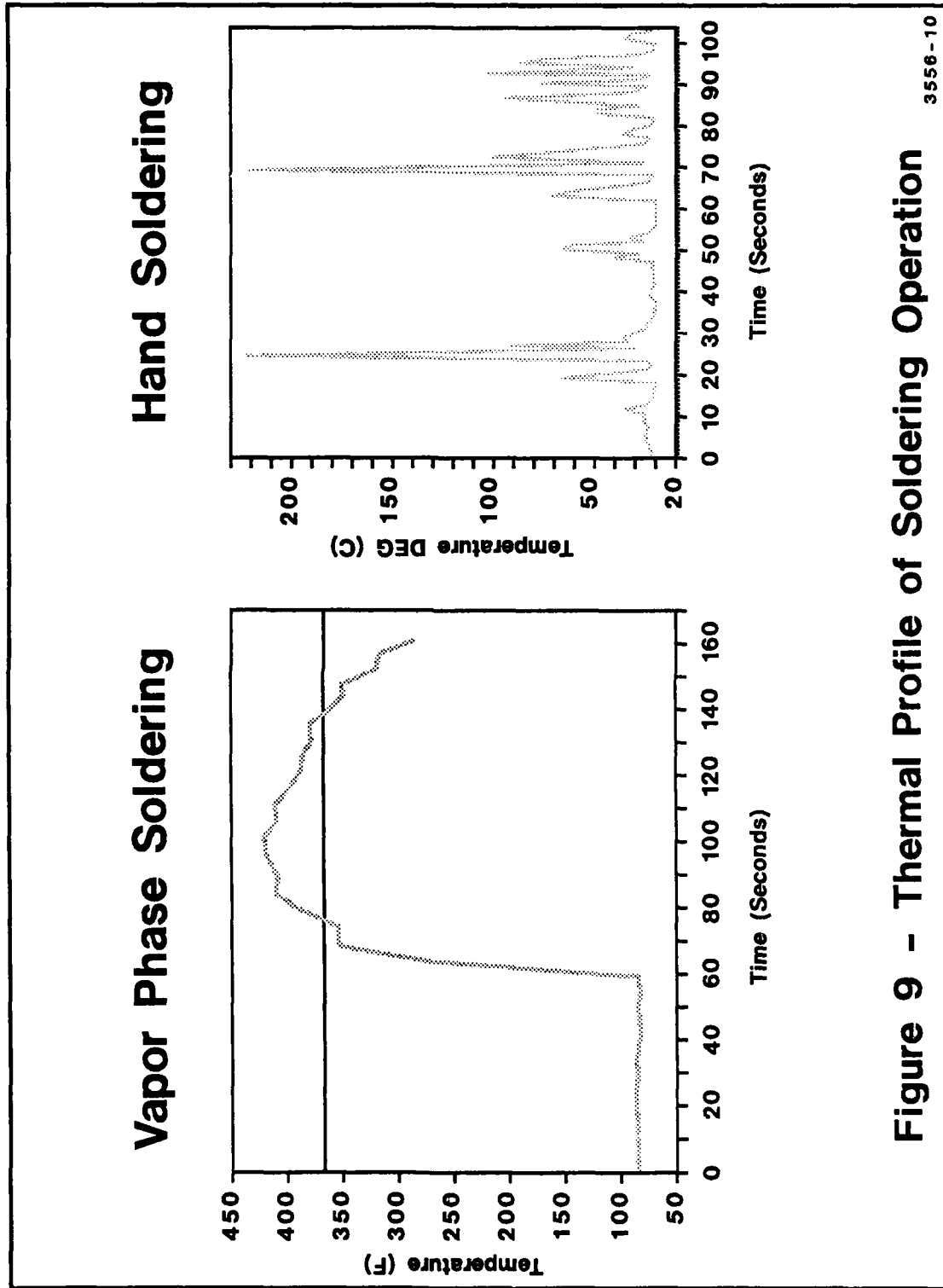
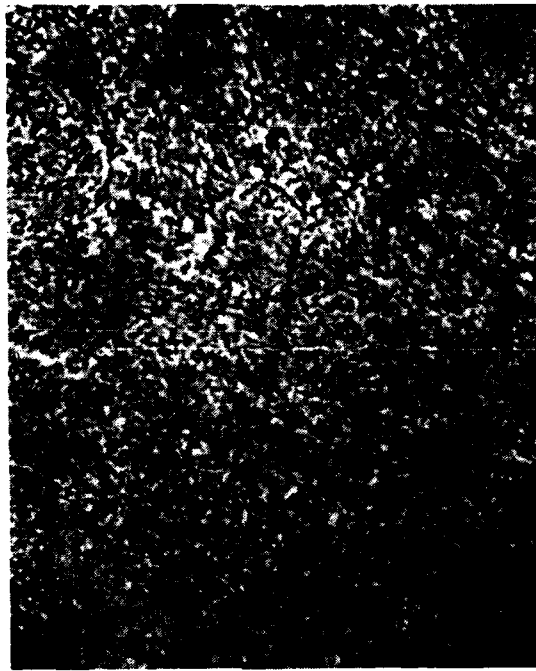


Figure 9 - Thermal Profile of Soldering Operation



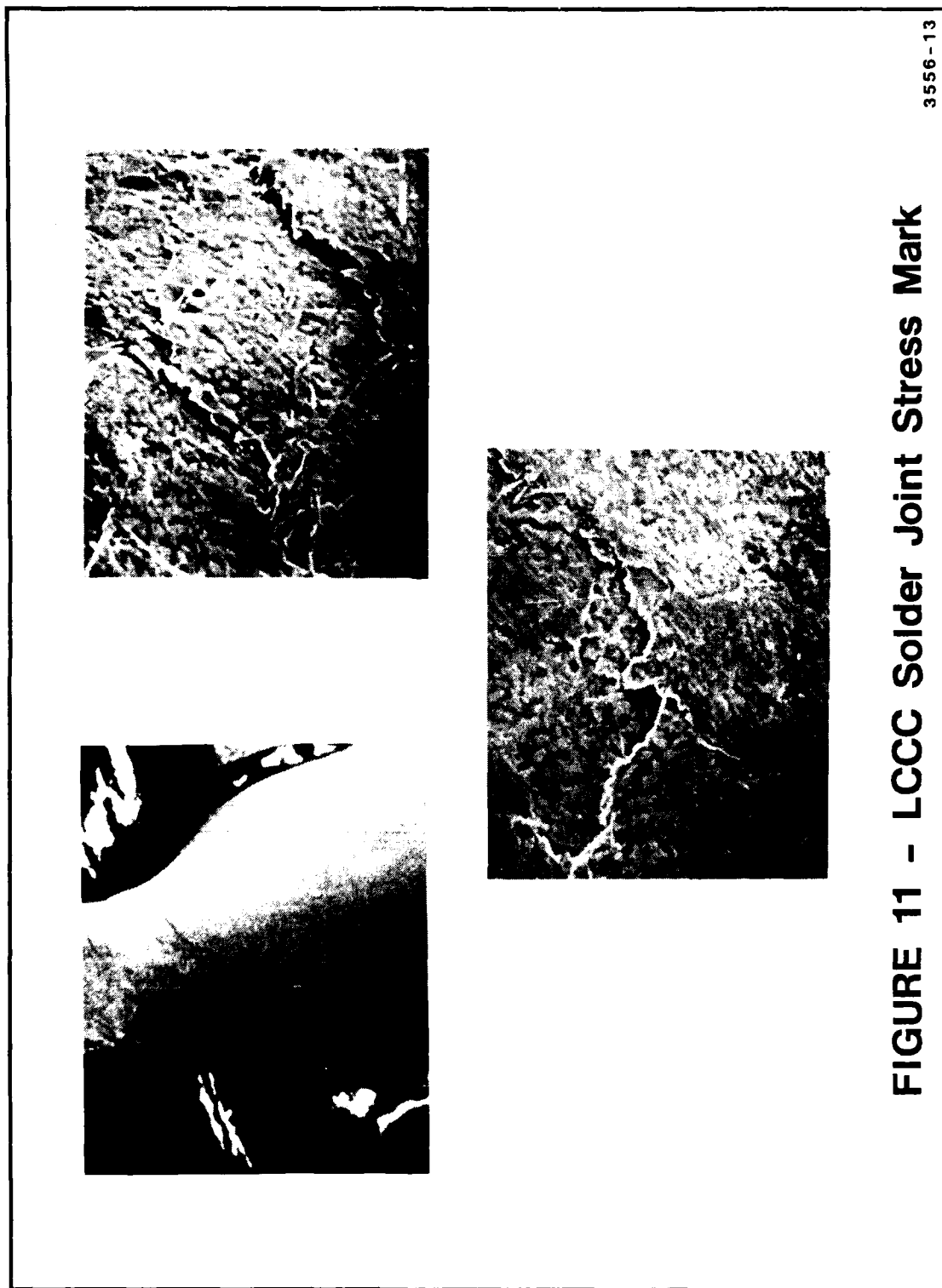
Hand Solder Joint



Vapor Phase Solder Joint

FIGURE 10 - Grain Structure of LCCC Solder Joint

3558-12



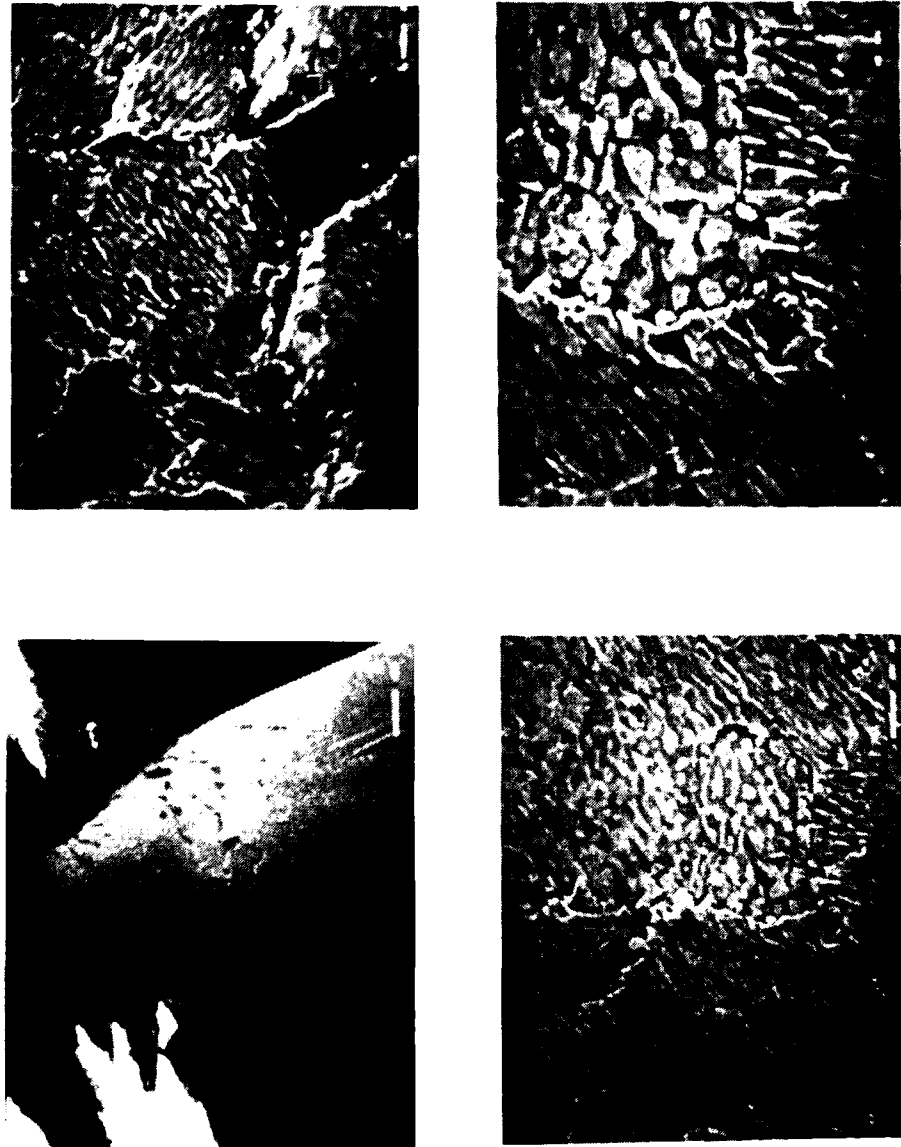


FIGURE 12 - LCCC Solder Joint Stress Crack

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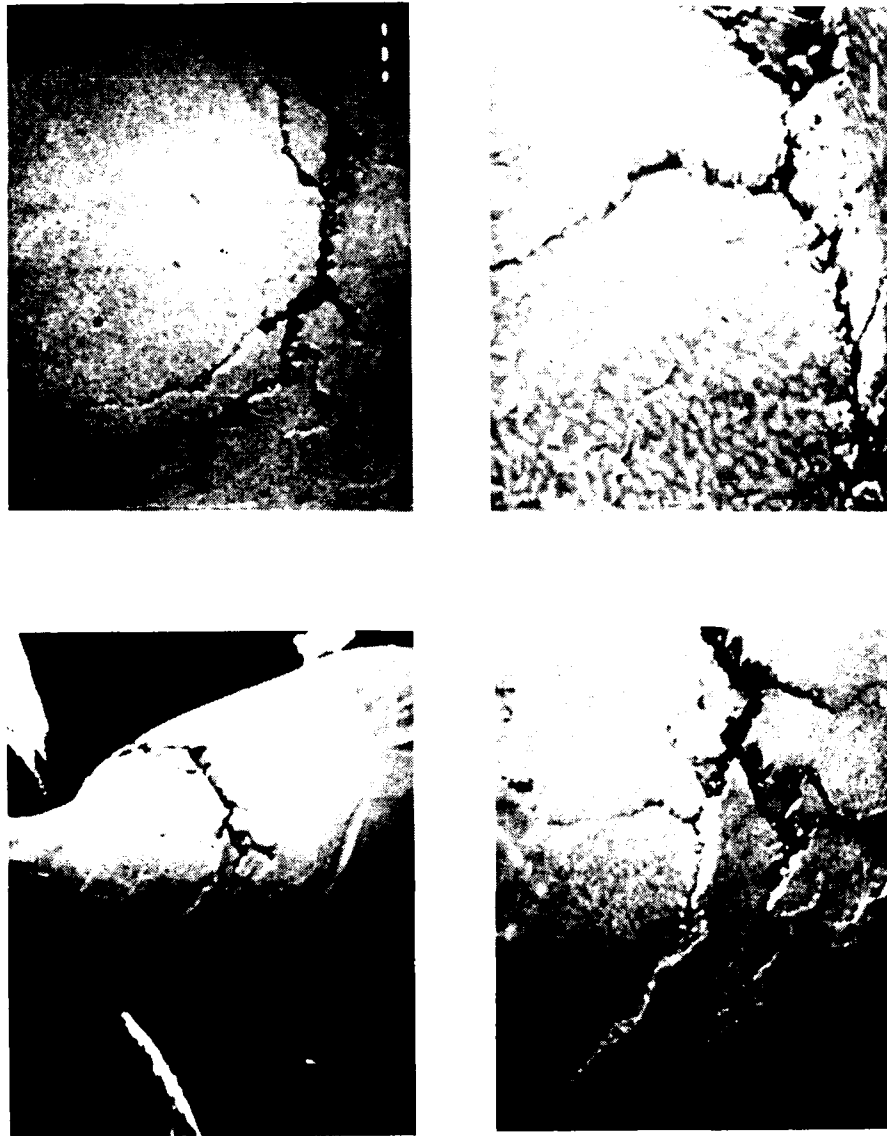


FIGURE 13 - LCCC Solder Joint Crack

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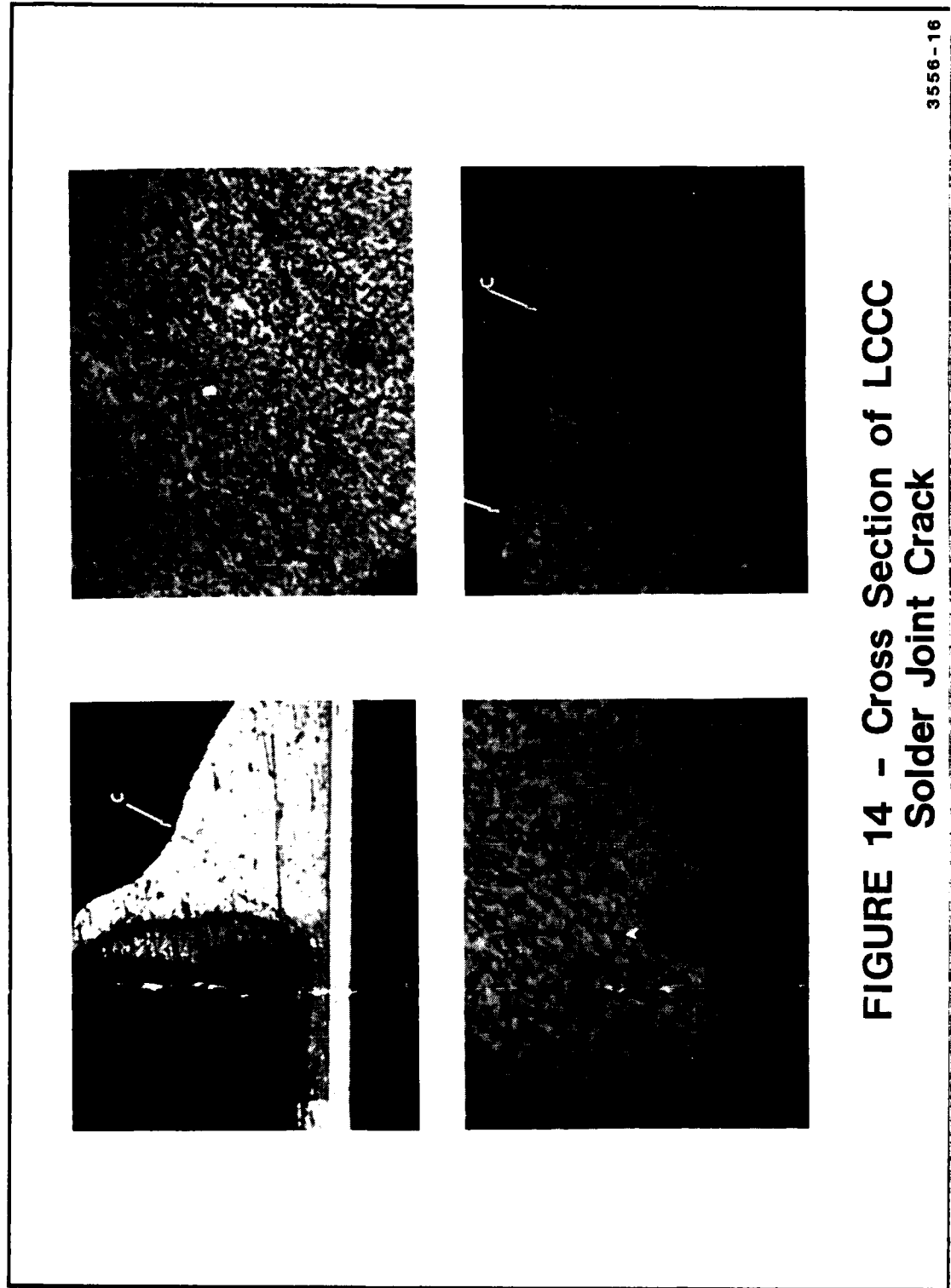


FIGURE 14 - Cross Section of LCCC
Solder Joint Crack

3556-16

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**SOME FACTORS AFFECTING LEADLESS CHIP CARRIER
SOLDER JOINT FATIGUE LIFE II**

by

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ABSTRACT

This paper will review some continuing IBM study efforts conducted on surface mounted Leadless Chip Carrier (LCC) packaging for use in high density, high thermal stress military environments. The paper will present some designs, materials and solder joint processing considerations that can effect solder joint fatigue life. Also discussed will be some thermal cycling test limitations, some important properties of solder failure mechanisms and finally some technical concerns with both WS 6536E and DoD 2000 specifications as to their limitations with future surface mounted technologies.

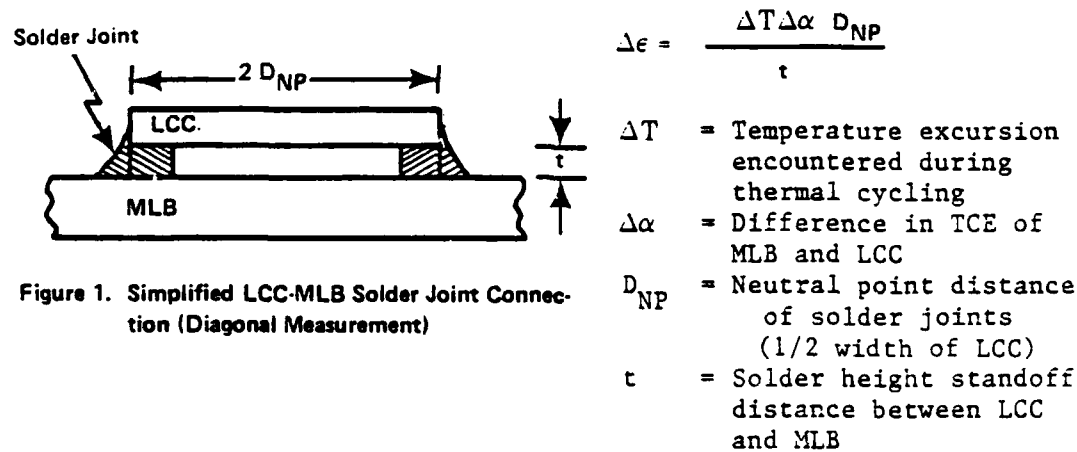
INTRODUCTION

Leadless chip carriers (LCCs) are becoming increasingly used in military applications as they offer significant reductions in packaging size as well as electrical improvement over many presently used electrical components. In addition, they are capable of fairly high speed automated assembly techniques. There are however, some thermal cycling fatigue life limitations for both LCC solder joints and in some design cases, the printed wiring board (PWB) plated-through-hole (PTH) connections. These limitations must both be understood and controlled in order to provide a reliable product for the intended use military applications.

This paper will discuss some packaging designs, various material and processing effects, thermal cycling optimization and limitations, in addition to some thermal cycling and mechanical fatigue experiments. This paper will also discuss basic failure mechanisms and concerns with some requirements of present DoD specifications.

Some Packaging Considerations:

As previously discussed, a major concern with using LCCs packaging in the more severe military applications is the cyclic fatigue limitations of the LCC solder joint connections. Many of the present and proposed LCC packages are specifically designed to reduce the total solder joint strains that will occur in thermal cycling. The following very simple model (Figure 1) can be used to obtain a rough estimation of LCC solder joint thermal cycling strains in various thermal applications. Figure 2 shows an LCC epoxy glass assembly with the Thermal Coefficient of Expansions (TCE) of the various materials used in a typical assembly (α).⁽¹⁾



For optimum thermal cycling fatigue life of the LCC solder joints, emphasis throughout industry has been placed primarily on minimizing the TCE difference between the MLB and LCC ($\Delta \alpha$). Solder joint design has also been under close evaluation, including joint configurations and solder alloys.

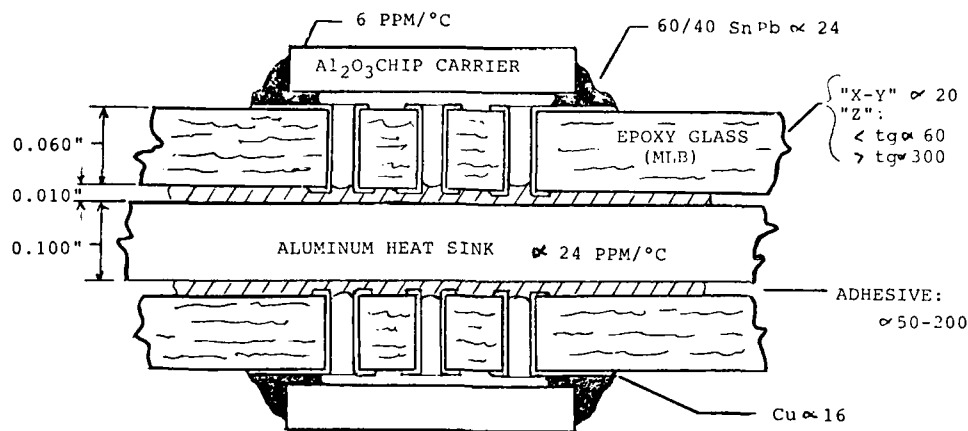


FIGURE 2 - TYPICAL LCC/MLB ASSEMBLY
(Expansion Differences)

The difference in TCE ($\Delta\alpha$) between the LCC and MLB designs can be reduced by one or more of the following technologies.

Compliant Designs:

Where a low expansion inorganic or organic system is used to better match the TCE of the MLB assembly to the low expanding Al_2O_3 LCC. An example of the organic system is Kevlar®/epoxy or Kevlar/polyimide where the negative or zero expanding Kevlar fibers are used within the MLB to produce a lower expanding MLB substrate material. Quartz fibers can also be used to restrain the MLB expansions in the "X" and "Y" board directions. An inorganic application is the use of a low expansion thick film ceramic or porcelainized metal substrate to better match the substrate TCE to the LCC modules.

Constrained Designs:

Which use low expansion materials either in the MLB as a composite or as a substrate frame bond material to again reduce "X" and "Y" board expansions. The most commonly used materials are copper laminated INVAR (CIC), Molybdenum or graphite epoxy frame materials.

Unconstrained Designs:

Which correct for differences in TCE by using greater flexibility in either the solder joint or by using leaded chip carriers. Differences in applied strains may also be reduced by the use of a more resilient surface layer on the MLB. The general trend in industry is to use leaded chip carriers where the design or environment is very severe and leadless chip carriers for the milder design applications.

SOLDER JOINT METALLURGY

Good control of both solder composition and microstructure during LCC attachment are considered important as to optimizing solder joint fatigue life. We believe that it is very important to insure that LCC modules are pretinned (solder dipped) to prevent possible gold embrittlement of the final solder connection. Intermetallic compound contamination due to rework operations are not normally considered detrimental if the rework processes are reasonably controlled.

Various studies (2)(3)(4)(5) have shown improvements in solder fatigue life with a finer alloy solder joint grain structure which would provide more uniform solder joint deformations in severe thermal cycling environments.



A LARGE GRAIN SIZE REDUCES FATIGUE LIFE DUE TO EASIER GRAIN BOUNDARY SLIPPING

(FAILED < 50 CYCLES)



FINE GRAIN STRUCTURE PROVIDES BETTER FATIGUE LIFE DUE TO MORE UNIFORM PLASTIC DEFORMATION

(NO FAILURES TO 300 CYCLES)

FIGURE 3

GRAIN SIZE EFFECT ON 63/37 SnPb FATIGUE LIFE
(-55°C to 71°C Cycling)

Solder joint deformations in thermal cycling normally takes place through plastic slip deformation along the grain boundaries in the solder. A coarse (larger) solder grain structure, which is normally produced by slower solidification rates will create faster and more severe fatigue damage as plastic strain deformation will concentrate along the larger and weaker grain boundaries of the solder (Figures 3 and 4). The most common LCC

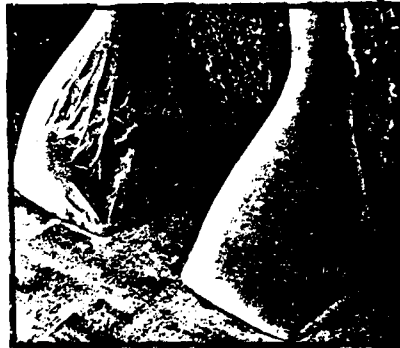


FIGURE 4 - LCC SOLDER JOINT "SOLIDIFICATION" EFFECTS

- a) shrinkage patterns
 - slow cooling
- b) smooth-shiny joint
 - fast cooling

reflow joining processes (Vapor Phase, IR, etc.) are not considered optimum as to optimizing the solder grain structure and appearance of the solder as the normal reflow solidification rates are inherently extremely slow ($1-2^{\circ}\text{C}/\text{sec}$) when compared to wave or hand soldering operations. Carefully controlled forced cooling of the assembly after vapor phase soldering has been found to be a feasible method to reduce grain size of the vapor phase reflowed solder joints. This is presently, however, a conflict with some DoD specifications which do not at this time allow any forced cooling in soldering. Some recent solder rework experiments have also shown that excessive rework heating can be detrimental to LCC solder joint fatigue life, primarily due to extremely slow solder solidification (cooling) rates. In addition to larger grains there can be excessive precipitation and growth of lead (Pb) rich phases in the solder alloy during this very slow cooling. These large grain boundaries and concentrations of extremely soft and weak

lead phases are very prone to crack propagation in fatigue stressing applications.

Substantial experiments have been made throughout industry and IBM to find a more fatigue resistant solder alloy; however, except for the very ductile Indium alloys which must be used with great care, due to corrosion and migrational concerns, no other alloy shows significant improvements over the present 60/40 SnPb or Eutectic SnPb system. Generally, one would select a more ductile solder alloy for fatigue enhancements as the stronger alloys lose their strength benefits in thermal cyclic "creep" applications. IBM Owego generally uses 60/40 SnPb alloy over eutectic SnPb alloy for LCC fatigue applications as the 60/40 SnPb alloy shows better ductility both at higher temperatures and at lower thermal cycling strain rates. Some mechanical and fatigue comparisons are shown in Figure 18.

Thermal and mechanical fatigue testing over the last several years has shown that a uniform large (bulbous) solder fillet configuration will greatly extend LCC solder joint fatigue life (Figure 5). Fatigue crack propagation up through the larger solder fillet configurations are normally very slow due to reduced strains near the surfaces of the larger solder fillets. A uniform solder configuration around the module also produces lower and more uniform thermal strains as the TCE neutral point distance (D_{NP}) of the LCC module remains in an optimum centered position. Very large fillets on one side of the module will shift the TCE neutral point distance with resulting higher thermal cycling strains with the smaller or weaker solder joints. IBM has established and uses the LCC solder joint criteria shown in Figure 5.

Extensive evaluations by IBM and other manufacturers has shown that gaseous solder voids under the LCC module has no significant effect on resulting solder joint fatigue life as, 1) stress concentrations in these small void areas are generally very low (with < 25% void area) and 2), we consider the fillet areas of the LCC solder joint to be much more critical as to fatigue reliability of the solder connection.

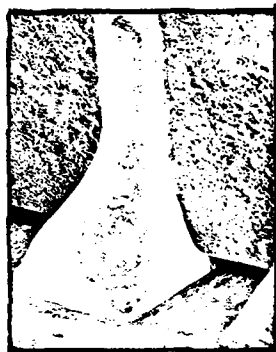


"A" JOINT



"B" JOINT

UNACCEPTABLE (SMALL) LCC SOLDER JOINTS

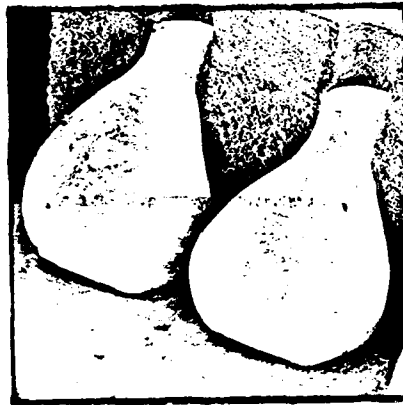


"C" JOINT



"D" JOINT

ACCEPTABLE LCC SOLDER JOINT CONFIGURATIONS



LCC "E" SOLDER JOINTS

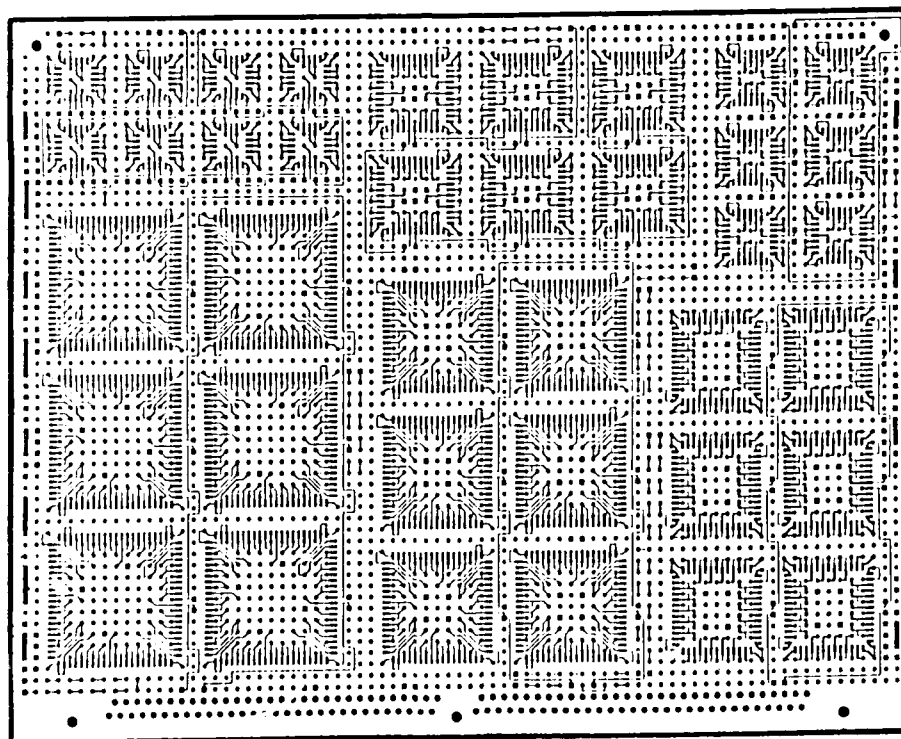
Joint unacceptable as to:

- o Lack of dielectric separation
- o Inadequate wetting evidence to pad

FIGURE 5 - LCC SOLDER JOINT FILLET CONFIGURATIONS

LCC THERMAL CYCLING LIFE TESTING

A number of engineering evaluations over the last several years has shown a need for further improvement in LCC solder joint fatigue life over the basic epoxy glass MLB system for some specific designs and for some specific military applications. The test vehicle used for most of these evaluations (Figure 6) provides both LCC solder joint and MLB PTH continuity circuits that are quite accurate for these type studies. The test hardware was assembled using standard solder paste screening and vapor phase reflow soldering techniques. No LCC standoff techniques were used in these experiments. The normal standoff height of the LCC module from the MLB was typically 0.001" to 0.003". A "C" to "D" type solder joint configuration (Figure 5) and 60 Sn 40 Pb solder was used to assemble the LCCs to both the epoxy glass and lower expanding epoxy-Kevlar MLBs. The test LCCs range in size from 20 IO to 84 IO modules. The MLBs used in these evaluations were assembled with 12 copper layers (0.080" thick), with 0.024" diameter PTHs, and 0.0018" thick PTH copper barrel plating.

**FIGURE 6 - LCC ASSEMBLY TEST VEHICLE**

The epoxy-Kevlar MLBs were soft bonded to a 0.100" thick aluminum frame while the epoxy glass MLBs were hard bonded to the aluminum frames. Typical "X" and "Y" surface TCE of the tested MLBs was ~ 21 ppm/ $^{\circ}$ C for the epoxy glass assemblies and ~ 10 ppm/ $^{\circ}$ C for the epoxy-Kevlar assemblies.

The epoxy-Kevlar compliant restraining MLB designs were of significant interest in this study, as it has a distinct weight and assembly advantage over several other MLB designs while still providing lower surface expansions for improved LCC solder joint fatigue life. This design is also not considered as detrimental to PTH reliability as previously found with some of the lower expansion designs, i.e., severe restraint of "X" and "Y" expansions can redirect higher TCE of the MLB into the "Z" axis of the MLB with substantial reduction in PTH barrel thermal cycling reliability.

Thermal Cycling Profiles:

Two thermal cycling tests were used in this experiment (Figure 7). The more severe engineering (-55° to 125° C) test cycle is similar to the MIL-STD-883 (-55° to 125° C) shock cycle, except dwell times are extended to provide better temperature

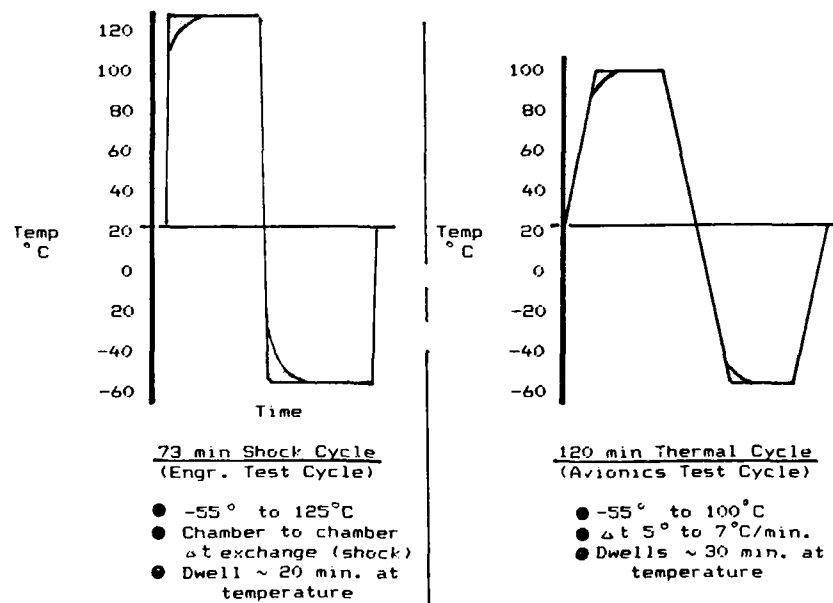


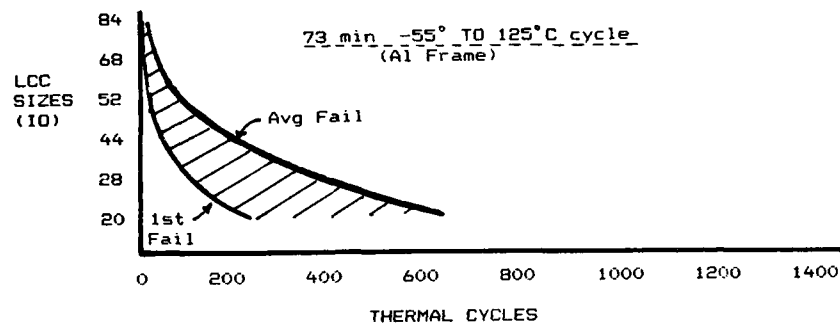
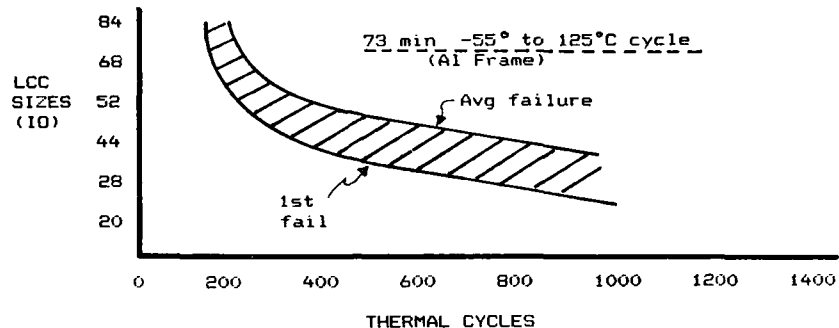
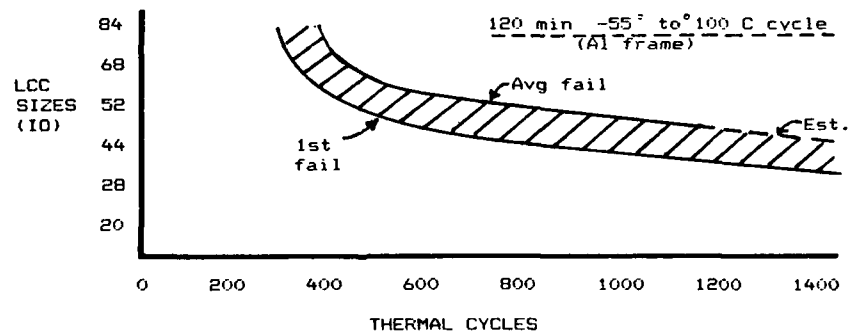
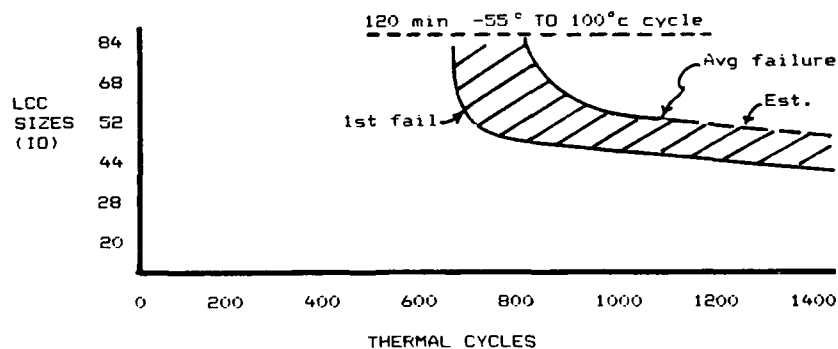
FIGURE 7 - THERMAL CYCLING TEST PROFILES

stabilization. The second two hour -55° to 100°C thermal cycle is considered a more reasonable but still worst case avionics type system cycle. A word of caution on these type testing cycles is that one must use great care in interpreting the results of these type tests as acceleration factors can be very difficult to establish, especially with the more severe -55° to 125°C shock cycle. Material properties of both solders and especially the MLBs can be extremely erratic with temperatures above 100°C . It is also extremely rare for military electronic systems to operate at temperatures above 100°C as integrated circuits are normally limited by design to a junction temperature less than 110°C (for IC Reliability), thus actual system operating temperature must be limited to lower temperatures, except for emergency military situations.

Test Results:

As shown (Figure 8-a), the LCC solder joint fatigue life with the epoxy-glass system in this severe shock test was quite poor, especially with the larger IO LCC modules. The epoxy-Kevlar MLBs (Figure 8-b) shows very significant improvements with LCC solder joint fatigue life in the same severe -55° to 125°C test cycle. The epoxy-Kevlar assembly shows further LCC solder joint fatigue life improvements in the more reasonable but still severe -55° to 100°C avionics type cycle (Figure 8-c).

A further and substantial improvement in LCC solder joint fatigue life was also established with the use of a properly applied conformal coating, in this case a silicone coating (Figure 8-d); however, great care must be used with conformal coating applications as we believe the use of conformal coatings can be detrimental if it shifts the Dwp of the module or creates bending or "Z" (vertical) axis thermal cycling solder strains. We believe that the LCC solder joint fatigue enhancements with the use of a properly applied conformal coating is due to, 1) more uniform strains and reductions in LCC solder joint stress concentrations, 2) an elastic type solder support with some coatings and 3) a compressive loading of the solder joint due to coating shrinkages. These fatigue improvements obtained with the use of conformal coatings have

a) EPOXY GLASS LCC FATIGUE LIFEb) EPOXY KEVLAR LCC FATIGUE LIFEc) EPOXY KEVLAR LCC FATIGUE LIFEd) EPOXY KEVLAR LCC FATIGUE LIFE - COATED

NOTE: As shown, a properly applied conformal coating can substantially improve LCC solder fatigue life

FIGURE 8 - THERMAL CYCLING LCC FATIGUE LIFE COMPARISONS

been verified in several different thermal cycling tests and also in some mechanical fatigue tests (Figure 18), which will be discussed later in this paper.

These overall test results show that with reasonable care in design and processing good LCC solder joint reliability can be provided for a great majority of military applications.

The plated-through-hole (PTH) reliability of the different MLBs used in these thermal cycling tests proved quite reliable with failures in the -55° to 100°C cycle being, in general, greater than 1000 cycles with the higher "Z" axis stress epoxy-Kevlar system. The epoxy-glass MLBs showed failures well beyond 1000 cycles. These tests verified that restraining normal "X" and "Y" expansions of the MLB can increase vertical "Z" axis PTH barrel stresses.

FAILURE ANALYSIS

Comprehensive failure analysis of the LCC solder joints showed that cyclic fatigue failure of the LCC joints were very dependent upon:

Solder Joint Configuration: with the smaller filleted ("A"- "B") type solder joints failing much earlier than the larger ("C"- "D") type solder joints (Figures 9, 10 and 11).

Uniformity of the LCC Solder Joints: Uniform solder fillets around the LCC module provides more uniform solder strains than with erratic solder joint configurations. Localized solder touch-up (rework) operations can also shift the TCE- D_{NP} thus, producing uneven and higher strain for the weaker or higher strained solder joints. In most cases, touched-up (reworked) solder joints rarely failed as these joints are normally stronger than non-touched joints due primarily to the stronger and finer grain structure with these faster cooled solder joints. Joint failure would normally occur on the opposite side of the reworked LCC module.

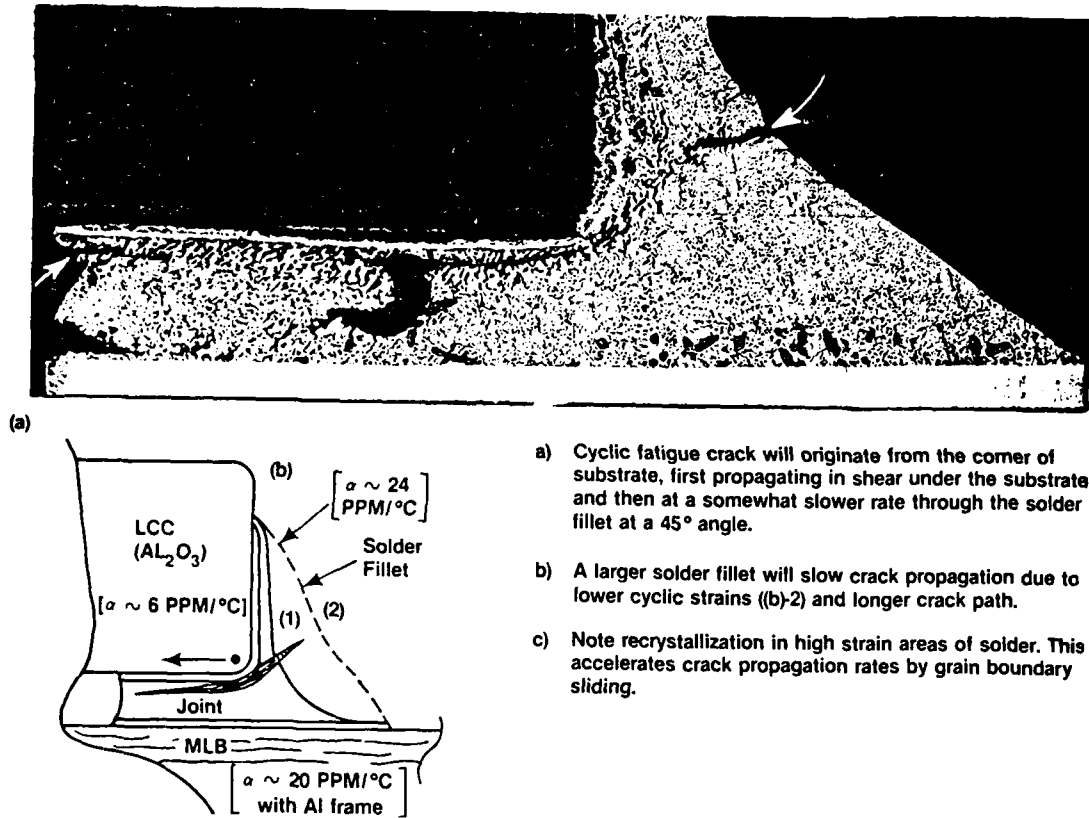


FIGURE 9 - TYPICAL CYCLIC SOLDER CRACK PROPAGATION



FIGURE 10 - TYPICAL CRACKING OF SMALL "A" TYPE JOINTS

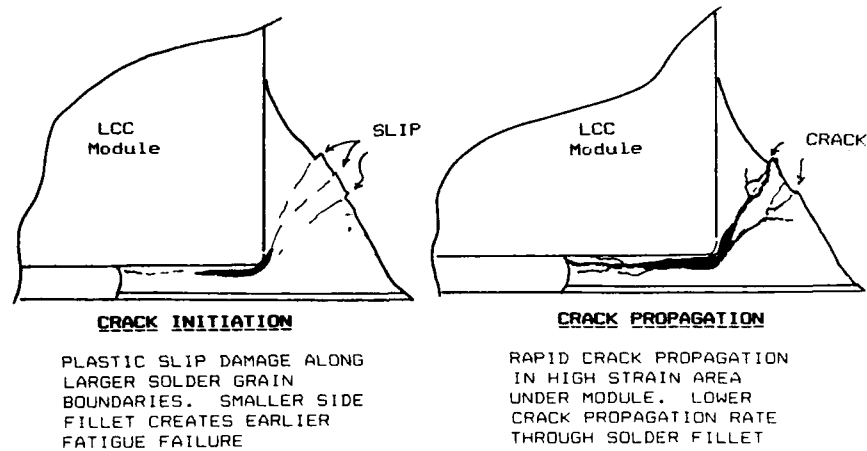


FIGURE 11 - TYPICAL LCC SOLDER JOINT FATIGUE DAMAGE

Anything that can lock down the LCC module (flux, coating, etc.) and shift the TCE-D_{NP} of the module can reduce LCC joint fatigue life due to uneven and higher cyclic joint strains. A bending or "Z" axis (vertical phase strains) can also reduce solder joint fatigue life.

Solder Joint Grain Structure: Crack propagation through the solder joint normally originates at the bottom corner of the LCC module, then the crack will propagate quite rapidly through the higher stress concentration solder area under the modules. Crack propagation would then continue up through the LCC solder fillets at $\sim 30^\circ$ to 45° angle, but normally at a lower rate than will occur in the higher stress areas under the LCC modules. Solder strain levels will be greatly reduced as the crack propagates into and toward the surfaces of the larger "D" type solder joint fillets (Figures 12 and 13).

Crack propagation rates through the solder fillets would be very dependent on, 1) the size of the LCC solder fillet (Figure 5), with the larger "D" type solder fillets providing much lower cyclic solder strains and a longer crack path to failure compared to the small "A" or "B" type solder fillets (Figure 9). There can easily be a four to five



BRIGHT/SHINY
 NO FATIGUE DAMAGE



AS-SOLDERED LCC SOLDER JOINTS



INITIAL
 SLIP DAMAGE



INITIAL CRACKING
 THROUGH SOLDER
 GRAIN BOUNDARIES



MORE SEVERE
 CRACKING
 (NOT FAILED)

LCC CRACK PROPAGATION - FATIGUE DAMAGE



- INTERMITTANT FAILURES -



ELECTRICALLY OPEN

FIGURE 12 - LCC TYPICAL CRACK PROPAGATION

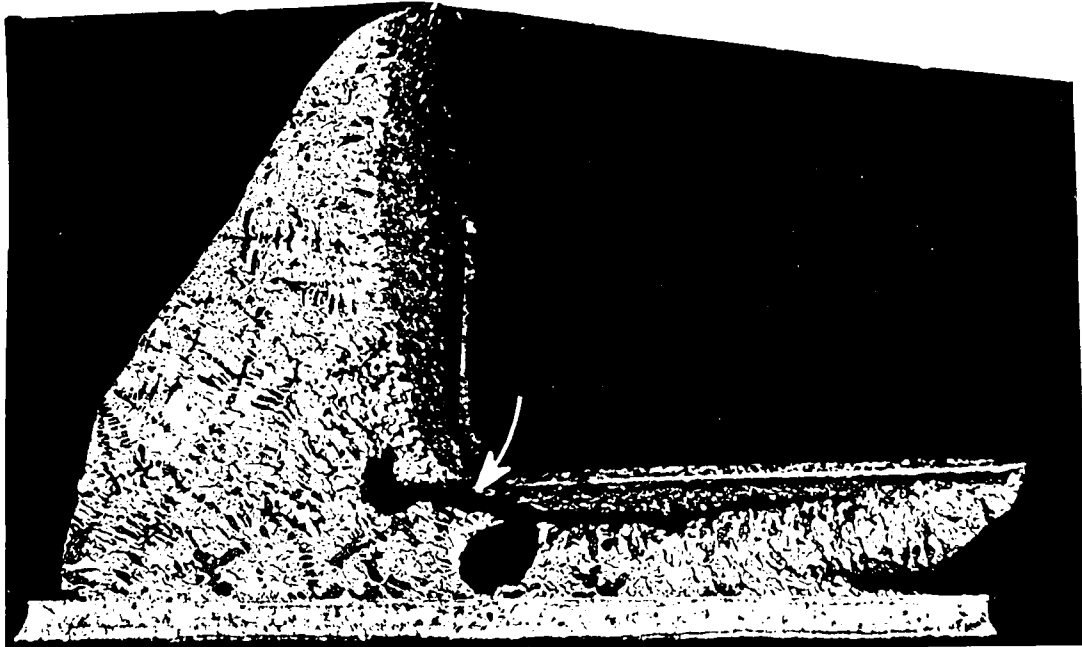


FIGURE 13 - TYPICAL JOINT CRACKING WITH AN OPTIMIZED JOINT CONFIGURATION

times improvement in fatigue life with the larger LCC solder fillets and 2) the resulting solder joint grain size and solidification direction can also be very important as to enhancing the fatigue life of the resultant solder joints. Again, a more uniform fine grain structure which can be created by faster cooling (solidification) rates will generally show better fatigue properties due to a more uniform plastic deformation of the solder joints. A very slowly cooled solder joint will experience both precipitation of lead (Pb) rich phases from the solder alloy with more lead phases in the slowest cooled areas of the solder joint in addition to a larger grain structure with the grains being somewhat aligned in the direction of cooling. Crack propagation rates can be very rapid through the weaker lead rich phases in the solder joint and through the very weak larger grain boundaries with a slowly cooled structure. Both solder grain size and direction can, however, be erratic with various LCC solder joints due to uneven cooling rates across the

assembly. This uneven cooling helps to explain the erratic nature (crack path) of some LCC solder joint failures.

SPECIAL MECHANICAL FATIGUE TESTING

In order to obtain more rapid test data on various solder alloys, processing effects and joint configuration a series of fatigue tests were conducted using the strain cycling dependent mechanical fatigue tester shown in Figure 14. This equipment has been quite useful in previous testing⁽⁴⁾ in helping to understanding solder fatigue mechanisms and to establish fatigue trends of various solder alloys, configurations, strain rates, temperature effects, etc.

Some Solder Alloy Evaluations:

These tests were conducted to establish both the mechanical properties and some basic bulk solder fatigue comparisons of several different solder alloys for possible application to these LCC technologies. Some [REDACTED] data suggested that there is substantial improvements in the fatigue properties of both Sn 50 and Sn 96 solder alloys; however, some of the testing could be questionable as the mechanical tests were conducted at unusually high cyclic fatigue testing rates (~3 sec/cycle.)

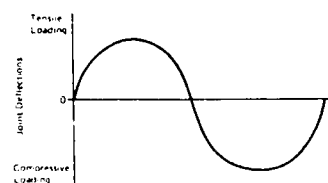
Both tensile and fatigue test bars were cast from the different test alloys for these evaluations (Figure 15). The samples were chilled cast to provide a reasonably fine grain structure and to insure alloy uniformity throughout the test specimen. The test specimens were then homogenized for 16 hours at a temperature ~50°C below the solidus point of the solders. Normally, at least five specimens were tested for each test group.

The tensile testing evaluation showed that the highest solder strength was obtained with Sn 62 solder alloy. This solder is normally used for both constant load "creep" applications and for diffusion applications especially with thick film technologies. The mechanical fatigue tests that were conducted at 6 cycle/min showed a substantial improvement in the fatigue properties of some of the solder alloys (Figure 15-c); however, when these alloys were retested at lower cyclic strain rates

MECHANICAL FATIGUE TESTER

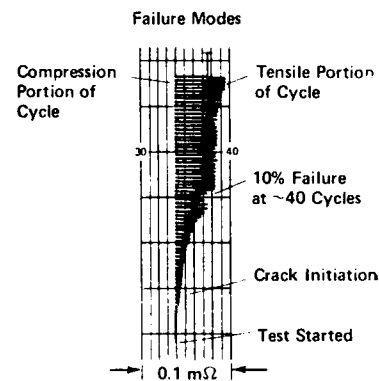


- 1/40 to 200 CPM
- 50 μ to 5/16 Inch
- Strain Dependent
- -55° to +100°C



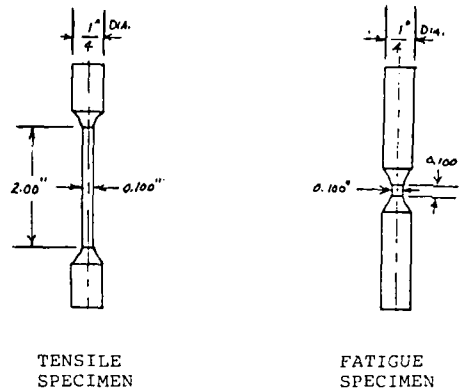
Mechanical Strain Cycle

(Not stress dependent)



Electrical Failure Plot

FIGURE 14 - SPECIAL MECHANICAL CYCLIC FATIGUE TESTER
(Strain Cycle Dependent)



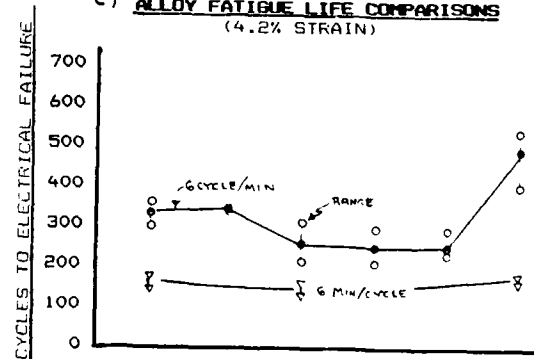
2) CAST MECHANICAL TEST SPECIMENS

b) TENSILE PROPERTIES

Alloy (Sn/Pb)	Tensile Strength (psi)		
	Tensile	Yield	% Elong.
50/50	4727	3781	85.1
60/40	4384	3565	113.5
SN 62	7271	6429	35.2
63/37	4961	4220	68.8
70/30	4302	3484	95.0
96/4	5076	4450	31.9

NOTE: Tests conducted at 23°C, 0.050 in/min strain rate.

c) ALLOY FATIGUE LIFE COMPARISONS
(4.2% STRAIN)



Solder Alloy Comp.	SN50	SN60	SN62	SN63	SN70	SN96
Sn	50	60	62	63	70	96
Pb	50	40	36	37	30	4
Ag	--	--	2	--	--	--

FIGURE 15 - BULK SOLDER ALLOY TESTING

(6 min/cycle) there was very little difference in the fatigue properties of the alloys. The testing was more limited at the lower testing rates (6 min/cycle); however, we believe that the data trends are reasonably accurate. These tests do not support major improvements with the use of either Sn 50 or Sn 96 solder alloys.

These tests, although not considered extensive, verified previous IBM data that suggested that it would be unlikely that a major LCC fatigue life improvement would be made with a selection of a more fatigue resistant solder alloy. Joint configuration and grain structure control is considered much more important as to enhancing solder joint fatigue life.

LCC SOLDER JOINT MECHANICAL FATIGUE TESTING

These series of tests were conducted to try and establish various fatigue life trends with actual LCC devices mounted on MLBs and then mechanically tested rather than thermally tested. A total deflection of 0.5 mil and a test rate of 6 min/cycle were selected to provide individual fatigue test results generally within a 24 hour test period. The test set-up (Figure 16) provided quite accurate mechanical strain testing of one row of 44 IO LCC solder joints. The test specimens were electrically monitored to establish a set 0.02 Ω failure point. The test specimens were soldered, inspected, mounted in the mechanical test fixture and then the side support portions of the specimen cut so that mechanical deflections would properly displace the now unrestrained LCC solder joint test assembly.

Strain Rate Tests:

Original fatigue testing was to determine the effect of mechanical testing rates on the fatigue testing results. All specimen for these tests were carefully hand soldered with "D" solder fillet configurations and a 0.004" standoff height of the LCC module from the MLBs. These were generally three to five tests conducted for each of the different strain rate tests.

These test results (Figure 17) showed that variation in cyclic testing rates will have extreme impacts on the test results obtained. This was especially noticeable with testing rates faster than 3 cycle/min where there is a sharp increase in cyclic fatigue life over the lower strain rate tests. The faster strain rate tests do not

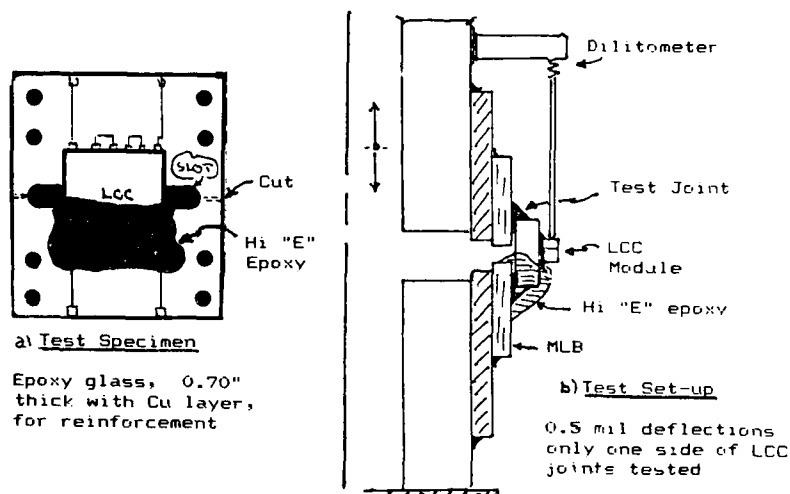


FIGURE 16 - LCC SOLDER JOINT MECHANICAL FATIGUE TESTING

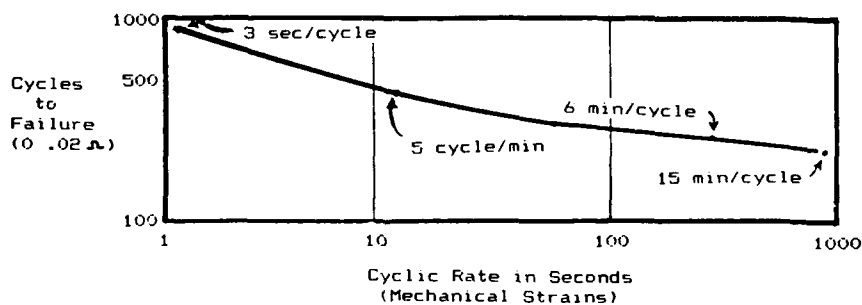


FIGURE 17 - LCC SOLDER JOINT FATIGUE LIFE VS CYCLIC TEST RATES

allow adequate time for low cycle plastic solder damage to occur as would be expected in normal thermal cycling environments.

As a result of these and other tests, IBM Owego has selected a standard test cycle of 6 min/cycle as a more reasonable and more accurate test for further evaluations.

Comparative Fatigue Testing:

Some comparisons in different LCC solder joint fatigue testing to date is shown in Figure 18. There are not a high number of tests in each test category but again what is shown is believed reasonably accurate. Some comments on these tests follows.

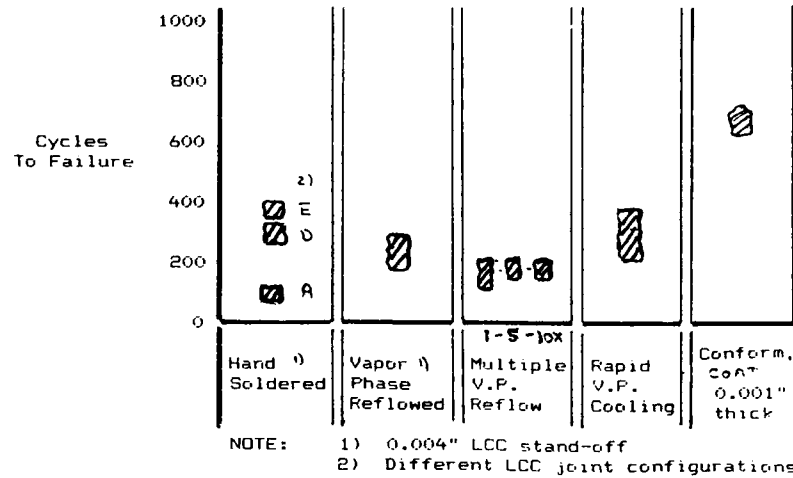


FIGURE 18 - SOME COMPARISONS IN LCC FATIGUE TESTING

Hand Soldered Tests: These tests show substantial fatigue life differences with a change in LCC solder joint fillet configurations. These mechanical tests again show that there are substantial fatigue life improvements with the larger "D" type solder joints over smaller "A" to "B" type solder joints, which is similar to that previously found in actual thermal cycling tests.

Vapor Phase Reflow Tests: These specimens were originally hand soldered, again with 0.004\" LCC module standoff from the MLB, and with "D" type fillet configurations. The 60/40 SnPb solder on the test samples was then reflowed using a standard vapor phase reflow process. The original LCC standoff was maintained during this vapor phase reflow operation.

The results showed a slight drop in fatigue life over the original hand soldered process. These results were expected as the vapor phase reflow process provides a coarser (larger) grain structure which is not as good for fatigue as would be a finer grain structure.

Multiple Vapor Phase Reflow Operations: This experiment was to establish the fatigue life trends with LCC modules, 1) processed with all normal (standard) in line process operations (solder screening, vapor phase reflow and normal cleaning operations) and 2) with multiple reflow cycles through the vapor phase reflow operation.

These fatigue test results show a small reduction in fatigue life with the lower 0.001" to 0.003" LCC standoff heights; however, multiple vapor phase reflow cycles showed little or no impacts on the fatigue life with up to 10 reflow cycles. These multiple reflow cycles degraded the appearance of the LCC solder joints but again the actual fatigue properties of the joints were not significantly degraded.

Rapid Vapor Phase Cooling Profile: These test specimens were the same as used in the above multiple V.P. reflow operations, except special spray mist cooling was used to accelerate the solder joint cooling (solidification) portion of the reflow process. The cooling rate on these specimens was approximately 10°C/sec. compared to a normal vapor phase cooling rate of ~ 1-2°C/sec. Although these tests are considered incomplete at this time, these tests provide further evidence that a faster cooling rate in soldering will be beneficial as to improvements in solder joint fatigue life.

Conformal Coating Experiments: The test specimens used in this evaluation were fabricated with the standard vapor phase reflow process with normal LCC standoff from the MLB. The specimens were conformally coated with a 0.001" thick Paralene coating for these tests.

As shown (Fig. 18) this conformal coating shows a major enhancement to fatigue life similar to that found with previous thermal cycling testing. Again, one must however use care with the selection and

the application of a conformal coating as there is evidence that an uneven or partial conformal coating can be detrimental to LCC solder joint fatigue life due to uneven solder joint stress application.

Summation:

The above test results show that these type mechanical fatigue test can be very helpful in establishing trends in LCC solder joint fatigue life, related to the effect of different processes, materials and configurations. These type tests do not replace the normally used thermal cycling tests, but they are very useful in helping to establish fatigue trends in a minimum testing time period.

DISCUSSIONS

The overall results show that for optimized solder joint fatigue properties of surface mounted components (SMT) it is important not only to control the design but to control several critical soldering processes. Some of these process controls are in conflict with the requirements of some present DoD soldering specifications (WS 6536E and DoD 2000). Recommendations on these specification conflicts follows.

Solder Configuration:

LCC joint optimization requires a very large bulbous solder fillet which is in conflict with the high wetting angle desired by DoD specifications. For LCC soldering applications, specification relief should be provided as long as proper solder wetting can still be established.

Enhanced Cooling:

Optimized solder joint properties normally require a faster cool down rate to produce a finer grain structure than provided by V.P. or IR soldering. Specification relief should be provided to use controlled cooling for V.P. or IR reflow soldering operations. This is needed in order to enhance both joint appearance and solder fatigue properties. Controlled enhanced cooling processes have been established to prevent the occurrence of disturbed joints.

Component Standoff Height:

LCC module standoff heights have been optimized for both fillet configuration control and proper cleaning at $\sim 0.005"$. A higher module standoff ($0.010"$) required by the DoD specifications (for cleaning) makes it near impossible to maintain control of the very critical LCC solder joint fillet configuration. Again, specification relief is needed for this critical requirement. We have proven proper assembly cleaning with a module standoff height of $\sim 0.005"$.

LCC Solder Voids:

A reasonable amount of solder voids ($< 25\%$) under the LCC module does not impact solder joint reliability. Specification relief should be provided as it is both extremely costly and difficult to meet the present specification requirements which technically are not needed.

Further Comments:

The technical issues with new technologies (SMT) and new soldering equipment (ex. V.P. or IR) are creating unique needs for soldering processes and controls which are or may be, in the future, in conflict with present DoD specifications. Industry and DoD must be flexible as to these possible specification conflicts and provide controlled relief when relief is proven to be technically proper.

CONCLUSIONS

- o With proper control of both designs and processes, LCCs packaging technologies have been proven to be reliable for the great majority of military applications.
- o In order to optimize LCC solder joint properties, substantial fatigue enhancements can be made by:
 - providing a bulbous ("D") type solder joint to reduce solder joint cyclic fatigue strains ("C"-"D" configurations).
 - enhancing joint cool down rates during IR or V.P. soldering will improve solder joint properties.

- A properly controlled conformal coating on the assembly can also improve solder joint fatigue life.
- o Optimization of LCC designs and soldering processes will at times be in conflict with some present DoD soldering requirements. Specifications relief will be needed to meet the technical needs of some SMT designs.
- o Major fatigue life enhancements are not believed probable with the most commonly used industry solder alloys. Configuration and process controls are believed much more important as to optimizing solder joint fatigue properties.
- o Solder voids under the LCC module do not have a significant impact on solder joint reliability.
- o Thermal and mechanical fatigue testing parameters (temperature limit and cyclic dwell times) are critical as to accuracy of test results.
- o Properly conducted mechanical fatigue testing can help establish fatigue life trends in a relatively short testing time period. Critical control of testing parameters and specimen preparation is however needed.

ACKNOWLEDGMENTS

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REFERENCES

- (1) K.C. Norris and A.H. Landsberg, Reliability of Controlled Collapse Interconnections, IBM J. Res. Devel. pp 266-271, 1969
- (2) J.K. Hagge, "Predicting Fatigue Life of Leadless Chip Carriers Using Manson-Coffin Equation". International Electronics Packaging Conference, Nov. 1982.
- (3) R.N. Wild, J.K. Lake, "Some Factors Affecting Leadless Chip Carrier Solder Joint Fatigue Life", presented 28th National SAMPE Symposium, Anaheim, CA April 12-14, 1983.
- (4) R.N. Wild, "Some Fatigue Properties of Solder and Solder Joints", IBM Tech. Report 742000448, July 1974.

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SOLDERABILITY AND SURFACE MOUNTING

by

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ABSTRACT

In the last decade through hole mounting to printed wiring boards has matured and people now have the tools to diagnose and correct any solderability problems which might arise. Such is not the case with surface mount soldering technology. In surface mount the connections are smaller and are often hidden from view. Therefore when a solderability problem does occur it may never be known until the assembly fails. The solution to the problem is to understand the nature of the problems and provide assurance they will not occur during assembly soldering.

This paper is structured in two parts. The first details the types of solderability problems unique to surface mounting. Examples of these problems will be shown and discussed with reference to solder joint life. The second part of the paper discusses the solderability testing of surface mount devices and printed wiring boards intended for surface mounting. This discussion will concentrate on the new quantitative solderability test methods being developed in our laboratory for leadless devices and printed wiring boards. As part of this development, new solderability criteria have been defined which reflect the unique problems associated with surface mounting.

Introduction

During the last decade through hole mounting and soldering of printed wiring assemblies has become a mature technology. Soldering in this technology is usually accomplished by molten bath soldering at 450 to 500°F. The impact of solderability on these processes is well known, the mechanisms of solderability are understood (Reference #1) and the tests used to define and control solderability are well developed. The situation is somewhat different in surface mount technology. The life limiting factor of fatigue is much stronger in surface mount technology than it is in through hole mounted technology. Therefore the need for complete and uniform solder joints is much higher. The testing of solderability of surface mount devices has generally followed the dip and look philosophy. The problem of assessment by this type of test is the small size of the terminations. In addition, the requirements for high solderability are much more stringent in surface mount due to the lower soldering temperatures of such processes as vapor phase and infrared. Only recently has there been serious investigation of the mechanisms and their effects on surface mount style solder joints. The problem of adequate solderability tests has also been approached and new quantitative tests are being developed.

This paper first discusses some of the work which has been done to define the effect of the mechanisms of solderability on surface mount solder joints. This is followed by a discussion of two new quantitative solderability test methods which have been developed around the wetting balance.

Effect of Solderability Mechanisms

The solder joints made in surface mount technology differ considerably in geometry from those in through hole technology. Through hole solder joints in printed wiring boards are analogous to a ring and plug joint. The solder joints in surface mount technology are more analogous to a lap shear style of joint. This difference causes more severe problems in surface mount than would normally be found in through hole. For example; any gases which are present in the joint area during soldering will have a much more difficult time of exiting the solder joint area in a lap shear solder joint than they will in a ring and plug style of joint (ie; plated-through hole through mount).

Another factor unique to surface mounting and soldering is the dynamics of the soldering process itself. Most high-tech, high reliability assemblies are soldered using pre-placed solder and a reflow process. This combination does not offer the mechanical and fluid agitation that the hand soldering and wave soldering do in through mount technology. Therefore these surface mount solder joints are more prone to contamination, intermetallic build-up and oxide film problems.

As in other areas of soldering technology, the worst condition is that of non-wetting. In surface mount technology the causes of non-wetting are much the same but can be of greater consequence. The major causes are still non-reducible films or too low a temperature to allow the solder to metallurgical wet. In surface mount, the area most susceptible to problems is the heel area under the package (see Figure 1). This is the same location as the normal initiation sites for thermally induced fatigue cracking. Heat has to flow into this area in order to raise the temperature of the surfaces to be soldered and also the solder. Both the substrate and the package termination must be clean and up to temperature in order to obtain a quality joint. Without a proper joint and with defects in the heel area, early fatigue failures can occur.

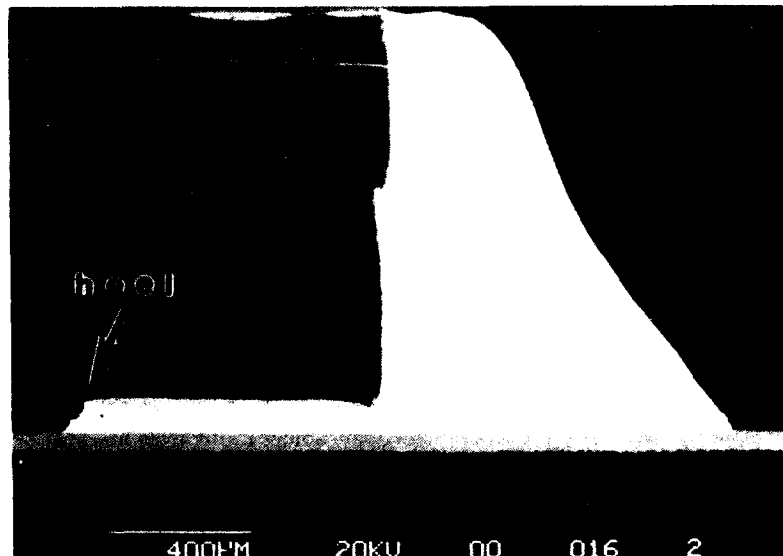


Figure 1

Figure 2 shows an example of a non-wetting solderability defect. In this case the board temperature was high enough to cause flow along the pad but there was a lack of heat at the component side and a situation analogous to a cold shut in castings occurred. This can be told by the microstructure of the tinning solder on the component. It is obvious that melting had not occurred during the soldering process. There also may be a passive film on the tinning solder surface which may have aggravated the problem. The resultant joint is highly susceptible to early failure.

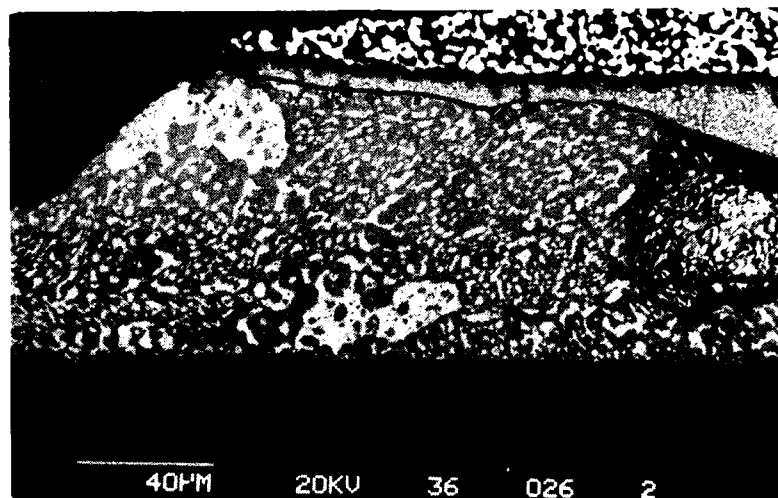


Figure 2

The other solderability mechanism of concern is dewetting. Our findings in the study of mechanisms involved with surface mount soldering have shown that a major cause of void formation in solder joints is dewetting. One of the features of the general mechanism of dewetting is gas evolution (Reference #2). This gas release is the one that is the cause of voids. It was first noted in through hole solder joints that had weak knees. A typical example of gas evolution due to dewetting in a through hole joint is shown in Figure 3. With dewetting, the longer the exposure to molten solder, the greater appears to be the evolution of gases. The figure shows that the gases will continue to evolve up until the time that the solder has solidified.

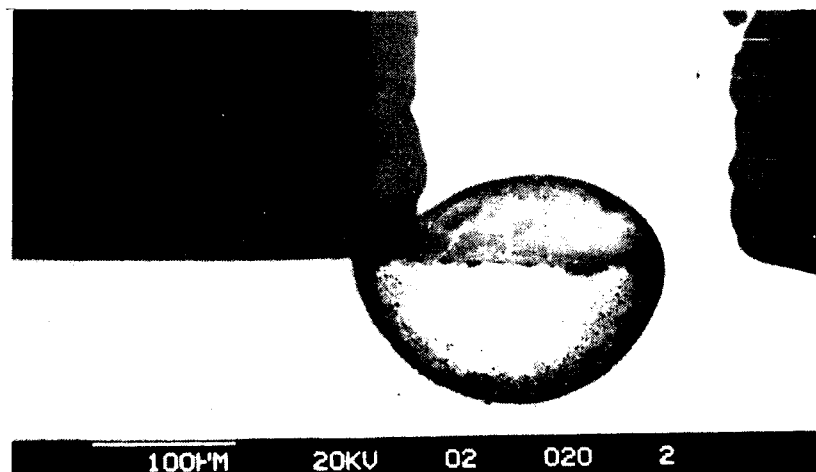


Figure 3

In surface mount soldering the same gas evolution problem occur but there is little probability that the gas will exit the joint area. Figure 4 shows the bottom pad area in the solder joint to a leadless chip carrier (LCC). Higher magnification, back scatter electron images show a large amount of co-deposited organics in the plating to which the solder joint is being made. The voids that have been produced are extensive and the source of the gas can be seen to be the layer with the organics.



Figure 4

As shown in previous work (Reference #2 and #3), the gas evolution that causes dewetting can come from many sources. Recent evaluations indicate that another source is the result of the flux related chemical reduction process. Areas which dewet are typically passivated, either from exposure to air or from the decomposition gases of contaminants or co-deposited materials. The flux, in general, will perform its cleaning function by converting the oxide (passive film) to a salt. This conversion will release oxygen containing compounds usually as a gas. It is this excess gas which causes the void formation.

Solderability Testing for Surface Mount

The advent of surface mount technology has put a new outlook on the problems of solderability. Processes such as vapor phase can operate at soldering temperatures as low as 200°C. These low temperatures reduce the ability of fluxes to clean and keep surface tensions low. In addition, the emphasis on doing it right the first time has become more intense. Many surface mount assemblies, especially the more advanced designs, are very dense or use components with very fine lead pitches. This often restricts the ability to apply repair or rework procedures. The answer to many of the problems is to have components and boards with very high solderability at the time of solder processing. Therefore, a solderability test must be applied in order to obtain the information needed.

Until recently, all solderability tests for surface mount components have been modifications of the dip and look tests. The main problems with these type of tests when applied to surface mount type of components are the subjectivity of the tests and the problem of defect identification on very small surfaces. In conjunction with the Air Force manufacturing technology program for Advanced Data/Signal Processing we have been developing quantitative solderability tests for surface mount applications. I would like to discuss two of the quantitative methods we have developed for surface mount parts as part of this program. One of these is for printed wiring boards and the other is for leadless components. Both are wetting balance techniques.

Solderability Test for Printed Wiring Board Surface Conductors

The purpose for development of a test for printed wiring is to ascertain the solderability of the attachment pads for use in surface mounting. The wetting balance has been used to good advantage in the testing of printed wiring board materials with no change in the equipment needed. Printed wiring board materials offer a major challenge to the use of the wetting balance as opposed to solid metallic materials because of their unusual buoyancy and thermal conductivity characteristics. Another problem in the development of a test was that every printed wiring board is application specific and there is no such thing as a few standard boards like there are component lead shapes in production articles.

The first problem approached was that of sample definition. The solution was the use of a coupon specifically designed for the test. While the use of a coupon is recognized as not an ideal situation, it was the only way the test could be standardized for printed wiring boards without introducing uncontrolled variables. The sample as finally defined, is a strip of clad laminate 1/4 inch wide by one inch long, preferably double sided. This coupon will fit easily into standard panels or into the 55:10 coupon area. In order to be useful the metal surfaces of the coupon must come fully to the edge of the coupon. The sample, as it is defined, can be used directly in any commercial wetting balance without modification to the fixtures or to the balance itself. Figure 5 shows a typical coupon in a standard fixture.

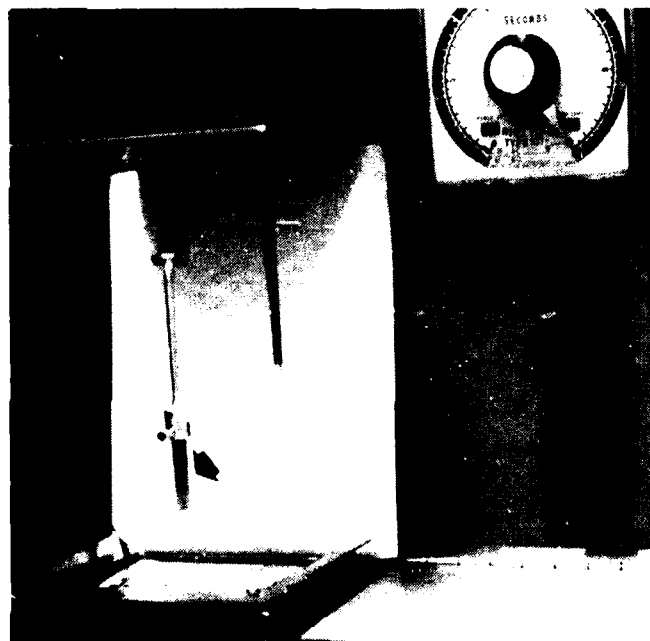


Figure 5

The next problem to be approached was that of buoyancy correction. A typical coupon sample has metal (solderable) surfaces on two sides in the case of a double sided laminate or one side for single side laminate. This means that a typical sample has considerable non-solderable surfaces exposed to the molten solder bath during testing. In addition laminate density is much less than solder density. Therefore the buoyancy effect on the generated wetting curve will be significant. A number of approaches to correct for buoyancy were tried and a very simple approach was settled upon. This is to use the standard formula applied to metal leads. With the large sample size the error is minimal. The formula or buoyancy correction is:

$$F_b = \rho g V$$

Where:

ρ = density of molten solder (8 g/cm³ for Sn63 solder)

g = acceleration of gravity (980 cm/sec²)

V = volume of sample immersed in solder

The last major problem was that of thermal conductivity of laminate materials. Since the thermal conductivity of laminates is much lower than that of metals they are slower to come up to soldering temperature. By empirical studies we are able to relate wetting times to the thickness of laminate. Figure 6 shows this relationship as it affects acceptable wetting times.

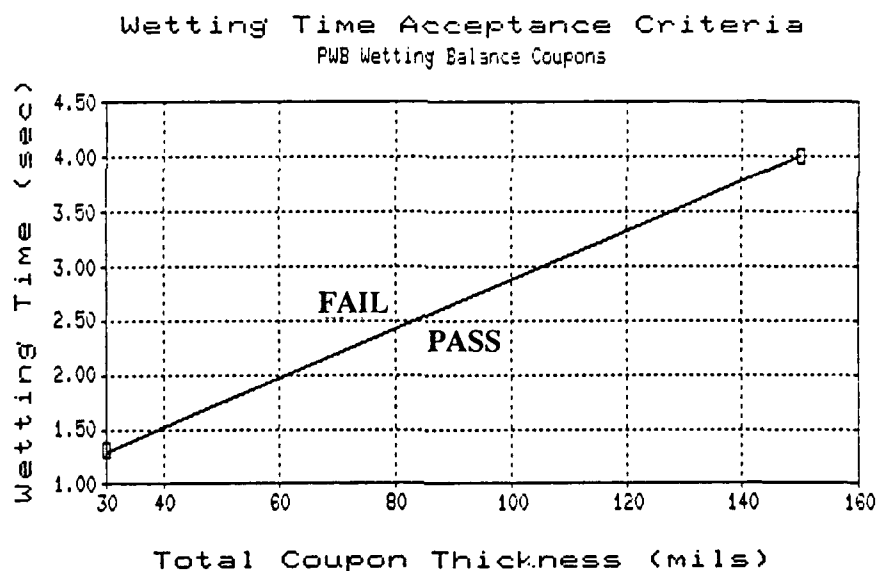


Figure 6

The wetting curves, as they are drawn, look different than those taken on solid metal samples. Figure 7 shows the typical curve for a metallic lead. Figure 8 shows the curve for an 0.062 inch thick laminate sample. This curve never rises above the instrument zero. However, when the corrections for buoyancy are made and the new zero drawn the curve appears more normal. The corrected curve is shown in Figure 9.

Normal Wetting Balance Curve

Solid Metal Lead

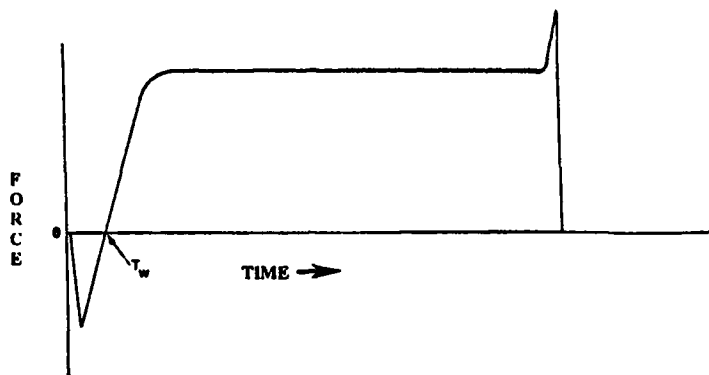


Figure 7

PWB Wetting Balance Curve

0.062 inch Thick Laminate

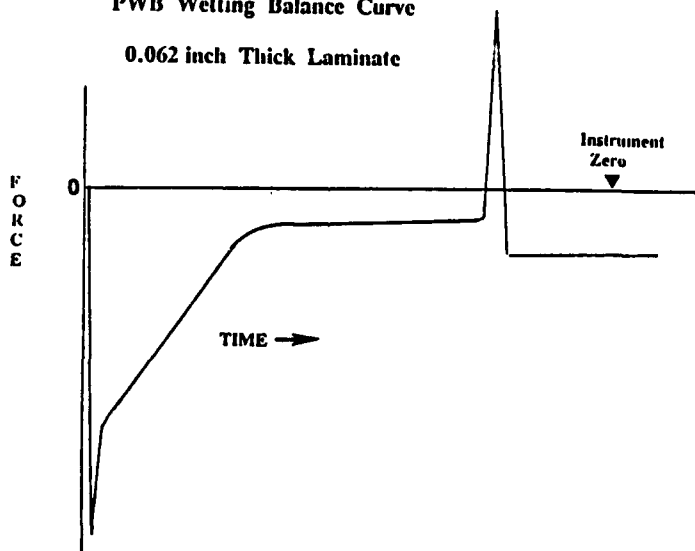


Figure 8

The one portion of the curve which has not been fully evaluated is the withdrawal force. This is much higher than normally develops when full metallic samples are tested. Work on this portion of the curve needs to be done to see how well it still relates to dewetting potential.

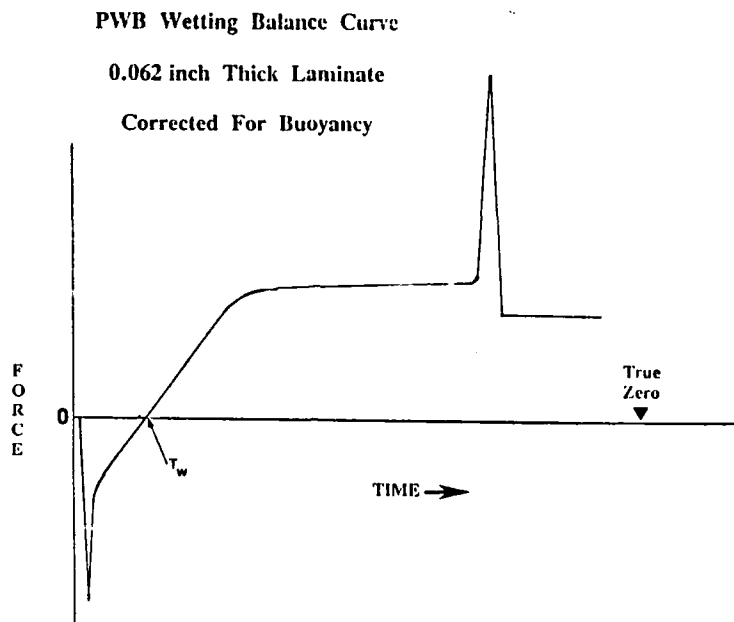


Figure 9

Solderability Testing of Leadless Components

The purpose of the development of a solderability test for leadless components was to eliminate the subjectivity of the dip and look test and provide one which was quantitative by nature. Work in Europe and Great Britain is now going on to develop a solderability test utilizing the wetting balance in the scanning mode. These methods are very early in their development (Reference #4 & 5). The curves generated are very different than the normal wetting balance test curve. Interpretation of such curves, in terms of physical events, has not been done to any extent. The work by Martin Marietta (Reference #6) requires a highly modified wetting balance and also develops a curve much different than normal.[^]

Our development effort has taken the approach that there should be no modifications to the wetting balance hardware, other than fixtures and that the developed curve should be as close to normal appearing as possible. Following a number of experiments with different techniques the method determined to have the greatest potential was one in which the leadless component is placed in contact with the molten solder at 45°. In other words, with the corner of the termination just touching the surface of the solder bath. Figure 10 is a schematic of the specimen orientation to the surface of the solder.

45° SOLDERABILITY TEST

FIXTURING SCHEMATIC

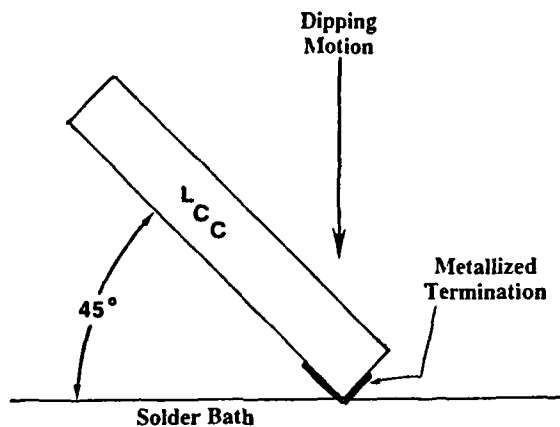


Figure 10

Early experiments with this method used dip depths of about 1 mm. Due to the small size of leadless component terminations very inconsistent results were obtained. This was especially true when attempting to measure wetting times. It appeared that there was no good way of determining buoyancy. The dip depth finally settled upon was 0.02 to 0.03 mm. The sample is really just touching the solder surface. The generated curve (Figure 11) shows no initial dip below instrument zero. The normal definition of wetting time does not apply under these dipping conditions. It was also found that in order to achieve consistent results that the flux solids content had to be raised to 40%. This seems to be a heat transfer problem.

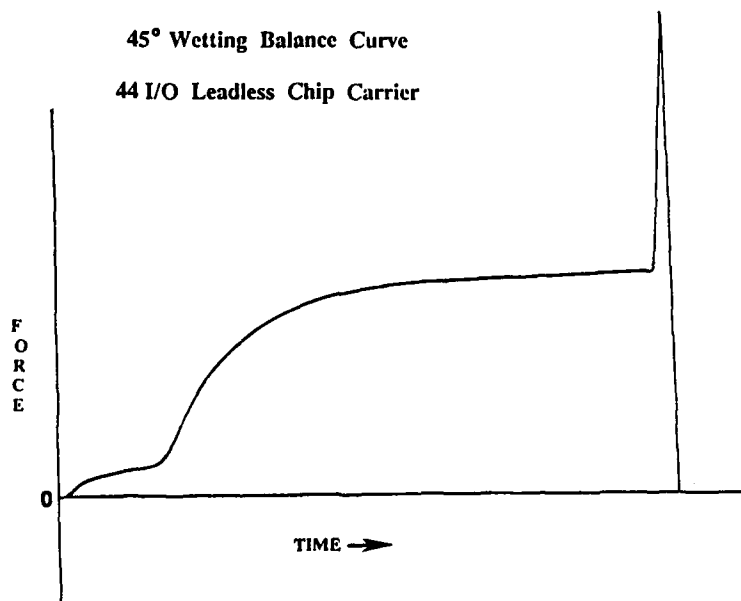


Figure 11

When the test is run on castellated chip carriers, the solder will wick up the castellation very rapidly and then will wet up the bottom pad at a much slower rate. As the solder wets the termination, the meniscus of the solder rises to cover all of the termination area (if solderability conditions allow). At this point equilibrium wetting is achieved. The wetting pattern follows very closely that which has been described by Klein-Wassink (Reference #7).

Since a wetting time evaluation is not possible with this test method some means of measuring both the speed of wetting and the quality of wetting had to be arrived at. The result of many curve evaluations and observing the wetting process resulted in the development of a new solderability measurement. This is the coefficient of wetting. It is the slope of a straight line drawn on the curve from the start of the test to the point where equilibrium wetting occurs (Figure 12). This requires that the test dwell time be not fixed and that enough time of dwell is left after equilibrium is reached to assure that the curve has truly turned flat. The best method to run the test is to watch the curve as it is being drawn. The slope measurement gives a composite of information on both speed and quality of wetting. Experiments with both castellated and bottom pad only LCC's of varying pad numbers and sizes indicate that the measurement is independent of these. The coefficient of wetting appears to be a property of the wettability of the terminal areas. The following table is the averages of several tests performed using 40% solids type "R" rosin flux. The samples labeled gold were as we received them and were not steam aged. These parts were of varying age and had seen a variety of treatments.

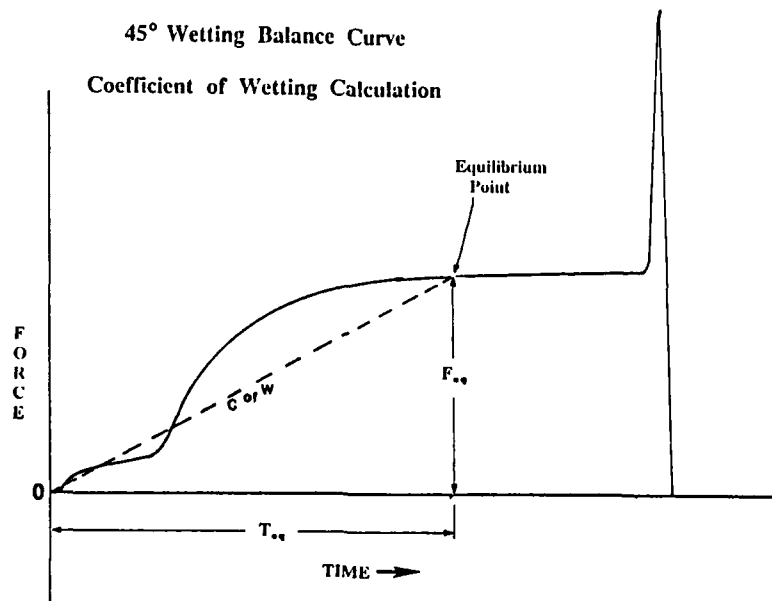


Figure 12

Table 1

Wetting Balance Data for LCC's

Specimen	Finish	Size	T _{eq} (sec)	F _{w@eq} (dynes)	Coef of Wetting (dynes/sec)
Castellated	Gold	44 I/O	67	448	7
Castellated	HSD	44 I/O	27	399	16
Bot Pad only	Gold	32 I/O	40	108	3
Bot Pad only	Gold	84 I/O	19	145	7
Bot Pad-spec	Gold	84 I/O	23	232	10
Bot Pad only	HSD	32 I/O	11	137	12
Bot Pad only	HSD	84 I/O	15	235	16
Castellated	HSD	44 I/O	27	399	16

The results shown in this table are consistent with what is known about the parts and their condition as we received them. For example, the 32 I/O carriers were very old, probably over 1 year. Even hot solder dipping did not give an optimum coating of solder on these parts. This was observed under a microscope prior to testing. The variation in some of the data pointed out the need for reliable fixturing. One aspect that close attention is required is the detection of contact of the terminations with the solder. It has been found that the only reliable way of doing this is by making direct electrical contact with one of the terminations by the fixture. A fine, non-wetting probe wire has been found to work well.

In normal wetting balance testing of solid metal leads or terminations it is possible to use the withdrawal portion of the curve to assess the tendency for a surface to dewet (Reference #1). When leadless component terminations or printed wiring board coupons are tested using these new tests a curve that is much different from the classic curve is obtained. Brief studies in evaluating the withdrawal portions of these curves indicate that the same information on dewetting cannot be arrived at. It appears that the information may be still present but is also combined with other factors such as drag from non-wettable areas and geometry effects.

Solderability Test Parameters

When testing of devices for surface mount applications is discussed the question of what constitutes the proper parameters always comes up. For the tests we have specified the standard eutectic solder (60/40 or 63/37 Sn/Pb) and a test temperature of 245°C have been selected. The reason for selecting these are for uniformity in test documents. Usually few people have problems with the solder selection. The main objection is the temperature as it is much higher than is normally found in surface mount soldering. We have found in our experimentation that any test temperature can be related to another through the use of data such as is shown in Figure 13. If someone wishes to use another temperature then the acceptance criteria will have to be adjusted accordingly.

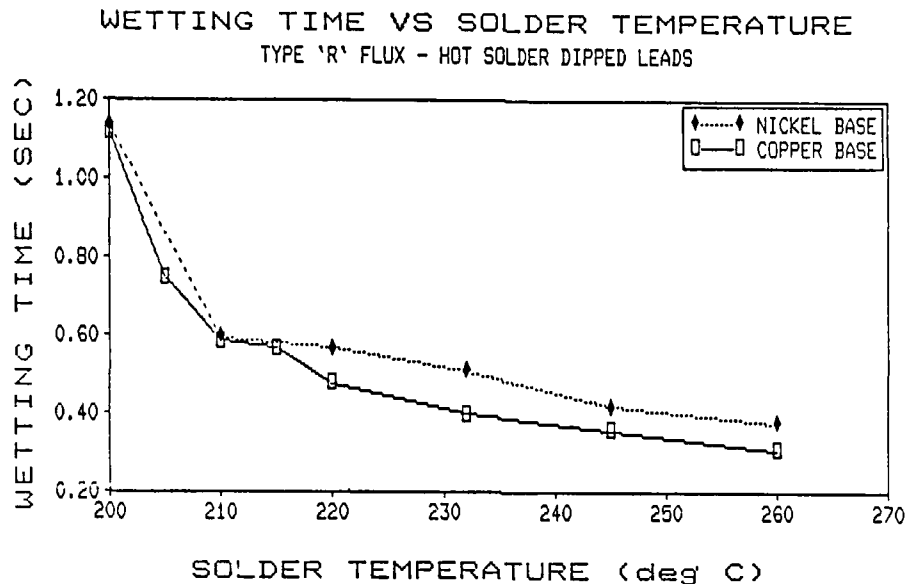


Figure 13

Summary

- 1- While the same solderability mechanisms that are valid for through hole mount technology are present in surface mount technology, their effect may be greater because of either geometry or solder processing differences.
- 2- It has been shown that a major source of solder joint voids are surfaces which exhibit dewetting. The gas evolution which is part of the mechanism will continue up until the time that solidification takes place. The sources of the gas appear to be either organics or oxides in the coatings or basis metals.
- 3- Since solderability becomes even more critical in surface mount applications it becomes more important to assure high solderability prior to assembly soldering. In addition, quantitative, non-visual solderability tests are required in order to properly assess the level of solderability at the time of component receipt.
- 4- Two new quantitative solderability tests have been developed to meet the needs stated above. One of these addresses the problem of board solderability while the other can assess the solderability of leadless components. Both of these tests are based on the wetting balance.
- 5- A new measure of solderability has been defined. This is the coefficient of wetting and provides composite information on both the speed and quality of wetting. It does not however assess the tendency a surface might have to dewet. While normal wetting balance testing of solid metal parts can describe the tendency to dewet further work is required in curve interpretation when surface mount style leadless component of printed wiring board coupons are tested.

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References

1. John A. DeVore. "Solderability", The Journal of Metals, July 1984.
2. John A. Devore. "Mechanism of Dewetting on Copper Surfaces", 2nd Annual Soldering Technology Seminar Proceedings, China Lake Naval Weapons Center, February 1978.
3. John A. DeVore. "Co-deposited Organics in Plated Coatings - A Problem", 5th Annual Soldering Technology Seminar, China Lake Naval Weapons Center, February 1981.
4. Gert Becker. "Scanning the Solderability of a Surface", Welding Research Supplement, October 1981.
5. I.A. Gunter. "The Solderability Testing of Surface Mount Devices Using the GEC Meniscograph Solderability Tester", Circuit World Magazine, Vol. 13, No. 1, 1986.
6. E.F. Lish and J.O. Weber. "Solderability Testing of Leaded and Leadless SMD's by Means of a Modified Wetting Balance", 11th Annual Electronics Manufacturing Seminar, China Lake Naval Weapons Center, February 1987.
7. R.J. Klein-Wassink. "Soldering in Electronics", Electrochemical Publications LTD, Scotland, England, 1984.

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DESIGNING ELECTRONICS FOR AUTOMATED INSPECTION

by

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ABSTRACT

Electronic packaging technologies, such as Pin Grid Arrays, increasingly small pitch Surface Mount, and double-sided assemblies are all aimed toward the highest possible product density, with improved performance. The gap between inspection effectiveness and advancements made in packaging technologies is becoming larger. As efforts proceed to learn more about critical factors influencing reliability of solder joints, it is prudent to ensure that Printed Wiring Assembly (PWA) design rules evolve to permit the broadest range of anticipated automated inspection requirements.

The range of automated inspection technologies can all be made more effective through careful design of electronics for inspection. Significant opportunities lie in both PWA layout and design, as well as electronic component design, tolerancing, and standardization. Many inspection issues are shared, but with increased recognition of digital radiography's unique capabilities, this discussion will emphasize x-ray inspection issues.

INTRODUCTION

MANUFACTURING IMPACT OF INSPECTION TECHNOLOGY

The typical discussion of electronics inspection has focused on a strict comparison of automated versus non-automated technology. We define automated inspection as the use of automated equipment featuring computer-based image or signal analysis to perform final determinations regarding the acceptability of a product. Non-automated inspection is therefore characterized by the use of human analysis, with the optional use of inspection instruments or equipment, for the determination of product acceptability. The distinction therefore, comes from the handling of the data analysis task. It can also be further noted that, in terms of reliability and economics, automated inspection lends itself best to a manufacturing process using automated assembly.

We believe that those who wish to look forward in this industry must begin to consider a third scenario in the discussion of electronics inspection. This is the maximization of automated inspection effectiveness through the practice of designing for automated inspection. This concept goes beyond design for strictly performance and manufacturability.

The motivation for considering such issues at the design level is indicated in Figures 1 through 3 and relate to improvements in inspection effectiveness. Inspection reliability can loosely be defined as the ability of the inspection process to effectively and repeatedly detect defects of interest while accepting non-defective product. Reliability will span a range depending on the technology being utilized. The specific reliability within this range will be affected by the inspection system's imaging technology, repeatability, resolution, and programmability. As all non-automated inspection technologies, regardless of the form of data collection and presentation, rely on human analysis, we suggest that the significant variable affecting reliability of non-automated inspection will be human judgement variability. As one adopts any application of automated technology, repeatability generally is significantly improved. A realistic upper bound to the general reliability of inspection technology, without design for inspection, is approximately ninety percent as Figure 1 shows. However, a commitment to designing and developing product at the earliest stages toward the requirements which automated inspection technologies impose can be rewarded with reliability figures approaching one-hundred percent.

A similar story is told in Figure 2 regarding the ability to effect reductions in outgoing defect levels. Although specific figures do not appear in published form, the general scaling and shape of the curves fairly show the opportunities for reducing outgoing defect levels as one considers progressively more effective forms of inspection technology. As inspection reliability improves and outgoing defect levels decline, one is faced with a natural decline in cost per unit (Figure 3).

The fundamental mechanisms affecting these improvements can be identified. A significant correlation exists between improvements in system reliability and reductions in system error (in Figure 4, system error is shown only for the case of automated inspection with design for inspection; the other two cases would have relatively greater system error). Reductions in inspection system error provide the opportunity to better control the manufacturing process. A process which is controlled will show a narrower distribution of critical PWA features than will a process which is not controlled. Figure 4 illustrates such a successive development of three different measurement (or feature) distributions for the inspection technology scenarios discussed above. A narrower distribution will naturally reduce the number of measurements near the pass/fail threshold. This is seen in the different heights of the three curves in this region. The effect of these relationships is shown in the areas defined as "false accepts" (also known as "escapes") and "false rejects" (also known as "false alarms"). Through a development of inspection technology, the "false accept" and "false reject" areas will be reduced both in width and in height. As an added benefit, the narrower distribution of critical PWA features, permits the inspection technology to be "tuned" to detect progressively more subtle features which will further enhance system reliability. In such a fashion, the system can reach a maximum level of performance capability.

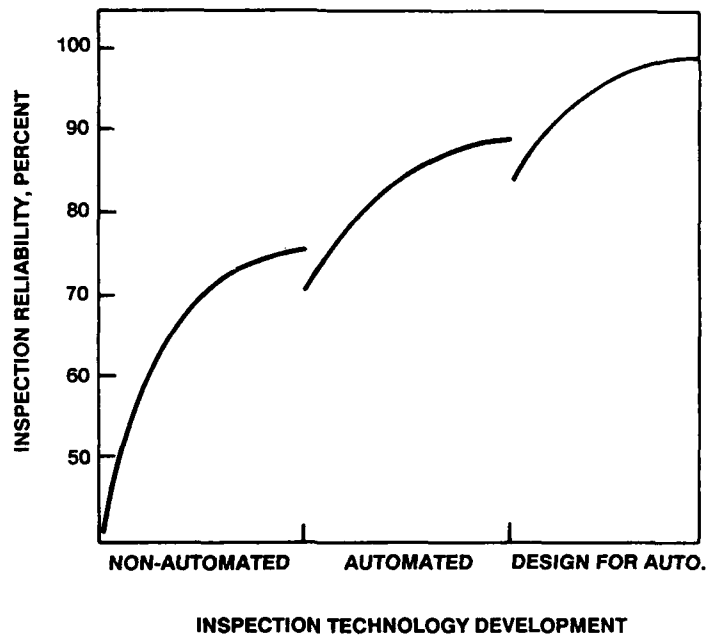


FIGURE 1. Inspection Reliability versus Inspection Technology Development

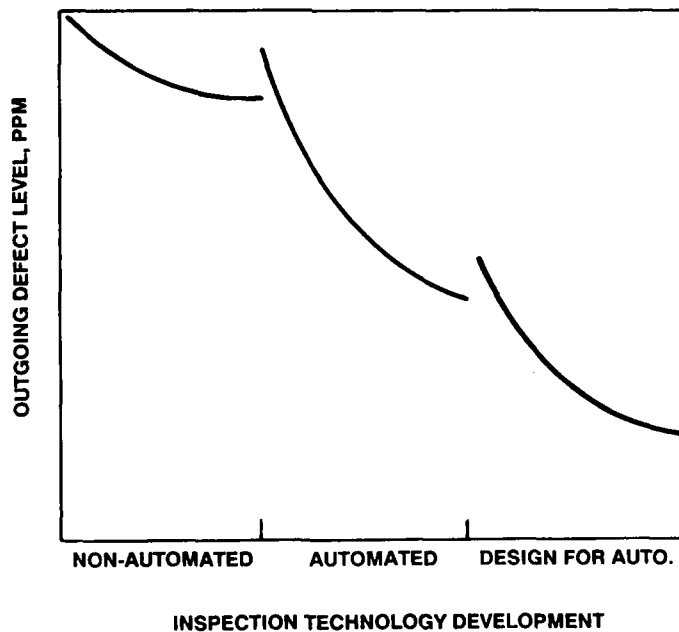


FIGURE 2. Outgoing Defect Level versus Inspection Technology Development

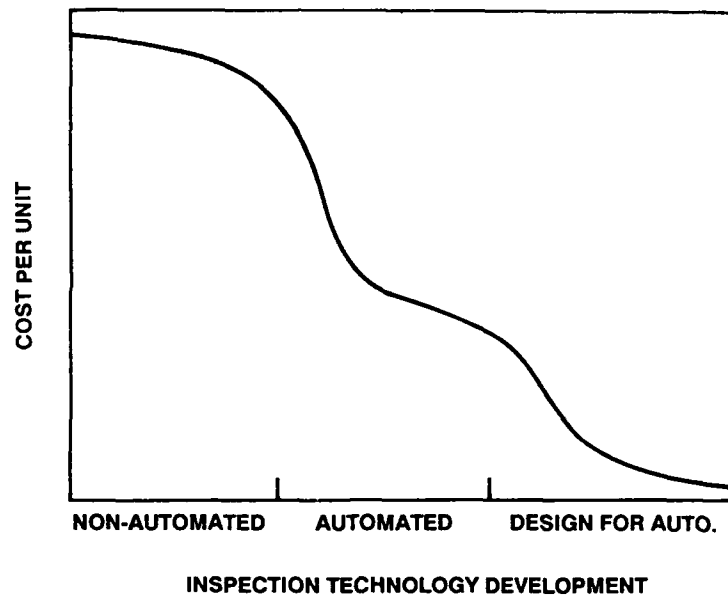


FIGURE 3. Cost per Unit versus Inspection Technology Development

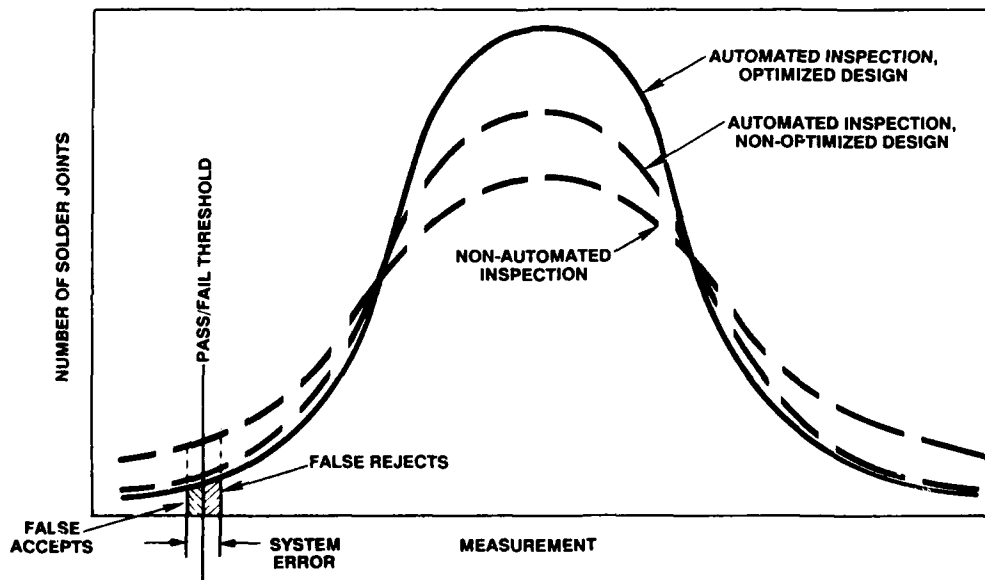


FIGURE 4. Comparison of Inspection Scenarios

OPPORTUNITIES

What follows is a discussion which will review the special opportunities for improving automated inspection of PWAs in the manufacturing environment and the technologies that can be considered. The analysis techniques that become a principal element of such inspection systems are also reviewed.

Many specific circuit board layout opportunities and issues have been identified. These include: general assembly issues, Plated Through Hole (PTH) technology issues, Surface Mount Technology (SMT) issues, and double-sided assembly issues. How to optimize these opportunities for automated inspection is discussed. Likewise, significant package design opportunities and issues exist. Those presented address tolerances, significant features, x-ray transparency, and new component opportunities.

AUTOMATED INSPECTION TECHNOLOGIES

There are currently four automated inspection technologies considered as viable for production line use. They are 2D Vision, 3D Vision/Structured Light, Laser/Infrared, and Real Time Digital X-ray. All but the Laser/Infrared will digitize the image. The most common digitization is to a 256 by 256 or a 512 by 512 grid of pixels (the 512 by 512 giving 4 times the resolution). Each pixel typically has a grey scale value of 8 bits where 0 represents black, 255 represents white and those numbers in-between are shades of gray (Figure 5).

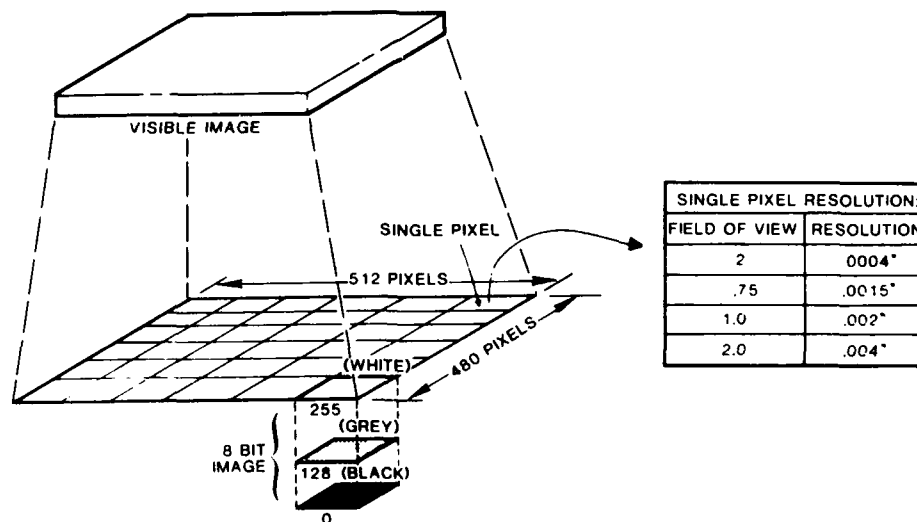


FIGURE 5. Image Digitization

Resolution is determined by the number of pixels and the size of the imaged object. If a 1" by 1" square is imaged with a 512 by 512 digitization scheme, each pixel represents 1/512" or about 0.002" square. Some systems allow a variable field of view to optimize resolution and throughput since throughput, in general, is tied to the number of images to process. Therefore, you want to choose the maximum field of view with a resolution able to distinguish the defects of interest.

2D Vision. With the 2D Vision technology, the camera translates the amount of light reflected into a shade of grey ranging from black for non-reflective regions to white for highly reflective regions (Figure 6). Colors will reflect different amounts of the visible spectrum, so filters can be used to selectively choose the spectrum desired.

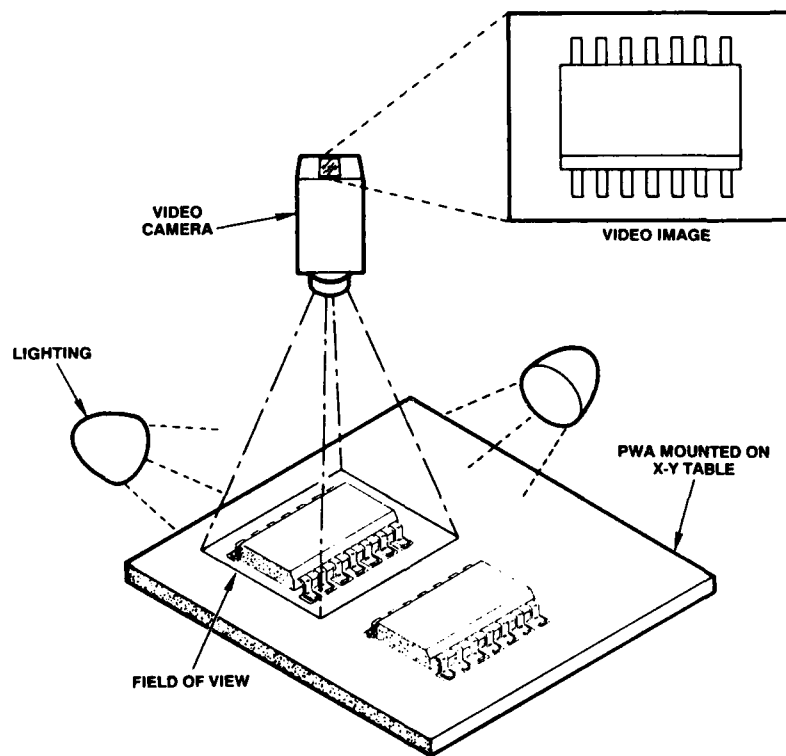


FIGURE 6. Conventional 2D Vision System

3D Vision. With 3D Vision the camera translates deflections in the position of the reflected scanning light into relative heights (Figure 7). These scans can optionally be combined into an image similar to a TV image by assigning a grey scale level to the height and thus producing a 3D effect. The grey levels typically range from black for board level to white for the highest elevations.

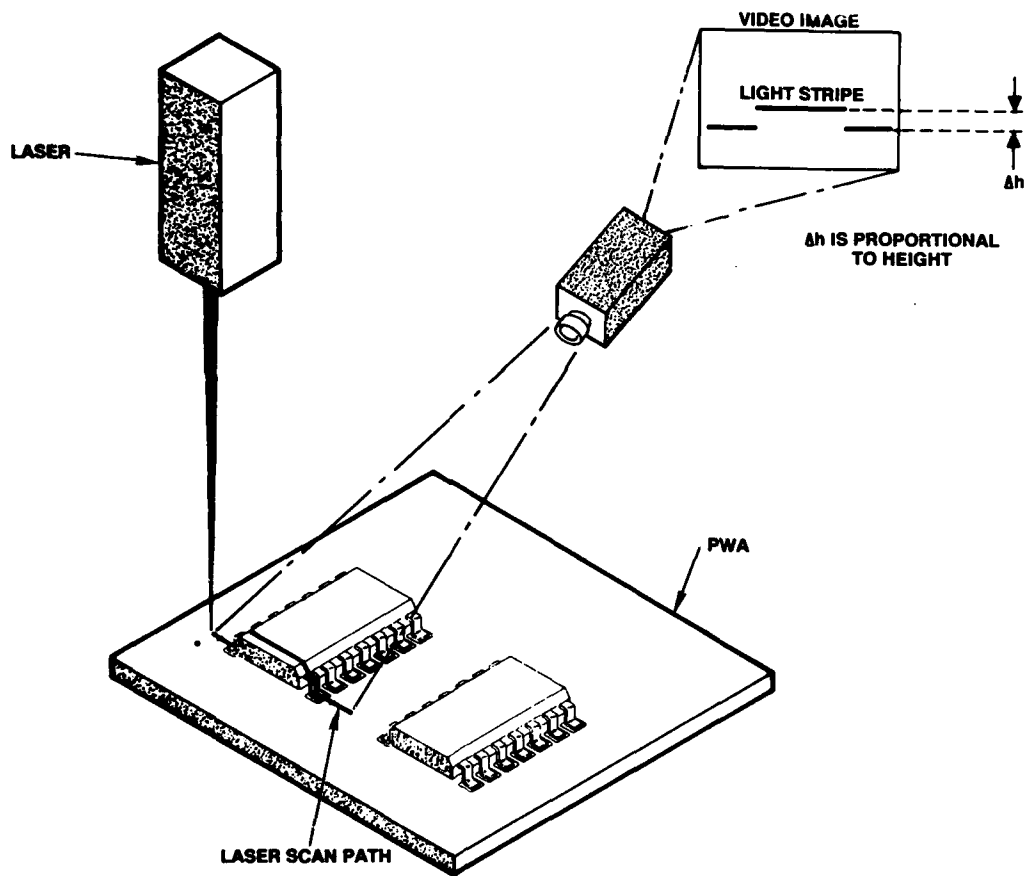


FIGURE 7. 3D Structured Light Vision System

Laser/Infrared. With the Laser/Infrared technology, the laser heats up the solder joint from which the infrared camera detects the emitted radiation (Figure 8). The intensity of the radiation in relation to time is measured. This thermal signature is then correlated to the desired signature of an "ideal" joint.

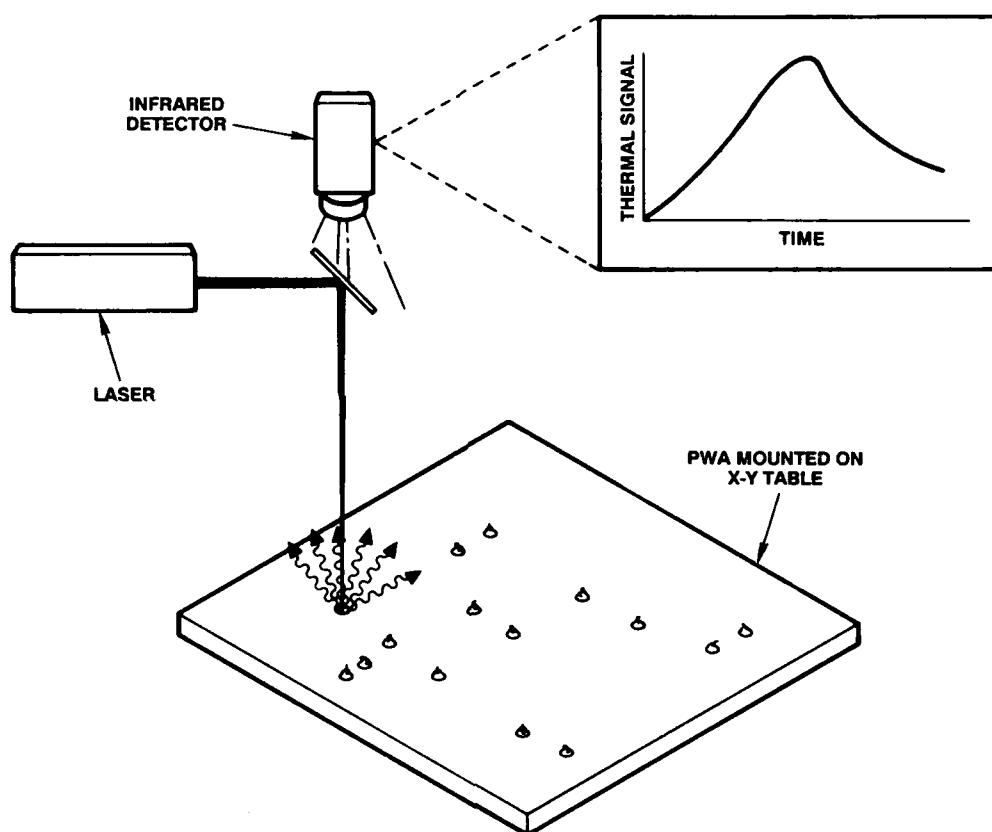


FIGURE 8. Laser/Infrared Detection System

X-ray. The x-ray source emits radiation which casts a differential shadow on an x-ray sensitive screen depending on the relative material thickness and density (Figure 9). The screen fluoresces in proportion to the amount and location of the x-rays. The screen is imaged by a low-level light camera translating the intensity of the fluorescence into grey levels where black is absence and white is saturated. Since a copper lead is not as dense as solder it will appear lighter for the same amount of thickness.

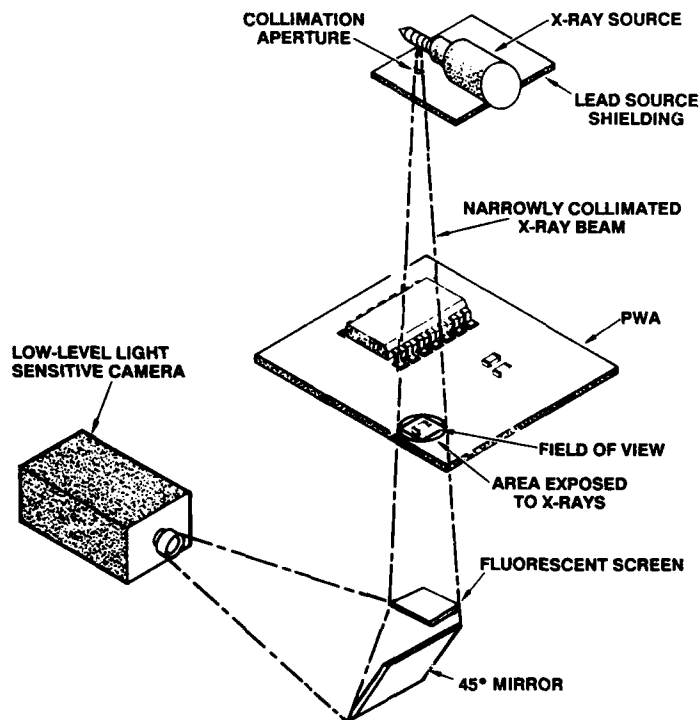


FIGURE 9. X-ray Imaging System

The four different technologies each have their benefits and drawbacks. Table 1 contrasts these differences.

	2D VISION	3D VISION/ STRUCTURED LT	LASER/ INFRARED	REAL TIME X-RAY
Camera	Video	Video	Infrared	Video
Source	Incandescent/ Fluorescent/ Strobe	Laser	Lasers	X-ray
Mirrors	No	Yes	Yes	Yes
Computer	Image Processor	Image Processor	Signal Processor	Image Processor
Price	Low	Moderate	Moderate	Moderate to High
Understand- ability of image	Easy	Moderate	Difficult	Moderate to Difficult
Filterable	Color selectable	None	None	Beam hardening
Reflectivity sensitivity	High	High	Low	None
Height/ thickness measure	Minimal indirect from edges	Indirect through projection	None	Indirect through grey level
Component shadowing	High	High	High	Moderate
Available internal info	None	None	Low	High
Algorithm programming required	Yes	Yes	No	Yes
Sensitivity to surface defects	High	Moderate	Moderate	Minimal
Classification of defects	Yes	Yes	No	Yes
Image clutter	Moderate	Low	Low	High *
Position sensitivity	Low	Low	High	Low

* Especially true for PWAs with components on both sides.

TABLE 1. Comparison of Inspection Technologies

VARIATIONS IN AUTOMATED INSPECTION TECHNIQUES

TEMPLATE MATCHING

In this method a "golden" board is used to compare to all other boards. Images of each section of interest are saved and compared to the same locations of the board under test at run-time. Correlation/registration must be done in order to precisely match up the two images. Once this is done, the two images are subtracted and the resultant image contains only the differences between the two images. Any deviations from the "golden" board images are assumed to be defects (Figure 10). The advantage is that the resultant image contains only differences and effectively eliminates any common background areas. If indeed the resultant image had only the defects, this would be very easy to analyze. This technique works for very uniform objects, such as inner layers of a bare board, but unfortunately in the world of solder, there is a large range of acceptable solder joints, especially for PTH components. Defects are not characterized only by location and size, but shape as well. The amount of solder for a good PTH solder joint can vary by as much as 100%. This makes the image subtraction technique unworkable (Figures 11 and 12). The correlation/registration routine is very compute intensive in software, but can be implemented in hardware. Also, saving the "golden" board images requires massive amounts of disk space which means slow access (1/4 mbyte per image with an average of 200 images). This could be alleviated by leaving the "golden" board in the inspection machine and viewing each section on both boards before moving to the next view. This roughly doubles the mechanical motion time of the inspection. Finally, this technique does not provide for broad fault coverage (identification of defect type) and thus is not optimum for process control.

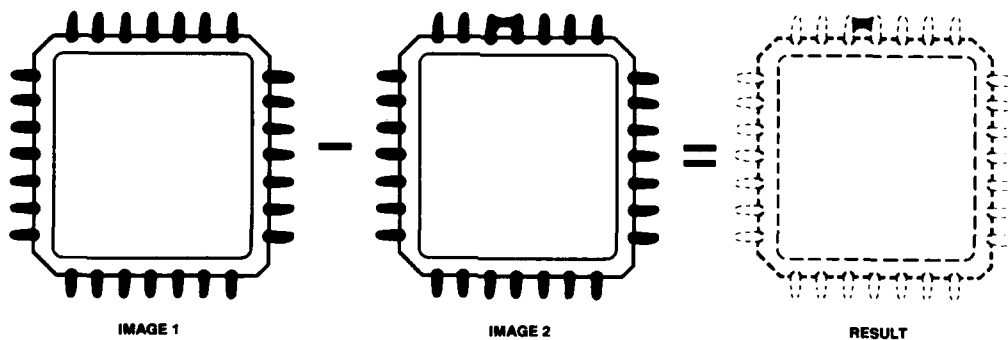


FIGURE 10. SMT Theoretical Image Subtraction (Template Matching)

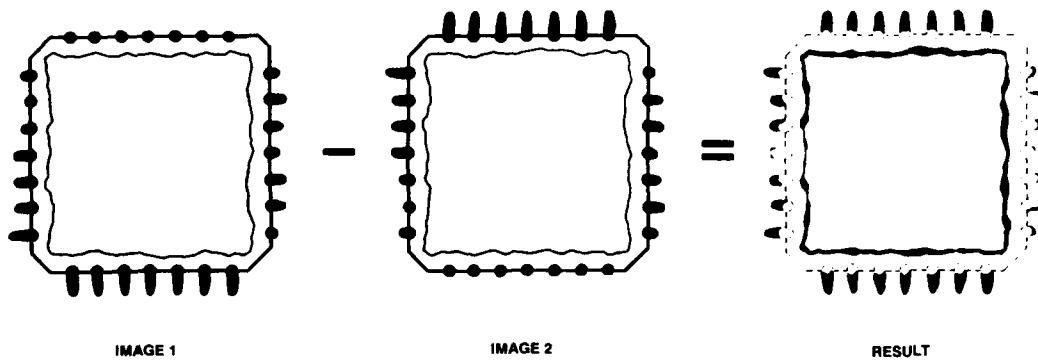


FIGURE 11. SMT Real-Life Image Subtraction (Template Matching)

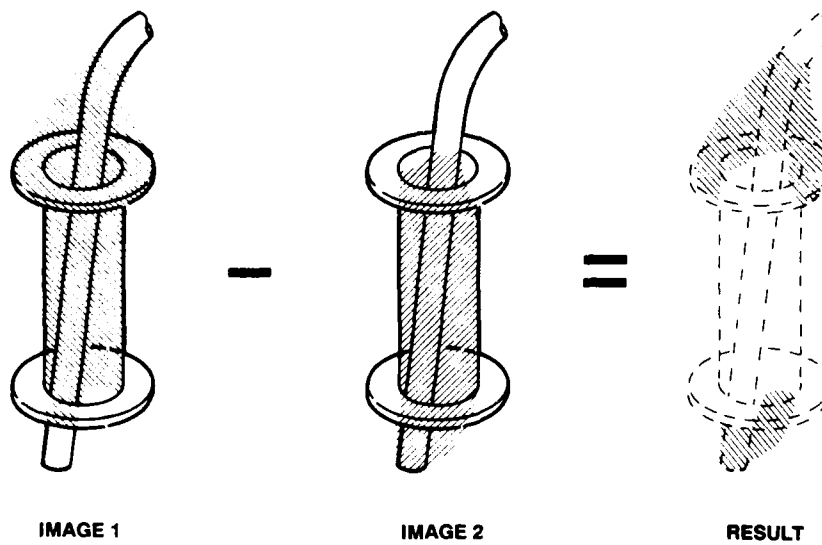


FIGURE 12. PTH Real-Life Image Subtraction (Template Matching)

FEATURE EXTRACTION

Typically this is done by picking a number of distinguishing features (on the order of 5 to 20) that correlate to the defects of interest. These are then run on each solder joint from a number of PWAs with a good sampling of defects, and the feature values saved. A large enough sample of defective joints and good joints is necessary in order to obtain statistical validity. The data is plotted and those features which distinguish between good and bad solder joints with at least one sigma difference are chosen as the distinguishing features for that defect type. The hope is that enough features will combine to make a three sigma distinction. The features of interest may need to be ANDed or ORed together, and weighted in order to achieve some combination for best defect recognition. Advantages are that once a good set of features are identified, only the statistical gathering and feature combining need be done. Features that have proven successful in other applications are: major over minor axes, binary area number of blobs, length of major axis, number of edges, number of peaks and valley: in a profile, etc. (Figure 13). Disadvantages are that features may be too general to find subtle defects, and "tuning" of the feature extractors is necessary.

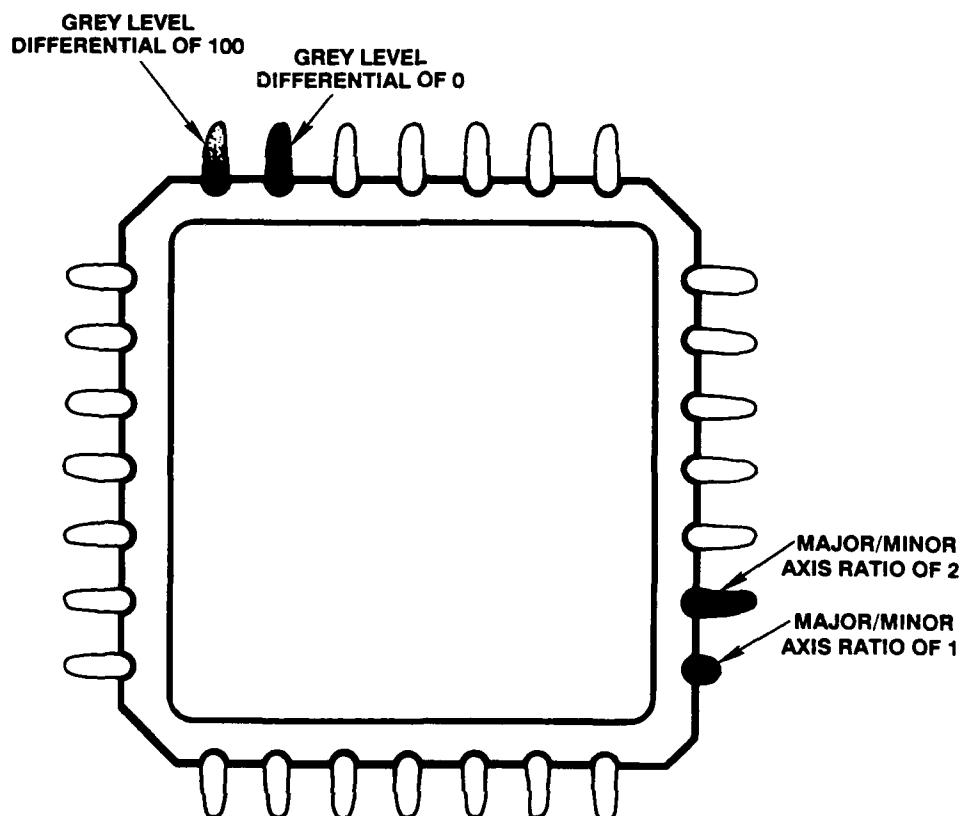


FIGURE 13. Feature Extraction

RULES-BASED MEASUREMENT

This technique is similar to feature extraction in that it measures features, but here the actual value is of more importance as it is compared directly to known physical dimensions rather than comparing to good and bad examples (Figure 14). Since measurements are taken and tested against known criteria, large sampling is not needed as in feature extraction. Sampling is needed only to assure that measurements are accurately taken over the range of solder joints that heights, thicknesses and areas are measured. Measurements can be taken where something is meant to reside in order to detect its presence and conversely, measurements can be taken at locations where nothing is to reside in order to assure no contamination. Advantages are that it is generally easier to relate to physical measurements than to more abstract features such as number of peaks/valleys in a profile. This can make algorithm development less "hit and miss", as it is easier to know if an algorithm will perform the desired task. Additional advantages are that the broadest fault coverage is achieved and quantitative measurements of these faults can be directly applied to closed-loop manufacturing process control. When measurements can be taken, this is the most accurate and straight forward approach. Problems occur when non-standardization exists in board layout, board design, or component manufacturing. These push the algorithm design to be tailored to the component and/or board which results in increased development and tuning time.

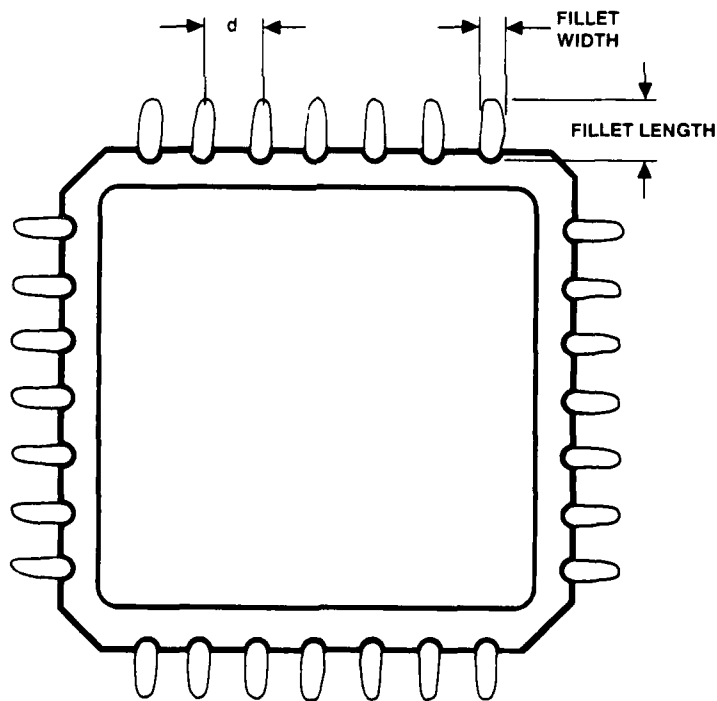


FIGURE 14. Rules-Based Measurement

BOARD LAYOUT OPPORTUNITIES AND ISSUES

General Rules. Uniform layout rules will maximize effectiveness of inspection software across a manufacturer's product line. Minimizing differences allows for more general purpose software.

Trigonometric Considerations. Component positioning is critical. In most SMT applications, and some PTH applications, only the plan view (view from directly above the PWA perpendicular to the PWA surface plane) is needed. Unlike contact technologies that have height limitations dictated by probe technology, non-contact technologies restrict height in respect to their surrounding devices only if tilt view inspection is needed. When tilted views are needed, *minimize shadowing* of neighboring components by keeping component height down. Maximize inspection viewing by allowing adequate spacing between components and the board surface for leads under dense components, or design components with leads that extend beyond the package outline such as gull wing leads (Figure 15).

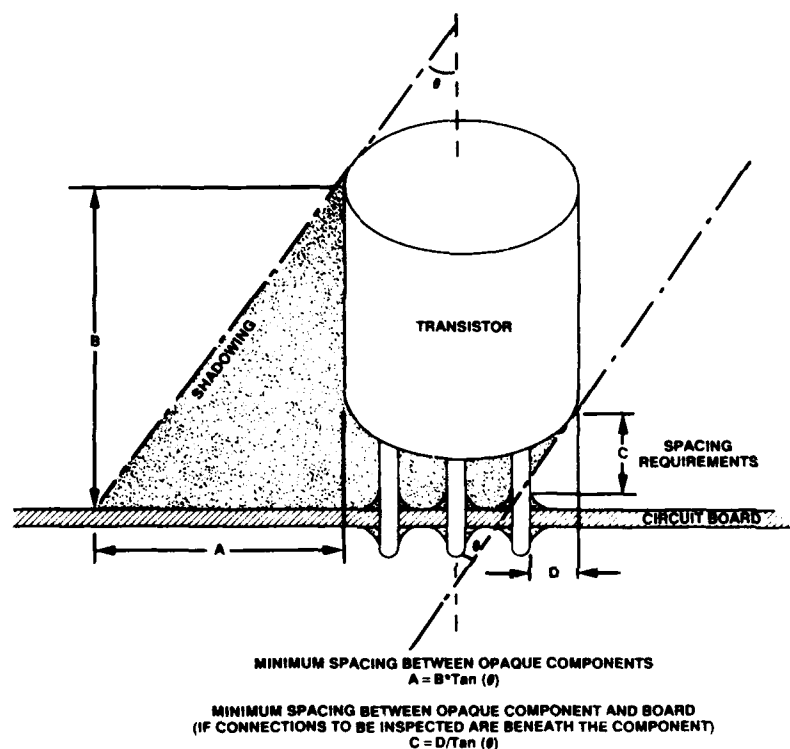


FIGURE 15. Spacing Requirements for Inspection of Connections Under Components (With Shadowing)

Uniform Geometry. Uniform land patterns minimize the inspection software by decreasing the number of special conditions. Make all pads rectangular or circular, if possible, and standardize on sizes. Special "T" or "L" patterns necessitate extra inspection software.

Minimize Component Types. The fewer the component types the fewer variables, and thus the faster will be the programming setup time for automated inspection.

Minimize Hidden Features. Hidden Vias or dense inner-layer traces near solder joints can affect the overall x-ray signature of the solder joint and result in decreased inspection reliability. Inner layers should be as uniform as possible especially near the solder joints.

Cluster Discretes. Minimize the number of inspection views by clustering discretes together when possible. This will help minimize inspection throughput with no adverse affect on reliability.

Datums. High accuracy datums allow for re-registration to account for fixturing, board, and art work tolerances. Datums optimally should be two square pads of approximately 0.050 inches on a side and connected at a single corner (as in opposite squares in a 2 x 2 checker-board). They should be tinned to allow for radiographical as well as visual imaging. There should be three of these, each placed at an extreme corner of the board to allow for optimum registration.

Mask Exposed Metallization. Exposed metallization such as ground planes or traces should be masked. Unmasked ground planes result in non-uniform solder coverage and can affect the reliability of x-ray inspection. Unmasked traces will also be non-uniform and can be confused as shorts. These can be compensated for, but only at a programming cost to handle each trace as a special case. Some reduction in performance should also be expected.

PTH BOARD LAYOUT OPPORTUNITIES

Masking Pads. For PTH components it might be considered possible to mask the top pad or possibly top and bottom pads. This would reduce the number of bridge defects, allow for denser component spacing, and give more information for x-ray imaging without tilting the PWA. Since presence of a minimum quantity of solder in the barrel can be verified radiographically, the structural and electrical integrity of the solder joint would likely not be compromised by deletion of the solder fillet wetting to the pad.

SMT BOARD LAYOUT OPPORTUNITIES

ICs Straddling Discretes. ICs straddling discretes can be radiographically inspected for low density ICs (Figure 16).

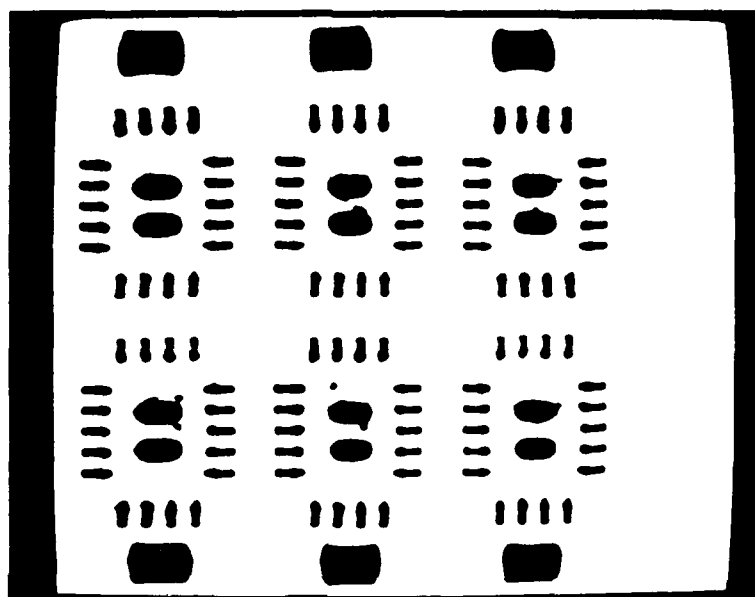


FIGURE 16. ICs Straddling Discretes

Tinning Pads. Many of the defect measurements are taken relative to the pad, which means precise locating of the pad for the best defect detection reliability. Therefore, it is necessary to get a clear image of the pad edge. Pads should be tinned with at least 0.001 inch of solder.

COMPONENTS ON TOP AND BOTTOM

Multi-layer PWAs with components mounted on both the top and bottom of the PWA (also referred to as double-sided assemblies) present unique challenges for x-ray inspection due to x-ray's transmissive rather than reflective nature. X-ray images combine the information on both surfaces as well as the inner layers. This double-sided layout should be avoided when possible. When not possible, we suggest the following guidelines.

Mirror Image Placement. Mirror image placement of components is where identical packages are placed on both sides of the PWA in the same relative X/Y position so that when viewed radiographically they appear as one component. Inspection here necessitates laminates thick enough to trigonometrically separate the top and bottom pads when viewed at a tilt. Use $\text{Thickness} = \text{pad width} / \tan 40^\circ$ as a minimum.

Stagger Non-Quad Packages. Non-quad packages such as SOICs can be staggered so that the solder joints of a component on one side of the board match up with the centerline of an SOIC on the opposite side. This may permit inspection without tilting the PWA.

Discretes Opposite ICs. Discretes can be placed on one side of the PWA so that they line up with the center of a Quad or SOIC on the opposite side. This allows for clear viewing of the solder joints for both components.

Flex Joints. One solution to double-sided inspection is the flex joint. Flex joints allow for the PWA inspection to be treated as two separate single-sided PWAs, and then joined after inspection (Figure 17). Additional connections between boards can be through edge connectors. Reliability may be a problem for this technique when PWAs are used in rugged applications, but for some commercial applications this may be a very valid technique.

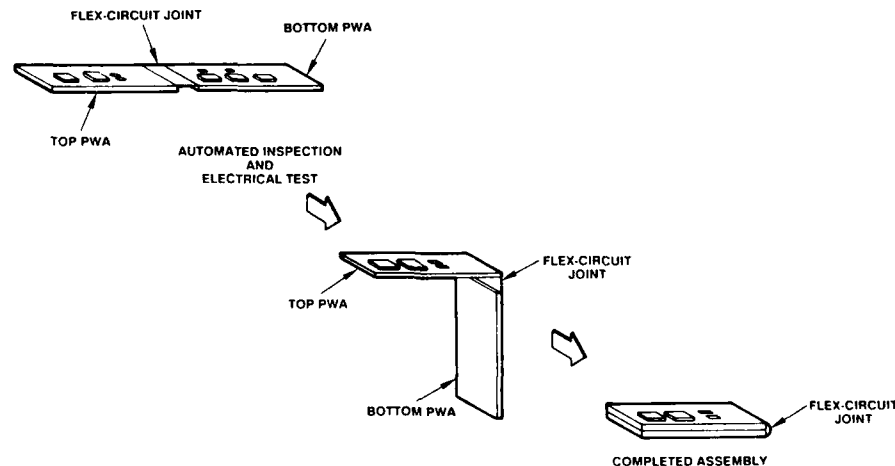


FIGURE 17. Double-Sided Assembly Using Flex-Circuit Joint Concept

Other Strategies. Some locations may not be inspectable due to obstruction. For process control purposes, a statistically meaningful sample is all that is needed. When 100% inspection is required, consider human inspection of those few areas uninspectable automatically. Also, consider modeling the PWA layout from CAD data before final design for verification of inspection coverage (Figures 18 and 19).

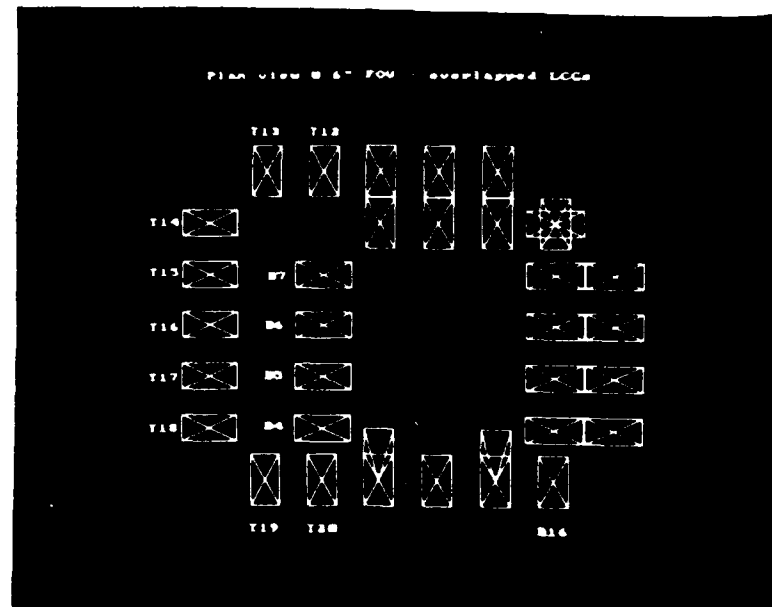


FIGURE 18. Double-Sided Modeling (Plan View)

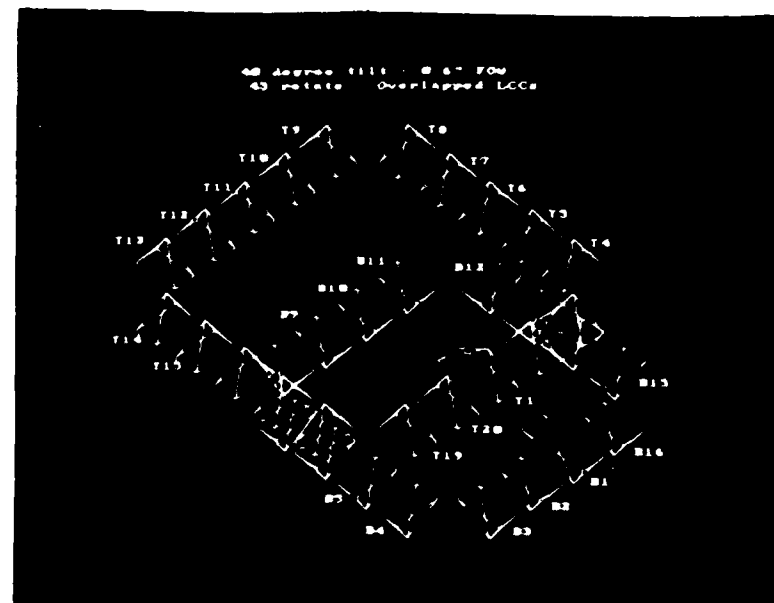


FIGURE 19. Double-Sided Modeling (Tilted/Rotated View)

PACKAGE DESIGN OPPORTUNITIES

Tolerance Band vs. Inspection Accuracy. A tightening of specific package tolerances will offer an improvement in automated inspection accuracy. External as well as internal package features should be standardized at least in the region of inspection.

Package Outline. Package outlines should be consistent in dimension relative to the solder joint location. It is often useful to reference from the package edge for automated inspection positioning. When package outline tolerances cannot be kept minimal, consider keeping the package body away from the solder joints rather than overlapping. Overlapping can make plan view inspection difficult or impossible, and necessitates tilted viewing of the PWA.

Lead/Metallization Geometry. Geometry (including thickness) of leads or of leadless package metallization will directly affect solder measurement in these areas. Solder width may indicate amount of solder, but if the lead thickness changes, the ratio of solder thickness to lead diameter for the same width measurement changes. Mixing lead diameters for the same component will make for unreliable measurements.

Lead/Metallization Composition. For x-ray inspection, lead composition will have additional influence on the measurement. Since material density directly affects the digital grey level, the various densities of different materials will show as different grey levels for the same thickness. If composition is known, thickness can be indirectly measured.

Castellations. Leadless package castellations, at present, vary significantly in depth, width, and height. Control of these parameters is required if measurements are to be made which pertain to the castellation.

Package Makeup. Package thickness and material composition will affect the ability to reliably detect package edges radiographically. Thin packages or packages of low density will present less contrast against the background and thus present a more difficult job of locating the edge precisely. 2D imaging necessitates high color contrast between the package and the substrate.

Variations in the internal design of chip carriers, such as lead frame geometry and composition, will influence x-ray inspection for double sided component mounting.

X-ray Inspection with Lid Seals. Plastic or ceramic lids are preferred over KOVAR due to their greater transparency to x-rays. It is best to migrate the lid seal away from the solder joints so that unobstructed viewing is allowed without tilting the PWA (Figure 20). Throughput increases when multiple viewing angles are eliminated. If a KOVAR lid with solder seal is not needed, consider a substitute for the solder lid seal that would be more transparent to x-rays (Reference 12). Fully ceramic (CERPAK) or aluminum (Metal Chip Carrier) packages generally would provide excellent x-ray transparency (Reference 11).

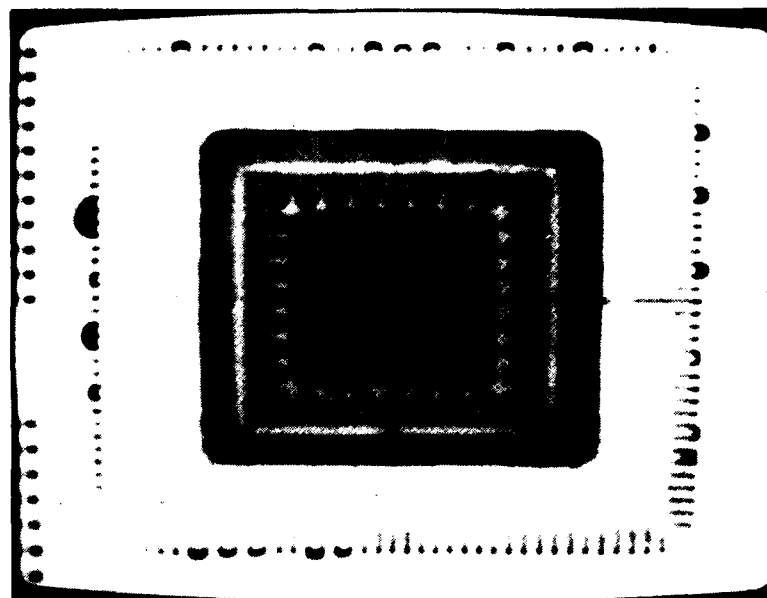


FIGURE 20. Lid Seal Away From Solder Joints



FIGURE 21. Tilted/Rotated View of LCCC Showing Long Pin 1

FEATURES

Orientation Reference. Internal or external orientation references are acceptable, but should be consistent for standard JEDEC package. Orientation features that are both visibly and radiographically identifiable are preferred. These would include cutouts on ICs and the bulbous end of PTH radial leaded capacitors. X-ray specific references would be an LCCC long pin 1 (Figure 21) and the internal structure of Tantalum capacitors. A vision-specific reference would be a painted dot on the top of an IC.

Component Verification. Visually and radiographically visible package markings should be developed and standardized to facilitate component verification. Lead paint using highly distinguishable symbols instead of numbers and letters could be used. Symbols such as circles, triangles, crosses, dots and lines are suggested.

NEW PACKAGES

Pad Grid Arrays. Pad Grid Arrays are surface mounted Pin Grid Array equivalents. They have an array of bump type solder connections. These devices would minimize footprint and inspection, but inspection would be limited to x-ray.

Non-Castellated LCCC. Non-castellated LCCCs are LCCCs without the metallization up the sides. The connection would be restricted to the hidden region, thus eliminating the high variability of the solder castellation (Reference 17). Decreased use of board area is an added benefit. Inspection would again be limited to x-ray.

CONCLUSION

The issues which have been presented reflect opportunities which have been selected as either specific recommendations or areas for further discussion within the electronics industry. Forums for such discussion should include, but not be limited to, the Tri-Services' manufacturing technology and solder quality centers, the IPC, JEDEC, and international standards organizations. Ultimately, the manufacturer has the greatest leverage toward achieving a positive change. This will come through internal change and standardization of design rules which are beneficial to inspection. Imposing requirements upon substrate and component vendors for standardized and more tightly toleranced parts, where desirable, should also take place.

Some of the opportunities discussed carry a price. This may come from reductions in assembly density, changes in layout practices and tolerancing, and tighter control on component variability. In order to achieve the highest potential of inspection effectiveness, an up-front price may need to be paid.

We have had the opportunity to review the inspection issues impacting many hundreds of PWAs. These assemblies reflect a substantial crosssection of current PTH, SMT and mixed technology products in both the defense and commercial community. Through such an extensive sampling of products, patterns emerge which permit relevant generalizations to be made. Nevertheless, we recognize that only through industry-wide forums can all facets of the design-manufacture-inspection picture be fully revealed.

As the electronics industry rushes headlong toward assembly and packaging technologies which provide the required density, performance, and/or alleged reliability improvements, the value of taking the time to fully address the consequences of these changes must be recognized. An electronic assembly, whatever its application or mission, will ultimately be competitive only if its **entire** life-cycle cost and performance adds up favorably against its competition. High yield will only be possible when PWAs are designed for manufacturability. Assuring high first-pass yields, through process control, necessitates design for inspection. Full maturation of electronic assembly technology can only be attained through design for manufacturability **and** inspection.

We have discussed how specific PWA layout opportunities and component feature issues will significantly impact automated inspection technology's effectiveness. As described earlier, effective inspection is viewed as critical to both minimizing production cost and maximizing product reliability. Whenever inspection technology cannot fully support a complex, manufactured product in these ways, the assembler has ventured into areas of indeterminate risk. The design of electronics for automated inspection is now a relevant, worthwhile and ongoing issue. Broad participation by industry is necessary to implement the standards needed to achieve high reliability through design.

BIBLIOGRAPHY/REFERENCES

1. M. P. Seah and C. Lea; "Certainty of Measurement using an Automated Infra-Red Laser Inspection Instrument for PCB Solder Joint Integrity"; Teddington, Middlesex, UK; National Physical Laboratory.
2. T. D. Doan; "Infra-Red Technology for Automated Inspection of Lap Solder Joint"; Naval Weapons Center, China Lake, CA.; February 1987; NWC TP 6789; 11th Annual Electronics Manufacturing Seminar Proceedings.
3. Douglas H. Ensign; "Laser Inspection Calibration Baseline for Thermal Signature Analysis"; Naval Weapons Center, China Lake, CA.; February 1987; NWC TP 6789; 11th Annual Electronics Manufacturing Seminar Proceedings.
4. Mike Juha; "Improving SMT Circuit Board Inspection with 3D Vision"; Naval Weapons Center, China Lake, CA.; February 1987; NWC TP 6789; 11th Annual Electronics Manufacturing Seminar Proceedings.
5. Patrick E. Casey; "X-RAY Inspection"; July 1987; Manufacturing Systems.
6. Edward W. Soron; "X-Ray Inspection Meets Increased PWB Throughput, Density Challenge - Part 1"; October 1987; Electri-onics Electronic Edition.
7. S. Leonard Spitz; "Automated Inspection Systems Reveal Loaded PCB Flaws"; December 1986; Electronic Packaging & Production.
8. The Institute for Interconnecting and Packaging Electronic Circuits; *User's Guidelines for Automated Solder Joint Inspection Systems*; Lincolnwood, Illinois; February 1987; IPC-AI-641.
9. Scott T. Jones; "Automatic PCB SMT Inspection - an Update"; Premiere Issue 1986; Printed Circuit Assembly.
10. Philip J. Klass; "Automated Military Avionics Factory Reducing Flaws in Workmanship"; October 26, 1987; Aviation Week & Space Technology.
11. Technical Staff, Integrated Circuit Engineering Corporation; "Surface Mount Packaging Report"; June 1986; Semiconductor International.
12. Jerry Lyman; "Packaging"; October 16, 1986; Electronics.
13. Lockheed Electronics Company Inc.; *The Dynamic Measurement and Functional Inspection of Solder Joints*; Plainfield, N.J.; December 1976; Product Assurance Directorate, Picatinny Arsenal, Dover, N.J..

14. Dr. Donald C. Mead; "Machine Vision in SMT"; September 1987; Assembly Engineering.
15. Alan Rotman; "The Veneration of the Topside Fillet"; September 1987; Printed Circuit Assembly.
16. Jeffrey S. Braden; "Advanced Surface Mountable Packages for VLSI Devices"; November 1987; Semiconductor International.
17. Jane Hallisey; "SMT Reliability: Interviews With the Experts"; November 1987; Circuits Manufacturing.
18. Jerry Lyman; "New Lead Scheme Saves Board Space"; January 8, 1987; Electronics.
19. Jerry Lyman; "Military Moves Headlong into Surface Mounting"; July 10, 1986; Electronics.
20. J. T. Lynch; *Surface Mount - Where are the Standards?*; 1987; IEEE 0569-5503/87/0000-0064.
21. Michael Negin and Nello Zuech; *Review of Vision System Techniques for Inspection of Electronic Components*; 1985; IEEE 0569-5503/85/0000-0474.
22. Allen Fridge, John Lee, Jr., and Richard Walker; "Automated Optical Inspection of Hybrid Circuitry"; Montgomery, Alabama; 1984; Proceedings of the 1984 International Symposium on Microelectronics.

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THERMAL ANALYSIS OF PCB USING SINDA AT EMPF

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ABSTRACT

Thermal design soundness of printed circuit boards (PCB) is the key reliability factor of the system. The Computer Integrated Manufacturing Department (CIM) of the Electronics Manufacturing Productivity Facility (EMPF) is developing pre- and postprocessing software that will interface the System Improved Numerical Differencing Analyzer (SINDA) with PCB computer-aided design (CAD) databases. This will enable the user to generate a SINDA input deck and perform thermal analysis on the mainframe and graphically display the temperature profile in color.

Preprocessing consists of two steps: In the first step the PCB CAD database is converted into a thermal database. In the second step the thermal database is converted into a SINDA input deck. Once the thermal analysis using SINDA is done, the postprocessing is performed to display temperature profiles.

The two-step operation of preprocessing makes the SINDA input deck preparation easier by setting up the thermal database and making the software more machine independent. In other words, once the thermal database is created in the first step, the second step of converting the thermal database into a SINDA input deck is independent of hardware.

The EMPF is also using SINDA to simulate the rework process of a solder joint using the Metcal soldering iron tip. The SINDA input deck was prepared, and the output from the simulations is displayed using Fortran program, which utilizes Graphic Data Display Manager (GDDM) subroutines, the IBM 4381 mainframe computer, and color terminal.

The experimental backups for the verification and validation will be performed. For PCB the results of thermal profiles obtained through the software postprocessing and the experimental thermograms would be compared. All the results and the software source code will be available to the U.S. industry.

INTRODUCTION

There are two reasons why thermal stresses cause electronic components to smoke. First, they are highly susceptible to extremes of temperature. Second the thermal factors are often neglected during the systems development. This calls for in-depth study of thermal problems associated with electronics hardware. The finite element analysis backed up with appropriate experimental testing for verification and validation of software is described in

this paper. The proposed analytical method provides two- and three-dimensional colorgraphic output for a timely analytical description of the PCB temperature during operation in transient start, steady state, and shutdown modes.

Figure 1 depicts the approach being used by CIM Department of EMPF for the development of the software to do thermal analysis of PCBs. The conversion of PCB CAD database into thermal database is the first step. The PCB CAD database can reside on one of the several kinds of computer, for example, IBM PC, DAISY, CV, etc. This step is machine-dependent and at present it is being done on IBM PC. The board layout is drawn on PC using Quick Basic. It has associated database with complete geometric, electronic, manufacturing, thermal, and material data. This database is usually very big and converting it directly into a SINDA input deck will be a time consuming software project. Therefore, this database is scanned with software A to filter it to a thermal database.

The thermal database files are much smaller compared to PCB CAD database files since it consists only of thermal and geometric data needed to perform complete thermal analysis using SINDA. The next step is to convert the thermal database into SINDA Input Deck, which is in special format. In addition, we have to create the mesh size on the board, components, and remaining geometry.

SINDA uses a finite difference technique that is similar to the finite element method. The PCB is divided into several elements. Each element is called a node in SINDA and all nodes are compiled under NODE BLOCK. The heat transfer takes place by conduction, convection, and radiation. In conduction, the heat is transferred through the adjoining elements. The data are compiled under CONDUCTOR BLOCK. Then we need additional data in the form of subroutines to run SINDA in SINDA input deck.

The SINDA thermal analysis code resides on the IBM 4381 mainframe at the EMPF. For a simplified problem of 24 nodes under normal mainframe load, the time taken to do analysis is less than a minute. But for 2400 nodes the time taken is 15 minutes, and for a production problem of approximately 10,000 nodes the time is approximately 4 hours. The longer jobs can be run as a batch, overnight, or on weekends.

The SINDA output is then displayed on a computer in two fashions. First is the temperature-versus-time curve, and second is the temperature profile in color. These displays can be shown either on IBM mainframe or PC. All the hot spots can then be seen, and the PCB layout can be changed before it goes for manufacturing. This cycle is repeated until all the hot spots are removed, thus saving costly changes after manufacturing.

PREPROCESSING

The preprocessing of any finite element system is one of the most important part of the complete cycle. Any error made at this stage will be carried all the way down and will generate incorrect results. The main idea of preprocessing is to create the SINDA input deck from the PCB drawing. The PCB drawing can be on any system.

As explained earlier, this conversion is done in two steps. The first step is done by using software A and the second by software B. Software A depends on the machine on which the PCB layout is residing. For example, if the PCB is laid out on a DAISY Boardmaster, Software A will convert the DAISY Boardmaster layout to the thermal database. At present the PCB layout is drawn on IBM PC using Quick Basic, and then Software A written in Quick Basic also converts the PCB database into thermal database as shown in Figure 2. The thermal database format can also be called neutral system and is defined under THERMAL DATABASE FORMAT.

The second step in preprocessing is to convert the thermal database into the SINDA input deck, and this is done using software B as shown in Figure 3. The SINDA input deck is relatively complex and can be prepared in several different formats. Because of limited space in this paper, only one format will be discussed. Readers interested in details are encouraged to read the SINDA manual listed in the Bibliography.

THERMAL DATABASE FORMAT

HEADER, TITLE OF THE THERMAL PROBLEM ;
BOARD, A, B, C, M1 ;
COMPONENT, I, L, W, H, D1, D2, D3, P, Q, M2, M3 ;
LOCATION, I, X, Y, Z, T ;
MATERIAL, Mi, E, R, K, S ;

Geometric Properties

A,B,C = Length, Width, Height of the board
L,W,H = Length, Width, Height of the component

X,Y,Z = Cartesian coordinates of the component
T = Angle of the component insertion

D1 = Distance between the pads
D2 = Distance between the pad rows
D3 = Distance between the board and body of the component

All dimensions in inches

Material Properties

R = Density (lb/cubic inch)
K = Thermal Conductivity (BTU/in min F)
S = Specific Heat (BTU/LB F)

E = Emmisivity
Mi = Material name, M1 for the board, M2 for the lead and
M3 for the component

Other Symbols

I = Identification Number for each component
P = The number of pins on component
Q = Heat Source (BTU/Min)

Example of Thermal Database

HEADER, Thermal Problem Test1 ;
BOARD,6.0,4.0,.05,Epoxy ;
COMPONENT,1,2,1,1,3,1.1,14,2.4,Copper,Silicon;
COMPONENT,2,1,1,2,2,1.1,8,4.5,Copper,Silicon;
LOCATION,1,1,2,.05,0,0;
LOCATION,2,4,1,.05,0,0;
MATERIAL,Epoxy,.04,.14,.1,.23;
MATERIAL,Silicon,.03,.12,.07,.21;
MATERIAL,Copper,.02,.21,.3,.45;

SINDA INPUT DECK FORMAT

The SINDA input deck is mostly written in fixed format and the first two lines below represent the column numbers.

111111111222222222333333333344444
12345678901234567890123456789012345678901234

```
BCD 3THERMAL LPCS
BCD 3TITLE OF THE THERMAL PROBLEM
END
BCD 3NODE DATA
    1,T,rcv
    .....
    n,T,rcv
END
BCD 3CONDUCTOR DATA
    1,1,2,kA/d
    .....
    m,n-1,n,kA/d
END
BCD 3CONSTANTS DATA
    DTIMEI = 0.01, NLOOP = 50, DRLXCA = 0.05
    TIMEND = 20.0, OUTPUT = 1.0, NDIM = 5000
END
BCD 3ARRAY DATA
END
BCD 3EXECUTION
    FWDBKL
END
BCD 3VARIABLES 1
M Qi = BTU
END
BCD 3VARIABLES 2
END
BCD 3OUTPUT CALLS
    TPRINT
    SUB1(TIMEN,T1,T8,T11)
END
BCD 3SUBROUTINES
SUBROUTINE SUB1
WRITE (20,100) TIME, T10,T20,T30
RETURN
100 FORMAT (1X,8(F5.1,1X))
END
END
BCD 3END OF DATA
```

SINDA INPUT DECK EXAMPLE

The SINDA input deck example shown below was used to run a transient problem as shown in Figure 4.

```
BCD 3THERMAL LPCS
BCD 3THERMAL PROBLEM TEST1
END
BCD 3NODE DATA
    1,70.0,.6
    2,70.0,.6
    .....
    600,70.0,.6
END
BCD 3CONDUCTOR DATA
    1,1,2,4
    .....
    900,599,600,.4
END
BCD 3CONSTANTS DATA
    DTIMEI = 0.01, NLOOP = 50, DRLXCA = 0.05
    TIMEND = 20.0, OUTPUT = 1.0, NDIM = 5000
END
BCD 3ARRAY DATA
END
BCD 3EXECUTION
    FWDBKL
END
BCD 3VARIABLES 1
M   Q306 = .02
M   Q .....
M   Q320 = .02
END
BCD 3VARIABLES 2
END
BCD 3OUTPUT CALLS
    TPRINT
    SUB1(TIMEN,T1,T8,T11)
END
BCD 3SUBROUTINES
SUBROUTINE SUB1
WRITE (20,100) TIME, Ti
RETURN
100 FORMAT (1X,8(F5.1,1X)
END
END
BCD 3END OF DATA
```

ANALYSIS

Thermal analysis for this project is done using SINDA. This system was originally designed as a general thermal analyzer accepting resistor-capacitor (R-C) network representations of thermal systems. One of the most outstanding features of SINDA is that, in addition to accepting network description cards and other relevant values as input data, it also accepts "program-like" logic statements and subroutine calls as data, which ultimately permits the user to tailor the program to suit his or her particular problem.

These features of SINDA create a challenge for developing pre- and postprocessing software, in particular for PCB problems. The system structure of SINDA is similar to that of the engineering environment. The engineer supplies input data and receives output data, as shown in Figure 1.

Changes to the logic and equations are difficult for the program user to implement conveniently because they must be written in a computer-oriented language and must be submitted through a formal programming organization. When SINDA is used, however, the engineer need only call on the programmer to supply a procedure, which will call into action the various elements of the system in the proper sequence. The engineer then formulates the problem in SINDA language, assembling both data and solution technique (i.e., FORTRAN logic and equations) into a file, which then serves as the complete input. By using the software flow described in Figure 1, the designer can accomplish the same task, particularly for the routine PCB thermal problems.

POSTPROCESSING

Once the thermal analysis is complete the results are displayed. This is done by Software C which converts the SINDA output files into a graphics display. The temperature profile at a given time is displayed as shown in Figure 5.

For transient problems, the temperature and time graphs are made as shown in Figure 6. Eventually the temperature profiles change color with real time or with a user-selected time scale for the PCB and will be displayed in animation or motion picture.

VALIDATION

This software system will be validated by testing two or more boards that fall within the followingspecifications:

- PCB size of 4 inches by 4 inches or less
- At least one surface mount device
- At least one through hole board
- One very simple PCB (approximately four components) and others more complex with 10 or more discrete, axial lead components and one or more ICs
- The board to be easily connected to a 5-VAC power supplyand be functional
- Simple sequential design incorporating flip-flops.

INTRODUCTION TO METCAL SOLDERING IRON PROJECT

The EMPF is currently using SINDA to simulate the rework process of a solder joint using the Metcal soldering iron tip. The output from the simulations was a file of time and nodal temperatures. Such temperatures can be displayed using a FORTRAN program, which utilizes the IBM GDDM subroutines, a color terminal and run on the IBM 4381 mainframe computer.

The initial SINDA input deck was created by the Thermal/Structures Branch of the Naval Weapons Center (NWC) for the EMPF. The input deck, in addition to SINDA, was loaded on to the EMPF mainframe from the NWC central VAX/VMS in March 1987. At this point, the input deck was expanded and fine-tuned to better fit the needs of the projects at hand.

Since then, the input deck has been applied to two projects. The Vanzetti LI6000 laser solder joint inspection equipment project is still in process. The Metcal soldering iron project, addressed here, was the simulation of the rework process of a solder joint using the Metcal soldering iron tip. This was done to quantify the time required for reflow of a solder joint and thus reduce the chance of overheating the board or component.

In this section, the details of the input deck networks will be presented as will the results of the SINDA input deck run.

CONFIGURATION OF THE SOLDER JOINT NODAL MESH

To perform a finite differencing analysis, we first need to define the geometry of the object or objects being analyzed and generate the nodal mesh that represents it. The nodal mesh must closely represent the geometry of the object or the results will be misleading.

The thermal profile of this solder joint has a plane of symmetry down the center of the component lead. The soldering iron tip has a similar plane of symmetry down its center. Therefore, only one-half of the solder joint, PCB, component lead, and soldering iron tip had to be modeled when using their respective planes of symmetry. This method of modeling allowed us to save computer compilation time and memory space. The modeling also made alterations to the input deck less cumbersome and time-consuming.

The modeling resulted in a nodal mesh with the appearance of a cutaway view. Thus, to have meaning, the graphics have the same appearance that allowed the user to view the complete solder joint and soldering iron tip temperature profiles. In other words, the user can watch the heat flow through the center of the nodal meshes.

The overall dimensions of the solder joint nodal mesh, including the board, are 0.5 inch by 0.1 inch thick. The dimensions of the solder joint are 0.075 inch across on the board surface, 0.034 inch across as it passes through the board, and 0.100 inch thick measured on the cross section. The board is 0.060 inch thick and the lead is 0.020 inch wide and 0.100 inch long. The configuration is shown in Figure 7.

The nodal mesh is configured in a semicircular pattern. The nodes are formed by making vertical radial cuts starting at the center of the copper lead. In addition, vertical concentric circular cuts are also made giving the mesh a dart board appearance when viewed from the top. The mesh was layered to complete the nodal mesh and was done to more accurately duplicate the geometry of a solder joint and, thus, its response to a thermal input.

The result was four layers of PCB and ten layers of solder joint and component lead. There are 256 nodes for the solder, 80 nodes for the component lead, and 392 nodes for the PCB. With the addition of the surrounding air, the total number of nodes was 729 for the solder joint alone. Figure 8 is a three-dimensional view of the nodal mesh.

CONFIGURATION OF METCAL SOLDERING IRON TIP MODAL MESH

To simulate the soldering iron tip, another nodal mesh had to be generated. The Metcal soldering iron tip is 0.5 inch long and 0.188 inch thick at the heating element. This tapers down to 0.014 inch at the very tip (Figure 9). The nodes were formed by cutting--perpendicular to the plane of symmetry--the soldering iron tip into nine layers. Each layer was then cut into ten sections. The resulting nodal mesh had a total of 90 nodes. Figure 10 is a three-dimensional view of the nodal mesh.

REWORK INPUT DECK

The complete input deck, solder joint, and soldering iron tip has a total of 819 nodes. Nodes 1 through 320 represent the PCB. Similarly, nodes 321 through 576, 577 through 728, and 901 through 990 represent the solder joint, component lead, and soldering iron tip, respectively. Node 1000 is the boundary node which represents the surrounding air. Figure 11 is a reduced view of the solder joint nodal mesh with the node numbers inserted into the view.

Free convection and radiation cooling were included in the input deck on the top and bottom surfaces of the board and solder joint. These factors were not included in the tip portion of the input deck, but were, however, taken into account by adjusting the heating element power input and the initial temperature profile of the tip. The latter was derived by experimentally using a video infrared system.

MATERIAL PROPERTIES USED

The materials used in the input deck were fiberglass epoxy in the PCB, copper in the component lead and soldering iron tip, 63-37 tin lead solder, and air for the boundary node. The material properties needed by SINDA are the thermal conductivity (k) in Btu/in³-°F and the product of the density times the specific heat ($\rho \cdot C_p$) in Btu/in-s-°F. The material properties used are given in Table 1.

TABLE 1. Thermal Properties Used in the SINDA Input Deck.

Material	Temperature, °F	Thermal conductivity (k), Btu/in ² /°F	Density × specific heat (ρ C _p) (Btu/in ³ -°F)
Fiberglass epoxy	0.0	0.2142E-05	0.1218E-01
	5000.0	0.2142E-05	0.1218E-01
Copper	0.0	0.5350E-02	0.2972E-01
	5000.0	0.5350E-02	0.2972E-01
Solder	0.0	---	0.1290E-01
	32.0	---	---
	68.0	0.6607E-03	---
	100.0	---	---
	158.0	0.6607E-03	---
	200.0	---	---
	284.0	0.6271E-03	---
	360.9	---	0.1290E-01
	361.1	---	0.1780E-00
	464.0	0.3025E-03	---
	788.0	0.3920E-03	---
	5000.0	---	0.1780E-00
Air	0.0	---	---
	32.0	3.2407E-07	1.1313E-05
	68.0	---	---
	100.0	3.5648E-07	9.8843E-06
	158.0	---	---
	200.0	4.0278E-07	8.3738E-06
	284.0	---	---
	360.9	---	---
	361.1	---	---
	464.0	---	---
	788.0	---	---
	4000.0	---	2.0197E-06
	5000.0	4.0278E-07	---

In addition to the change in the material properties at various temperatures, the change in phase of the solder that occurs at 361.0°F was also included. The heat of fusion--the energy required to change solder from the solid to the liquid phase--was taken into account. The value for the heat of fusion used in this input deck was 28 Btu/lb.

RESULTS FROM REWORK INPUT DECK RUN

The SINDA output file is in the form of temperature and time. For small input decks, this is a usable form, but for larger input decks the output is too cumbersome to use. For this

reason, a subroutine was written and added to the SINDA input deck to write the time and temperatures for each output time step into a separate output file in a format that could be read easily by a FORTRAN program. At this point a Graphical FORTRAN program had to be written to display the results in a form that could be used.

The resulting program utilizes GDDM subroutines. Because of the difference in the size and the maximum and minimum temperatures of the soldering iron tip and solder joint, it was decided to keep them in separate displays. The solder joint appears as a combination of the top and cutaway side views of the joint. The two views are shown--separated in Figure 12 and joined in Figure 13. The three input deck materials--solder, copper, and fiberglass epoxy--are included in the resulting view along with a color key related to the temperatures, giving the user an overall showing of the solder joint temperature profile.

The soldering iron tip display appears in much the same way. A side view of the tip mesh with a temperature/color key is shown in Figure 14. For examples of either of these displays, contact John Guy at the EMPF.

An animation program is being worked on that will show a series of views allowing the user to see the temperature profiles in a time sequence.

Because color views could not be used in this paper, Figure 15 shows a simplified relationship of temperature to time. The figure shows the maximum, minimum, and average solder node temperatures with respect to time.

Although this plot does not show the temperature profile, it shows how the solder reacts under this thermal input. The maximum temperature rises quickly to about 570°F while the minimum temperature reacts much more slowly. In addition, the minimum temperature holds constant between 1.125 and 1.275 seconds as the node goes through reflow.

CONCLUSION

These projects will be of great value to the EMPF as well as to the electronics manufacturing industry. Since its founding in 1984 the EMPF has led a cooperative effort between electronic equipment manufacturers, product manufacturers, and Government agencies to research and test electronics manufacturing processes and materials. We at the EMPF have benefited from this type of research and will continue to pursue it--and share it--in the future.

We believe that the time has come to use computers efficiently at the design and manufacturing stages of a PCB. By doing so, we can help to eliminate the hit-and-miss approach to predicting the location of hot spots in a new PCB design as well as determining what will be required for its rework.

BIBLIOGRAPHY

- "Color Video Thermal Maps," *NASA Tech Briefs*, MFS-29233, March 1979.
- Gaski, J. *SINDA User's Manual*. 10 February 1986.
- Holman, J. P. *Heat Transfer*. New York, McGraw-Hill, 1981.
- Kallis, J. "Programs Help Spot Hot Spots," *IEEE Spectrum*, March 1987.
- Kays, W. *Convective Heat and Mass Transfer*, 1966.
- Kreith, F. "*Principles of Heat Transfer*," 1965.
- Marks' Standard Handbook for Mechanical Engineers*. New York, McGraw-Hill, 1978.
- White, D. "The Thermal Puzzle," *Mechanical Engineering*, October 1986.

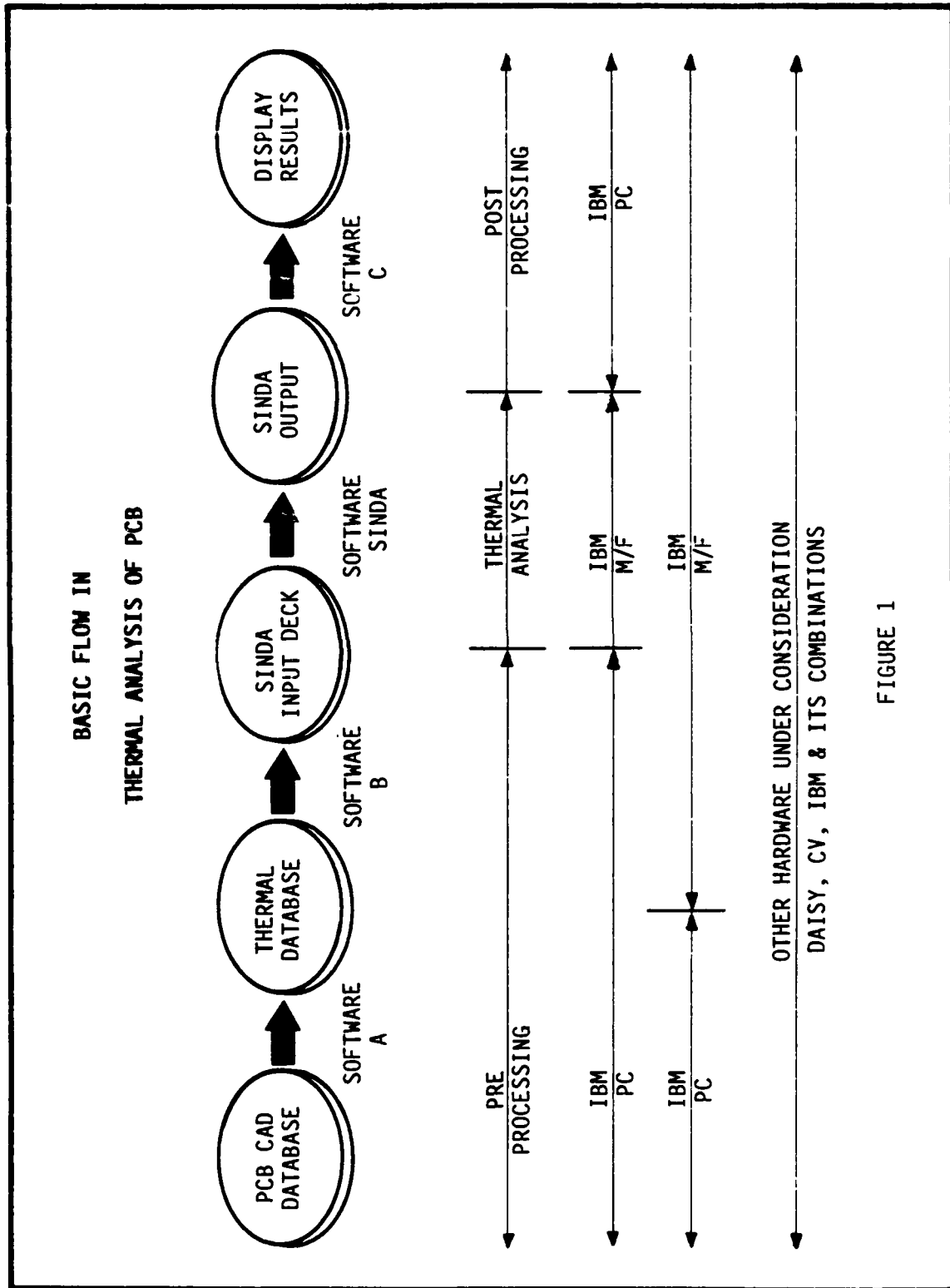


FIGURE 1

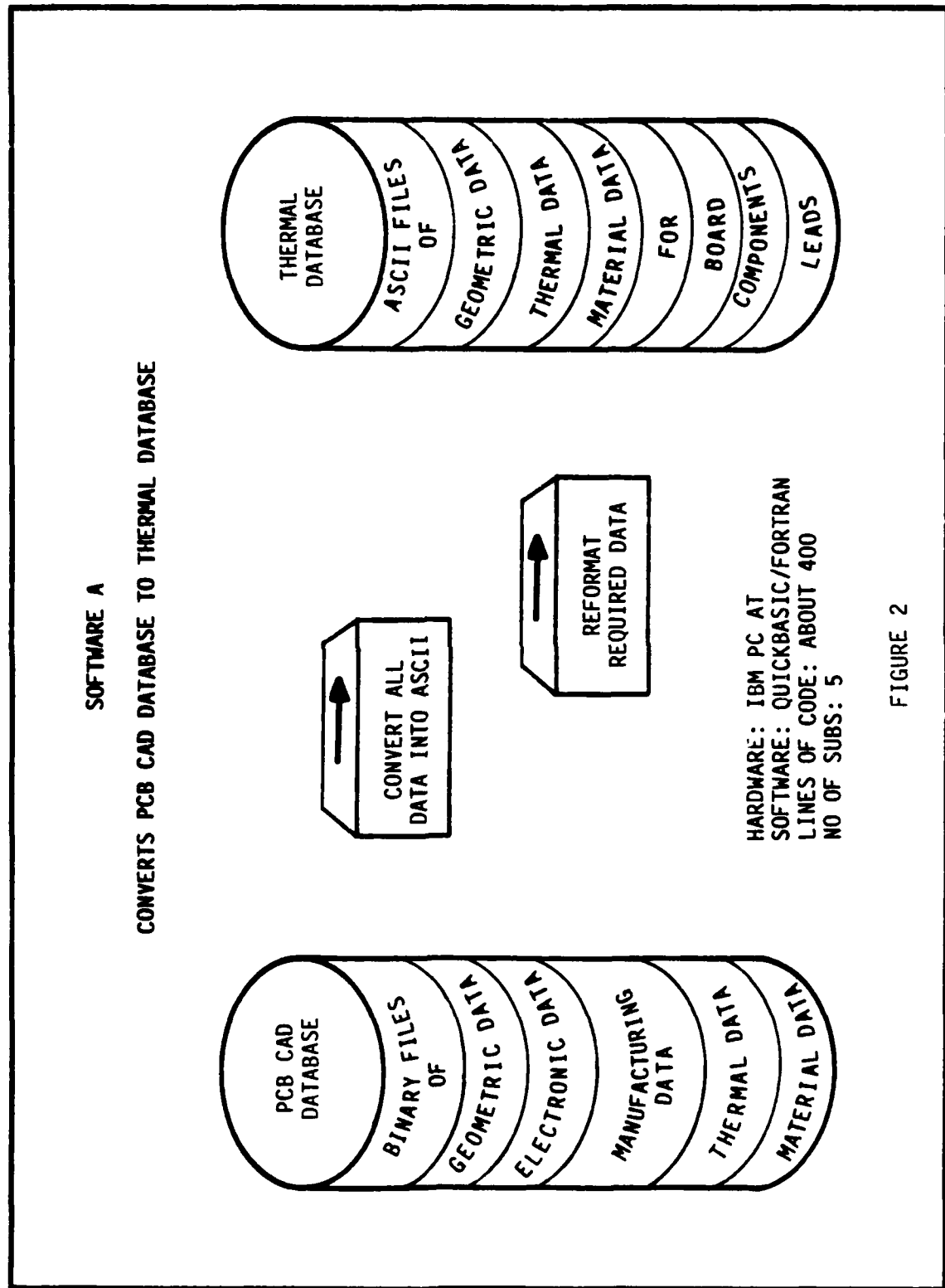


FIGURE 2

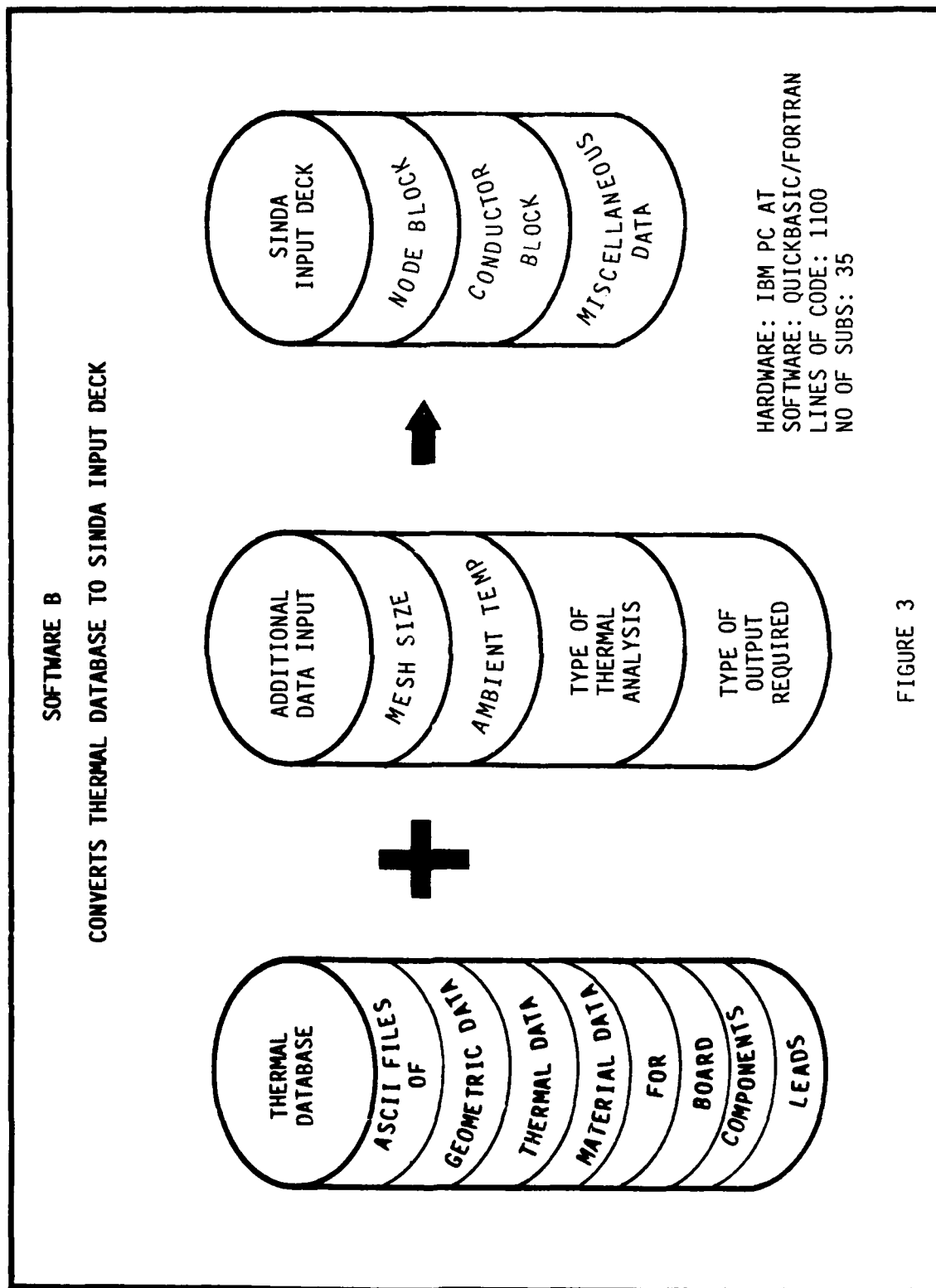


FIGURE 3

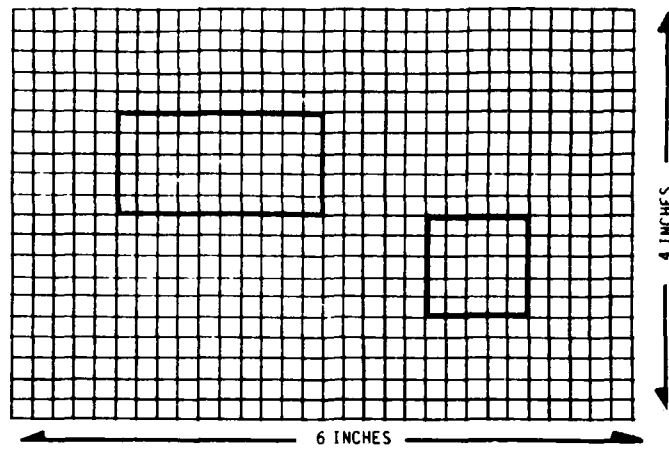


FIGURE 4. SIMPLIFIED PCB

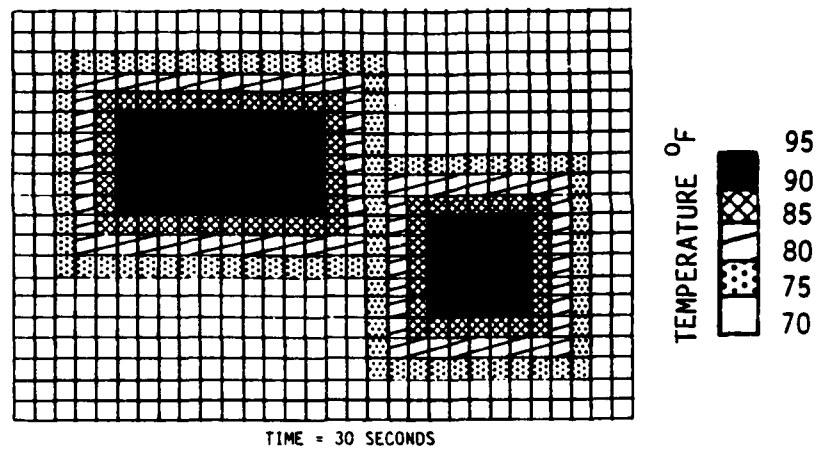


FIGURE 5. THERMAL PROFILE

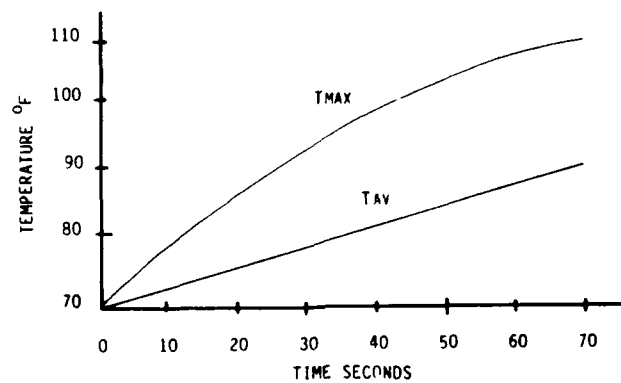


FIGURE 6. TRANSIENT RESPONSE

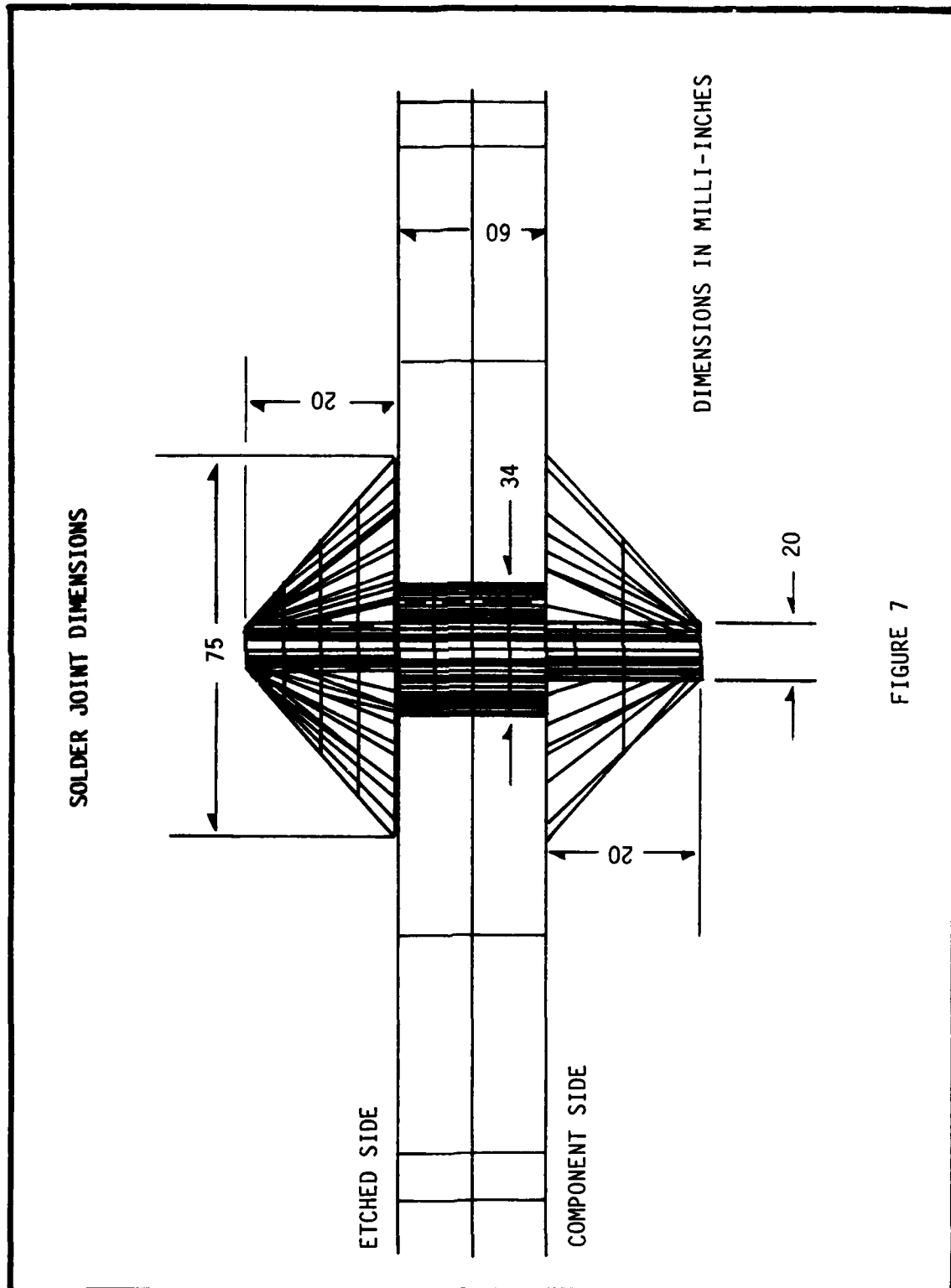


FIGURE 7

SOLDER JOINT NODAL MESH
THREE DIMENSIONAL VIEW

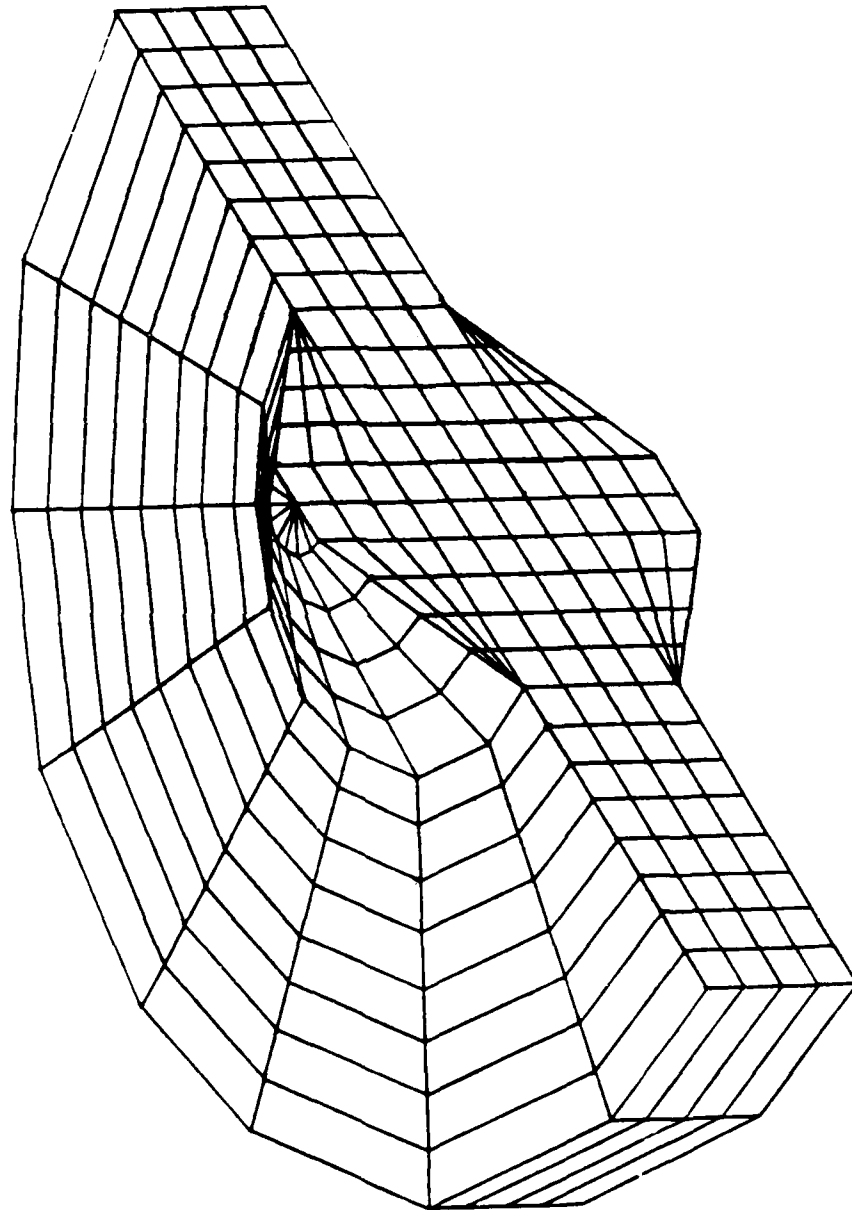
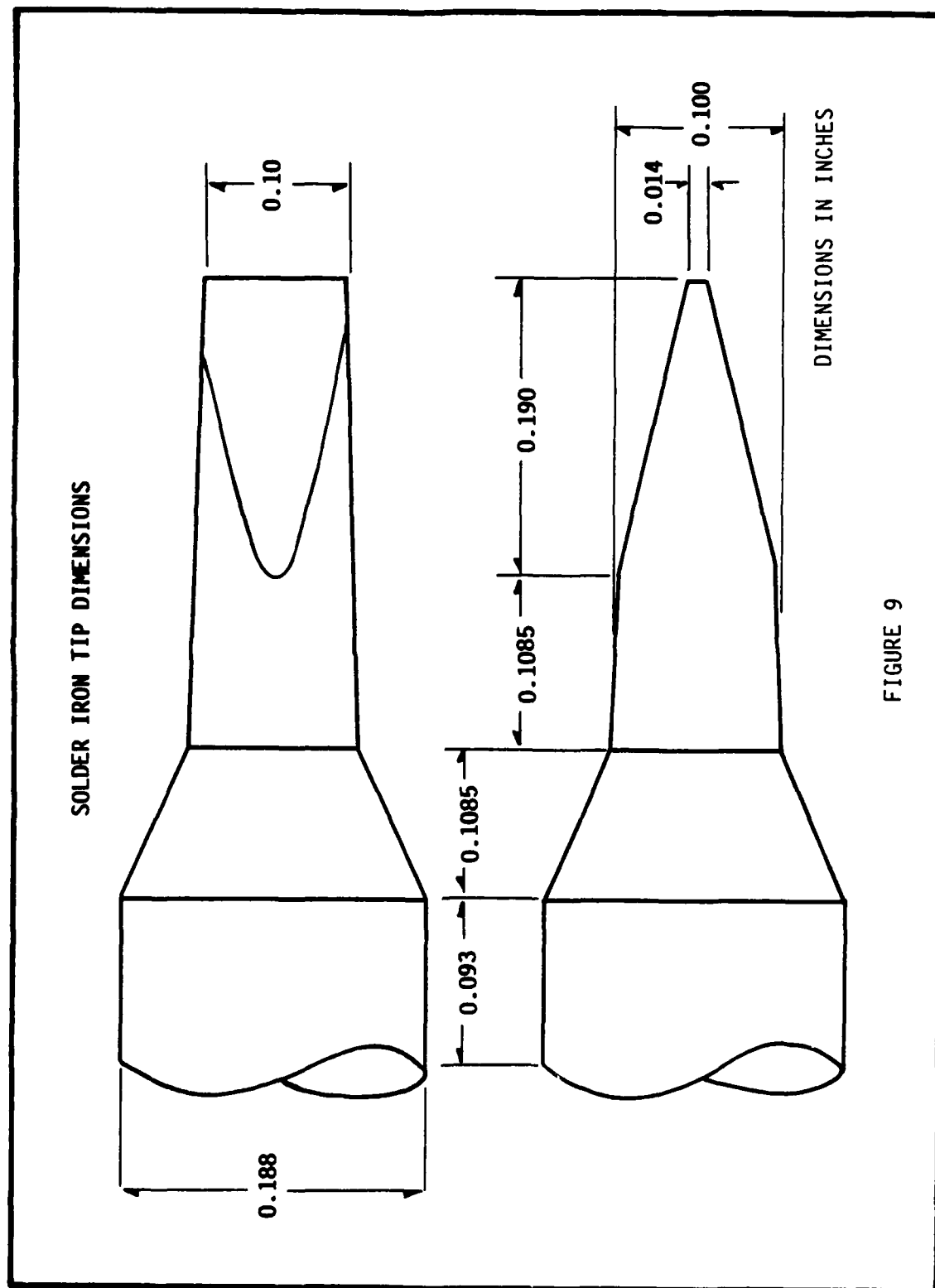


FIGURE 8



SOLDERING IRON TIP NODAL MESH
THREE DIMENSIONAL VIEW

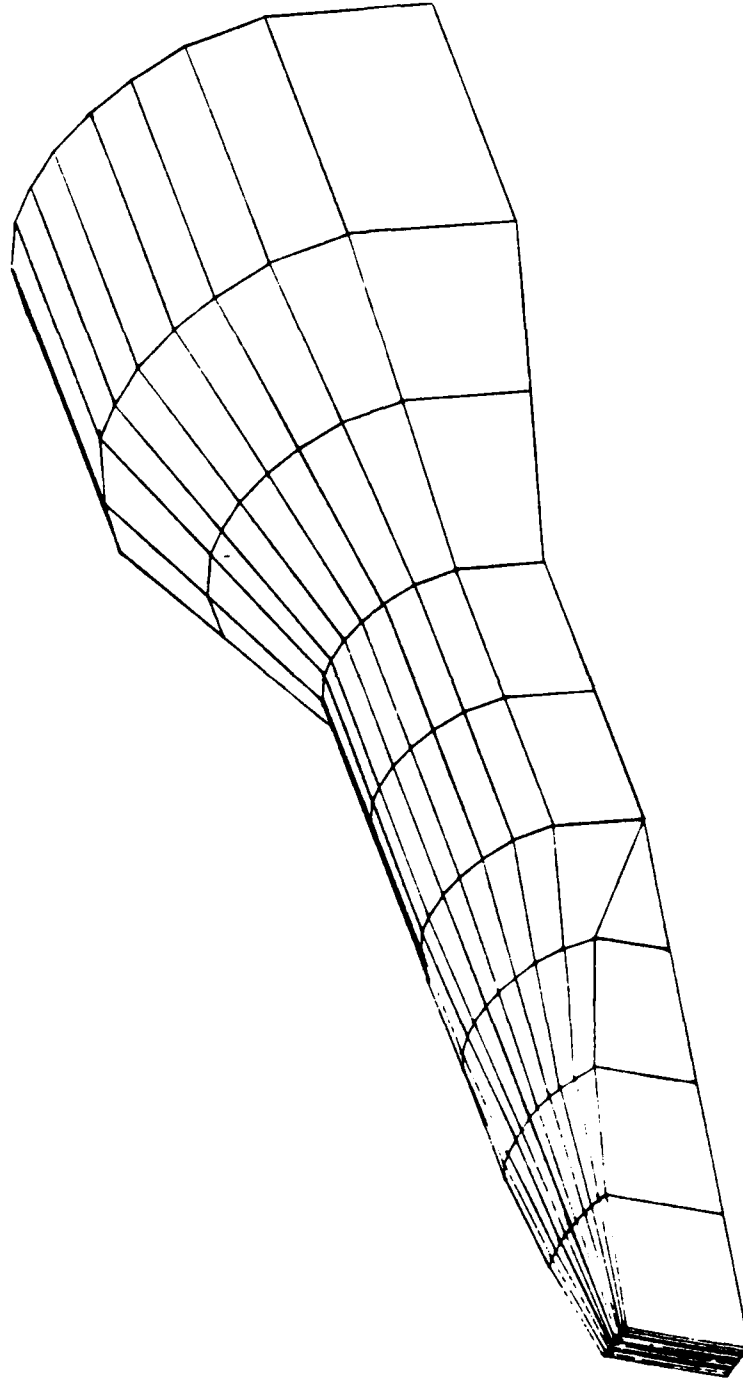


FIGURE 10

SOLDER JOINT MODEL MESH

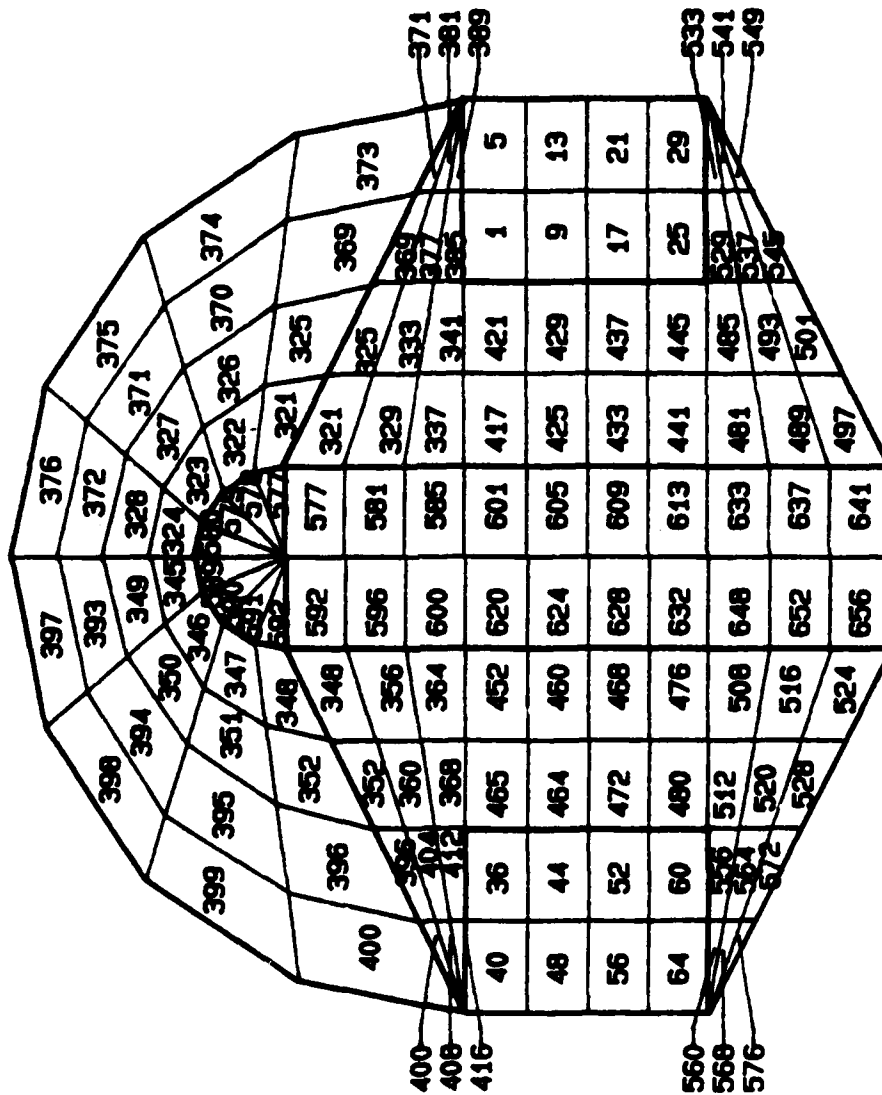


FIGURE 11

SOLDERING IRON TIP
NODAL MESH

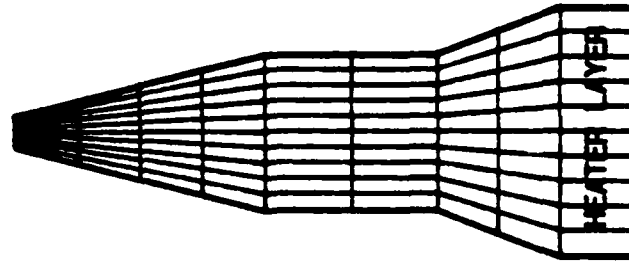


FIGURE 14

SOLDER JOINT NODAL MESH

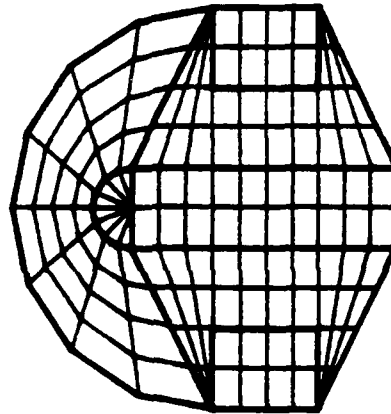
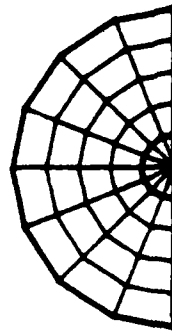
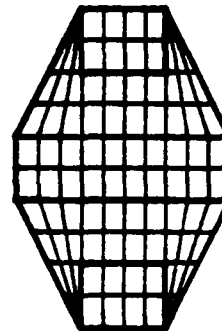


FIGURE 13

SOLDER JOINT NODAL MESH



TOP VIEW



SIDE VIEW

FIGURE 12

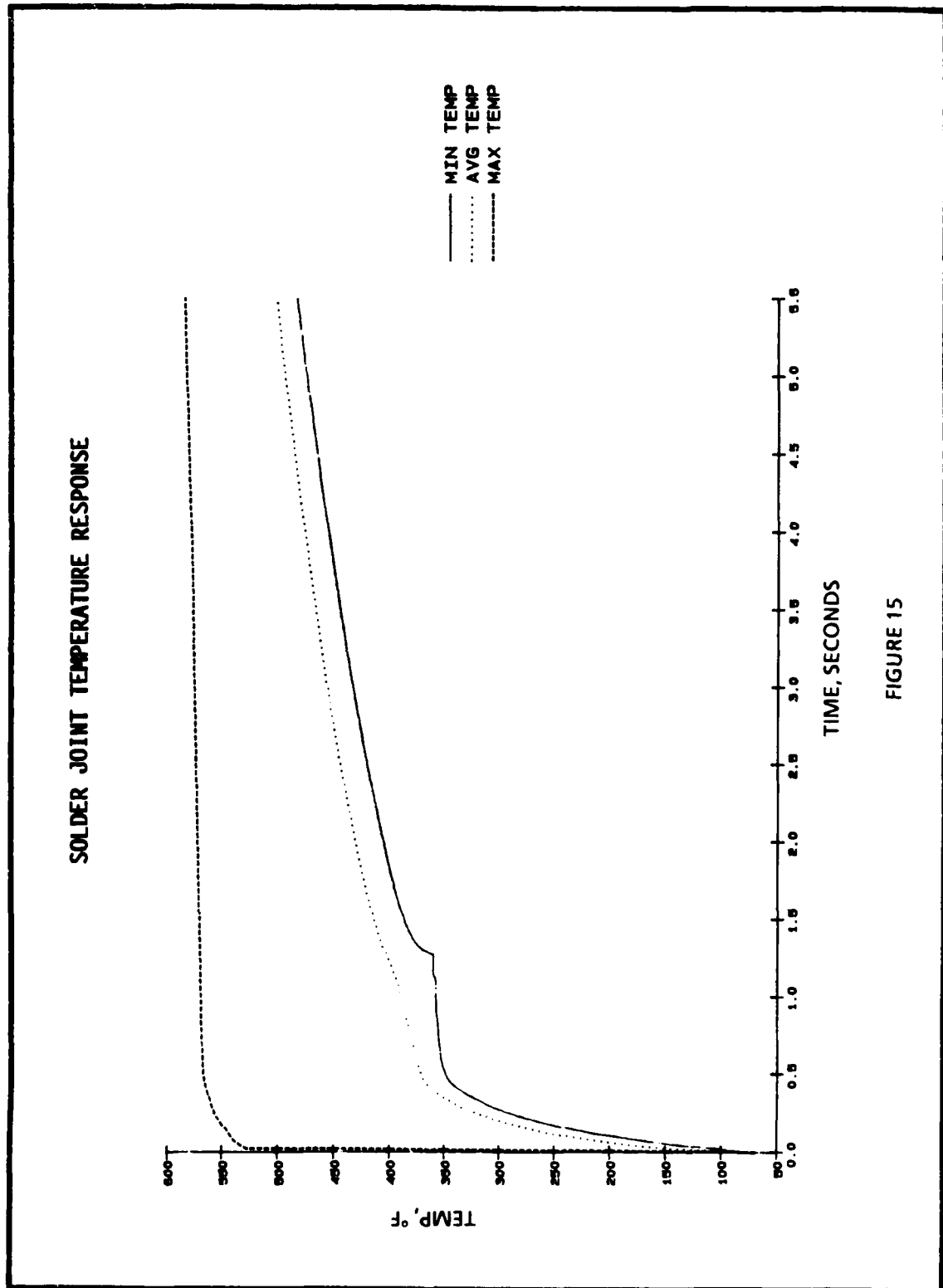


FIGURE 15

NWC TP 6896
EMPF TP 0003

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NWC TP 6896
EMPF TP 0003

John T. Guy, a Mechanical Engineer with the EMPF Detachment, Naval Industrial Resource Support Activity (NAVIRSA), works with finite element analysis and software development. He was educated at the University of Wisconsin, Platteville.

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MANUAL SOLDERING - A SCIENTIFIC APPROACH

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ABSTRACT

In recent years, manual soldering has been considered to be a process principally controlled by the human. Therefore, process controls could not be incorporated easily. Due to technology advancements and the inability to replace manually controlled processes, process controls must be implemented in the manual soldering process.

The soldering iron, in simple terms, is a tool that uses the conduction method of heat transfer to raise the temperature of a solder connection to a preselected temperature. At this temperature, solder will flow and form a metallurgical bond with the hardware. Due to the small mass of the soldering iron tip, the operator, soldering iron, and hardware can critically affect the rate of heat transfer. The rate at which the hardware is heated and the temperature it attains has an impact on the reliability of the final solder connection.

Through experimentation, the thermal energy that various soldering tools and processes can provide to discrete hardware configurations are predicted. By using these prediction algorithms, the soldering tools and processes that ensure optimum quality are selected for a particular solder connection using analytical methods. These analytical methods allow us to venture into robotic soldering with process control.

INTRODUCTION

The goal of the manual soldering process is to provide consistent and reliable solder connections through proper material selection, tool design, and operator training. With both multilayer assemblies and surface mount circuitry, the industry faces a variety of assemblies to solder. Due to this large variety, the manual soldering process is in need of an approach for tool and technique selection that will provide the quality and reliability demanded by military electronics.

During the soldering process, the tip will cycle through various temperatures, losing heat during hardware contact and gaining heat when removed. The amount of heat that is lost from the soldering iron tip depends upon the temperature and thermal capacity (calories stored) of both the tip and the solder connection. The ideal process controlling parameter is the assembly temperature during the soldering process. Because of instrumentation and cost limitations, this measurement is not feasible. As an alternative, we can monitor the soldering iron tip temperature during the soldering process and make approximations of the assembly temperature.

There are new technologies that do not depend upon the tip thermal storage but rather power provided to the tip. In this case, power can be monitored in place of tip temperature.

CURRENT METHODOLOGY

The military industry faces a variety of soldering iron tests when trying to meet current specifications. One of these tests is the tip-to-ground and tip potential test. These tests ensure that electrical energy induced from the environment or leaked from the soldering iron heaters does not damage sensitive components. However, voltage and resistance values in current specifications are difficult to measure with any level of accuracy.

The process of measuring tip-to-ground resistance using a conventional multimeter with the soldering iron hot might cause unrepeatable measurements. Some digital multimeters use a constant voltage of less than a volt to make the resistance measurement. With the iron hot and in contact with a probe, the dissimilar metals between the iron tip and the probe produce thermocouple voltages (See Table 1). These voltages are usually in the millivolt range and will affect the resistance measurements by adding or subtracting from the constant voltage supplied by the ohmmeter. From measurements made, we have seen as much as $\frac{1}{2}$ ohm using various probes. If the minimum resistance allowed is 2 ohms, this fraction can be significant!

TABLE 1. Thermoelectric Voltage vs. Material Types

Material	Voltage (mV) *
Copper	1.242 \pm 0.016
Brass	0.820 \pm 0.006
Beryllium-Copper (Clip Lead)	1.050 \pm 0.006

* Voltage at approximately 620° F

There is a recommended solution to this problem. Since the thermocouple voltage is polarized, true voltage or resistance is obtained by taking a measurement, reversing the leads to the multimeter, and making the measurement again (See Figure 1). The average of these 2 values will eliminate the thermoelectric effects and will provide an accurate measurement (See Appendix 1). From our testing, we have found that brass provides the smallest thermocouple voltage; therefore, it is the preferred probe material.

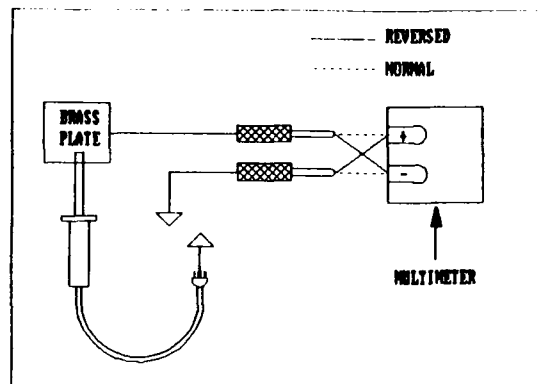


FIGURE 1. Probe Configuration for the Tip Potential and Resistance Test.

The tip potential measurement is controversial due to insufficient knowledge regarding what energy level will cause failure or latent defects in sensitive components. At present, measurements are being made with a RMS AC Voltmeter. If a broad-band meter is being used, these measurements can be extremely sensitive to environmental electromagnetic radiation. Values as high as 0.3 millivolts were measured with no power applied to the iron. This phenomenon occurs because the soldering iron acts as an antenna in the presence of electromagnetic radiation.

Measuring tip temperature of the soldering iron while at idle is another military requirement. This measurement determines the iron's ability to maintain a constant temperature in the absence of a thermal load. A variety of methods are used to measure tip temperature. They include noncontact (infrared and chemical) thermometers, contact pyrometers, and embedded thermocouples. Each of the measurement systems has various limitations and repeatability characteristics which are covered in the following text.

Infrared thermometry normally requires the tip to be prepared with some type of a constant emissivity coating and a small beam diameter on the infrared equipment. The latest method includes firing a glass band on the tip above the wetted area. The glass coating can maintain an emissivity of approximately 0.90 from ambient to soldering temperatures.

Contact pyrometers are systems that use a thermocouple junction to measure the surface temperature of the soldering iron tip. These systems will typically load the tip and cause it to read a temperature lower than when it was at idle. The key to implementing a contact pyrometer as a process control device is to ensure that it provides a consistent thermal load from one measurement to another. In previous testing, we have found placement and pressure between the soldering iron and the contact pyrometer to significantly affect the temperature measurement.

Embedded thermocouples have in the past been deemed the industry standard for tip temperature measurement. Thermocouples may be attached to the tip in a number of ways. One approach is to weld the thermocouple junction to the surface of the tip. Another method is to place the thermocouple junction in a hole drilled in the tip and secure the assembly with silver solder. Finally, the junction is supported in a hole by a copper spike, or by some other means. The embedded thermocouple will also act as a thermal load to the tip; however, since it is being held in a stable position, it will provide a consistent load.

The methods used to embed a thermocouple are extremely critical to the measurements accuracy and repeatability. The thermocouple must be exposed to as little stress as possible when being attached, as excessive bending will fatigue the thermocouple and cause erroneous temperature measurements.

The tip temperature measurement process should include a calibration procedure. Most of the systems previously mentioned use a thermocouple junction as the tip temperature sensing mechanism. With excessive use and mechanical fatiguing, it is possible for the thermocouple junctions to degrade. The degradation of the junction is detected by using standard temperature baths when calibrating the thermocouple junctions.

MEASURING OPERATOR INTERACTION

The operator is the key controlling element in the manual soldering process. Process controlling parameters such as tip contact area, pressure, and dwell time are all controlled by the operator. The operator's ability to control significant process parameters and the iron's ability to provide sufficient thermal power determines product consistency.

The soldering iron's principal function is to provide thermal energy to the hardware. Both amount and rate of thermal energy being transferred to the hardware is controlled by the operator and the soldering iron. Through experimentation, we have developed testing techniques that measure how operator inconsistencies affect the thermal energy transfer of the soldering iron.

This technique was derived from measuring the working tip temperature of a soldering iron while soldering a standard production printed circuit board. In addition to providing operator interaction information, this test directly reveals the iron's temperature drop during the soldering process. Operator interaction information is provided by correlating the average tip temperature of the soldering iron to the time the operator spends performing various activities. These activities include soldering the connection, cleaning the tip of the soldering iron, and transporting the iron between the connection and the tip cleaning device. Results provided from this test show how operator variations affect tip temperature variations during the soldering process.

The first attempt at running this test involved a set of standard printed circuit assemblies, a video system, and an automatic data acquisition system (See Figure 2). The circuit assemblies were soldered by 3 different operators using 2 different soldering stations. The standard printed circuit assemblies provided a constant thermal load to the soldering iron. The video system was used to extract operator time and motion data while the data acquisition system was used to collect tip temperature data. The differences in the soldering irons can be seen in Table 2.

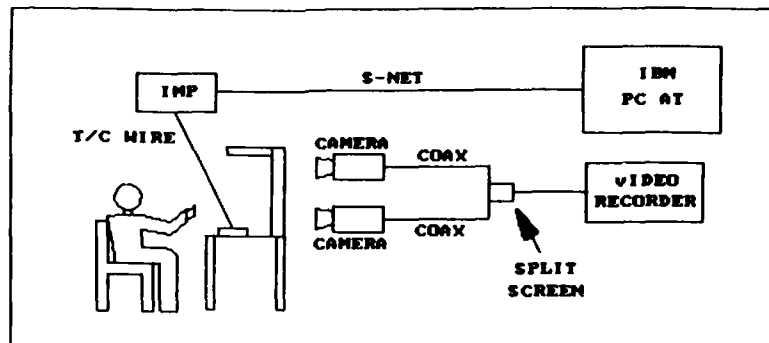


FIGURE 2. Instrumentation for Operator Interaction Test.

Table 2. Results of the Correlation Analysis.

Activity	R^2 (Iron #1) *	R^2 (Iron #2)
Soldering	0.04	0.16
Cleaning	0.03	0.01
Transport	0.20	0.49

* $R^2 \times 100$ is the percentage of variance in the tip temperature that can be explained by the variance in the activity. The formula used to derive this value is as follows:

$$R = \frac{n\sum x_i y_i - (\sum x_i)(\sum y_i)}{\sqrt{[n\sum x_i^2 - (\sum x_i)^2][n\sum y_i^2 - (\sum y_i)^2]}}$$

where x_i = the mean time for the activity on assembly i .

y_i = the mean tip temperature while soldering assembly i .

The operator and iron combination with the smallest interaction coefficient (R^2) will provide the most stable temperature during the soldering process. Since both of the tests performed used the same operators and circuit assemblies, soldering iron #1 is affected less by operator inconsistencies. In fact, results seem to suggest that the soldering iron compensated for the operators' variability.

Future testing will incorporate computer control to eliminate the video equipment and obtain results by soldering fewer connections. Fewer connections will be needed because the analysis will correlate the time and tip temperature at the connection level instead of the assembly level.

EMPIRICALLY MODELING THE SOLDERING IRON

Experimentally modeling the soldering iron without the presence of the operator is another approach in determining a soldering iron's ability to solder a particular circuit assembly. Either a spring tension pivot arm or a robot is used as a controlling mechanism (See Figure 3). In addition, it is important to perform the experiment within the realistic realm of the manual soldering process. For example, the pressure applied to the tip should be within the region of that supplied by an operator.

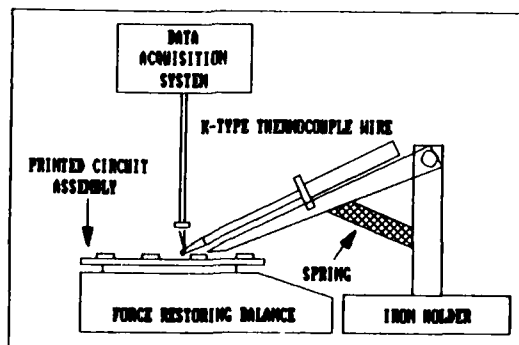


FIGURE 3. Spring Tension Arm used for Developing Empirical Models.

The parameters selected for the first model are pressure, contact angle, temperature, and thermal load. The method used to generate the model is a two-level full factorial analysis. If more accuracy is needed in the empirical model, we will re-run the experiment using a response surface design. The output of this analysis provides us with 2 equations that will predict the temperature of the tip and a designed thermal load at a particular time. If the heat capacity** of a designed thermal load is known, then we can calculate the heat capacity of the soldering iron tip. This will provide us with the amount and rate which thermal energy can be provided to the hardware from a particular soldering iron and tip combination. The thermal energy of the soldering iron is also affected by the rate in which connections are made. In the future, the soldering rate will be added to the model using robotics.

By incorporating minimum and maximum realistic values for each process parameter into the empirical model, we can calculate minimum and maximum heat capacity coefficients. In addition, if the heat capacity and thermal conductivity of the assembly is estimated, then we can approximate the average temperature of the assembly during the soldering process. (The stability of the soldering materials' thermal properties will affect the accuracy of this approximation.)

*A thermal load is a body that will absorb thermal energy and will raise its temperature proportional to the energy absorbed. When brought into physical contact with another body (such as a soldering iron tip) of a different temperature, thermal energy will flow between the two bodies until they reach thermal equilibrium. For our testing, we used a specially designed thermal load and a completed solder connection. The thermal load is made of a precisely measured stainless steel substraits and a solder bead.**

Heat Capacity is the quantity of heat required to raise the temperature of the load by one degree of temperature, given in Joules per degree C.)

ROBOTIC SOLDERING

Robotic point-to-point conduction soldering uses the same tool as manual soldering, except a machine replaces the human. In the manually controlled soldering process, humans will typically compensate for material inconsistencies such as solderability. When these inconsistencies occur, the human will make decisions and will adjust various parameters in order to achieve a given quality level. For example, if the solderability of the printed circuit board affects the solder flow through the board, the operator might increase the dwell time slightly to compensate for this.

The robotic soldering process does not have this capability. All of the soldering conditions on the robot are programmed before the soldering process begins. If the robot is to achieve the same decision making capability as the human, it will need to monitor process controlling parameter(s), decide which parameter to change, and adjust the appropriate process parameter during soldering. For our testing, the process control parameter that will be monitored will be tip temperature. The decision making tool will be an empirically developed algorithm. This algorithm will predict changes in tip temperature, defect calls, and laser inspected thermal profiles due to changes in process parameters.

An initial screening experiment has been conducted to determine which process parameters affected tip temperature, number of defects visually inspected, and thermal profile of a laser inspected solder connection. After significant process parameters are determined, the empirical model will be developed.

CONCLUSION

Testing dictated by military specifications regarding soldering irons does not address methods for ensuring sufficient thermal energy needed to manufacture a quality connection. The testing that is being performed basically addresses electrical and steady-state thermal measurements. These measurements do not ensure quality hardware from the manual soldering process and are extremely dependent upon testing methodology. Phenomena such as thermoelectric effects change the values measured solely due to the probe material used.

Developing process controls in the manual soldering process is essential. The cost of the manufacturing equipment should not dictate the efforts spent controlling the process around it. Even though most soldering irons cost well under 500 dollars, the circuit assemblies can achieve costs as high as $\frac{1}{2}$ million dollars. The systems that these assemblies are placed in can cost up to 2 million dollars. These systems are then placed on aircraft that can cost well beyond 20 million dollars. Processes that are not controlled can cost the military millions of dollars and possibly the loss of life.

The manual soldering process is one of the weakest links in electronics manufacturing due to the human controlling element. This process can, however, provide higher product consistency and quality if more analytical testing and controlling methods are implemented.

APPENDIX 1

The formulas used to calculate the true resistance and D.C. voltage values are as follows:

If both values are positive:

$$\text{True Value} = \frac{\text{H.V.} + \text{L.V.}}{2}$$

If one value is positive and one is negative:

$$\text{True Value} = (\text{H.V.}) - \frac{|\text{H.V.}| + |\text{L.V.}|}{2}$$

Where H.V. = the highest value; measurement taken with the leads in the normal configuration.

L.V. = the lowest value; measurement taken with the leads in the reverse configuration.

True Value = Resistance and Voltage value minus thermoelectric electromotive force.

BIBLIOGRAPHY

Spencer, Richard, E., "Hand-to-Hand Combat, Selecting a Soldering Station", Circuits Manufacturing, May 1986, pp. 65-69.

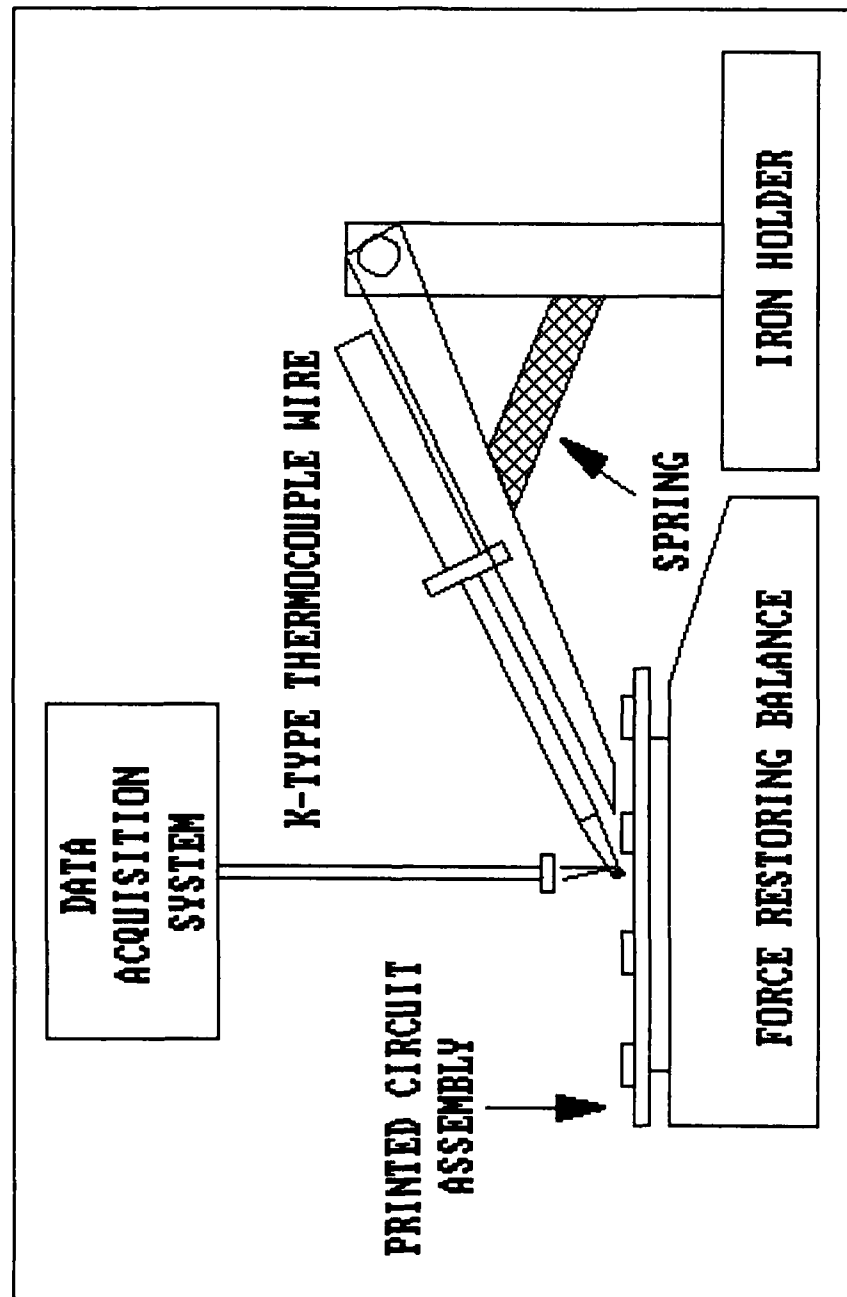
Cowell, Mark, "New Thermal Strategy For Hand Soldering", 11th Annual Electronics Manufacturing Seminar Proceedings, 18-19 February 1987, pp. 117-131.

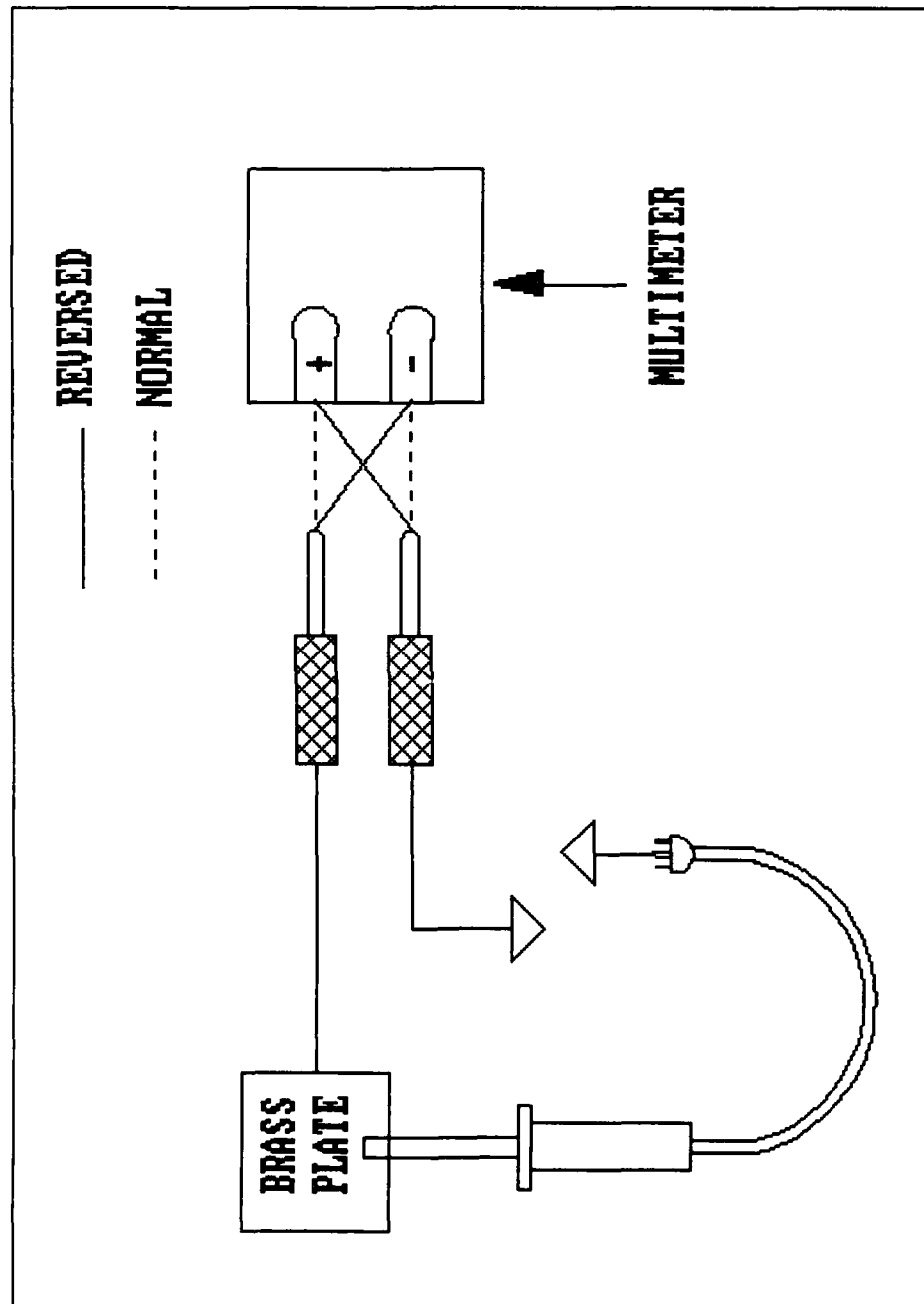
Johnson, Richard, O., "Non-Destructive Hand Soldering Of Military Electronics", 11th Annual Electronics Manufacturing Seminar Proceedings, 18-19 February 1987, pp. 133-161.

Crockett, Lionel, "Seven Iron-Plated Rules For A Good (Soldered) Joint", Electronics Weekly, 11 October 1978, pp. 16,18.

George E.P. Box and Norman R. Draper, Empirical Model-Building And Response Surfaces, New York, John Wiley & Sons, Inc., 1987.

George E.P. Box, William G. Hunter, and J. Stuart Hunter, Statistics For Experimenters-An Introduction to Design, Data Analysis, and Model Building, New York, John Wiley & Sons, Inc., 1978.





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CHARACTERIZATION OF SOLDER FATIGUE
IN ELECTRONIC PACKAGING

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ABSTRACT

As electronic packaging becomes more diverse, the mechanical interplay of various metals, ceramics, and plastics becomes an important issue. With incorrect design, thermal fatigue can cause serious reliability problems. This paper addresses the characterization and study of solder fatigue in metal/ceramic/FR-4 assemblies. In most cases, problems in the field can be traced to an improper combination of materials and can be avoided by proper design.

In this work, theoretical and mechanical models were designed and constructed for mixed material assemblies. For each of these test assemblies, the different materials were joined by designs involving various degrees of compliancy. Also, a wide variety of solders were tested, including not only the "normal" tin/lead solders, but also several other alloys encompassing a wide range of soft and hard solders. Temperature cycling studies were performed to evaluate each of these assembly and solder possibilities. Scanning electron microscopy/energy dispersive X-ray (SEM/EDX) studies allowed an understanding of the mechanism of fatigue and failure in each case. Mathematical models were developed for each of these cases, resulting in an overall predictive test for solder fatigue. This predictive test directs the design towards the correct degree of compliancy in the solder joint or elsewhere in the overall assembly to avoid fatigue and eventual failure.

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INTRODUCTION

A primary charter in modern technology and manufacture processing is the development of interrelating concepts among the chemistry, structure, mechanical and physical properties, performance, and processing of various materials (Reference 1). Nowhere is this challenge better underscored than in the area of solders, which are used in virtually all electronic devices -- either consumer, industrial, or military. Hence, nowhere are defects in one material more far-reaching in their consequences.

Defects due to faulty solder materials, design, and processing are indeed high (Reference 2), and accordingly it is not surprising that a large number of studies have been carried out. The nature of these studies has been twofold: mechanical/chemical (Reference 3) and theoretical (Reference 4). The challenge in these studies is to develop models that are simultaneously complex enough to take into account all of the variables important to a fatiguing process, and yet general enough to be applicable and easy to use in a wide variety of cases.

In this account we will develop a mechanical/mathematical model, test it in the laboratory, and move on to SEM/EDX characterization of the fatiguing process under study.

THE THEORETICAL MODEL

For the theoretical model, we view an electronic assembly as a series of interplaying materials which follow the usual principles of stress and strain in solid mechanics (Reference 5). Figure 1 shows the simplest case where two springs in series represent the solder joint and the remaining assembly. Each spring possesses its characteristic force constant k (with a smaller k designating greater compliancy), which interact with one another according to equation 1. If one of the force constants is much larger than the other, then it (the larger force constant) will be negligible in the final expression.

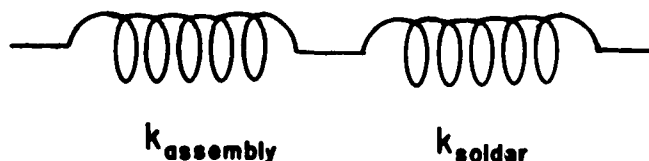


FIGURE 1. Simple theoretical model of solder joint and assembly: a series of springs obeying Hooke's law.

$$k_T = (k_{\text{assembly}}^{-1} + k_{\text{solder}}^{-1})^{-1} \quad (1)$$

where k_T = total force constant (of entire assembly)

k_{assembly} = force constant of assembly other than solder joint

k_{solder} = force constant of solder joint

SPECIFIC CASE: MINIMUM COMPLIANCY

We next transform Figure 1 into a specific case for analysis, where minimum compliancy exists (see Figures 2-3). For the assembly, thermal mismatch arises from two different materials (Figure 2), leading to a

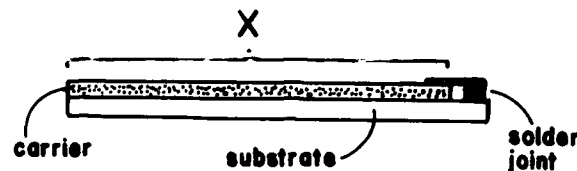


FIGURE 2. Theoretical model of assembly showing source of thermal mismatch. In this model, we assume the left terminus is rigidly anchored, so that the linear deformation difference is observed at the right terminus (the location of the solder joint).

difference in linear deformation (equation 2). In this model we assume the left termini are rigidly anchored to one another, so that the free deformation difference is observed at the right terminus (the location of the solder joint). At the right terminus (Figure 3) we have a copper bar (or lead) whose ends are mounted rigidly to the substrate (left end) and soldered to the substrate (right end).

$$\delta = (TCE_{\text{substrate}} - TCE_{\text{lead}}) (X) (T) \quad (2)$$

where δ = linear deformation difference

$TCE_{\text{substrate}}$, TCE_{lead} = thermal coefficient of expansion of substrate, lead

X = total length of assembly

T = temperature excursion

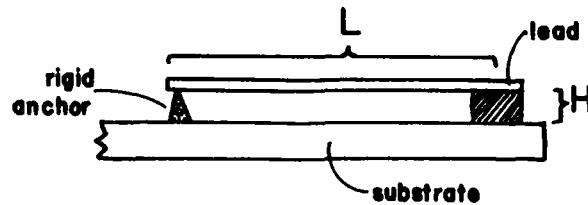


FIGURE 3. Theoretical model showing detail of right terminus of Figure 2 (i.e., the solder joint).

We now evaluate the force constants k of Figure 3. For the copper lead, we have axial deformation and Hooke's law gives:

$$k_{\text{lead}} = \frac{(A_v) (E)}{(L)} \quad (3)$$

where A_v = vertical cross sectional area of copper lead

E = modulus of elasticity of lead

L = length of lead

For the solder joint, we have shearing deformation, and Hooke's law gives:

$$k_{\text{solder}} = \frac{(A_h) (G)}{(H)} \quad (4)$$

where A_h = horizontal cross sectional area of solder lead

G = modulus of rigidity = $E/[2(1 + \nu)]$
(ν = Poisson's ratio)

H = height of solder joint

Let us now substitute some specific values. Assume the copper lead is 10 x 80 mils in area (0.01 x 0.08 inch) and 0.25 inch in length; and the solder joint is 60 mils high (0.06 inch) and 50 x 80 mils in area (0.05 x 0.08 inch). Substitution into equations 3 and 4, and then equation 1, gives:

$$\begin{aligned} k_{\text{lead}} &= A_v E/L = (0.08)(0.01)(17 \times 10^6)/0.25 \\ &= 54,000 \text{ pounds/inch} \end{aligned} \quad (5)$$

$$\begin{aligned} k_{\text{solder}} &= A_h G/H = \frac{(0.08)(0.05)(2 \times 10^6)}{(0.06)[2(1 + 0.3)]} \\ &= 51,000 \text{ pounds/inch} \end{aligned} \quad (6)$$

$$\begin{aligned} k_T &= (54,000^{-1} + 51,000^{-1})^{-1} \\ &= 26,000 \text{ pounds/inch} \end{aligned} \quad (7)$$

Let us now calculate the shear stress experienced by the solder joint. Assuming a temperature excursion of 130° C (for the justification of this choice, see below), and for a 2-inch assembly, from equation 2 comes:

$$\begin{aligned} \delta &= (\text{TCE}_{\text{substrate}} - \text{TCE}_{\text{lead}}) (X) (T) \\ &= (17 - 6) 10^{-6} (2) (130) \\ &= 0.0029 \text{ inch} \end{aligned} \quad (8)$$

Directly from Hooke's law,

$$\begin{aligned} F &= k_T \delta = (26,000) (0.0029) \\ &= 75 \text{ pounds} \end{aligned} \quad (9)$$

The shear stress experienced by the solder joint will be:

$$\begin{aligned} \tau &= F/A_h = \frac{(75)}{(0.05)(0.08)} \\ &= 19,000 \text{ pounds/square inch} \end{aligned} \quad (10)$$

Note that the value obtained for τ by assuming the lead is completely rigid is similar (because k_{solder} is not much larger than k_{lead}):

$$\begin{aligned} \delta/L &= F/(A_v E) \\ (0.0029)/(0.25) &= \frac{(F)}{(0.08)(0.01)(17 \times 10^6)} \\ F &= 160 \text{ pounds} \end{aligned} \quad (11)$$

Or, calculated from equation 9,

$$F = k_{\text{lead}} \delta = (54,000) (0.0029) \quad (12)$$

$$= 160 \text{ pounds}$$

The shear force experienced by the solder joint is comparable to that obtained in equation 10:

$$\tau = F/A_h = \frac{(160)}{(0.05)(0.08)} \quad (13)$$

$$= 40,000 \text{ pounds/square inch}$$

Will the solder joint fail? Various studies (Reference 6) suggest that the value of τ (shear stress) at which failure will occur is about 500 pounds/square inch. Hence, in this example, we would predict rapid failure.

SPECIFIC CASE: COMPLIANCY IN LEAD

Let us now evaluate the effect of rendering the copper lead compliant. For this model, we will assume a design where the same lead is bent at a 90° angle (Figure 4). Assuming the major contribution

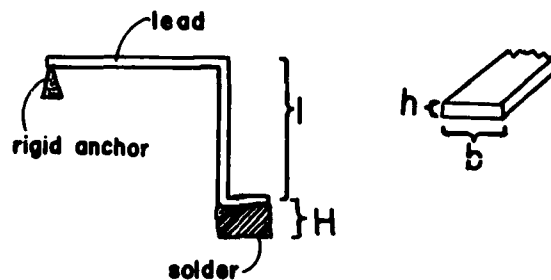


FIGURE 4. Theoretical model of Figure 3 continued, where the copper lead is bent at a 90° angle.

of the lead is compliancy originating from the bending moment*, we

*Other contributions in the analysis of Figure 4 include (1) the flexing of the horizontal portion of the lead and (2) the tensile contribution of the copper lead. The tensile contribution was calculated above and would be negligible in this case. The vertical flexing contribution y would be $Mr^2/2EI$, where the moment M is the length of the vertical beam r times the force F . The horizontal contribution δ is (by similar triangles) $(1/r)(y)$. The δ contribution is thus $l^2Fr/2Eb^3$, and thus is calculated

calculate the force from equation 14:

$$\delta = \frac{(F) (l)^3}{3 (E) (I)} \quad (14)$$

where l = vertical length of lead

I = moment of inertia = $bh^3/12$

b = horizontal dimension of copper lead

h = vertical dimension of copper lead

$$\delta = \frac{4 (F) (l)^3}{(E) (b) (h)^3} \quad (15)$$

$$0.0029 = \frac{4 (F) (0.125)^3}{(17 \times 10^6) (0.08) (0.01)^3}$$

$$F = 0.50 \text{ pound}$$

The shear stress experienced by the solder joint will be:

$$\begin{aligned} \tau &= F/A_h = \frac{(0.50)}{(0.05)(0.08)} \\ &= 125 \text{ pounds/square inch} \end{aligned} \quad (16)$$

The value of τ is now below 500 pounds/square inch and we would predict no failure. Hence, by merely bending the lead, we improve the compliancy of the system sufficiently to change the solder joint from a failure to a safe situation.

to be about one-eighth of the contribution to δ from equation 14. Hence, for simplicity we ignore this contribution, simply recognizing that the compliancy of the lead is actually 10% or so greater than calculated from equation 15.

TEST CASES

Inspection of equations 3, 4, and 15 suggest several ways to approach the problem of solder joint failure:

1. Increase the lead compliancy by designing bends or loops (should be very effective).
2. Increase the lead compliancy by reducing the cross sectional area of the lead (should be effective).
3. Increase the lead compliancy by reducing the elastic modulus (not much opportunity for improvement).
4. Increase the lead compliancy by increasing its length (generally not practical).
5. Decrease the solder joint shear stress by increasing the solder joint area (should be effective if space permits).
6. Decrease the solder joint shear stress by decreasing the solder joint height (not generally controllable).

To test those ideas which were practical, test samples were prepared as similar as possible to the theoretical model of Figure 2. In these test samples, two-inch ceramic carriers were placed on FR-4 substrates, and a copper lead was soldered on each side of the carrier, with two solder joints per lead (see Figure 5). The test sample was thus mathematically equivalent to the theoretical model, except that: for each solder joint the linear deformation is one-half that calculated in equation 2, and four solder joints are involved, rather than one. The test samples were thermally cycled, -30 to $+100^{\circ}\text{C}$, 10 cycles/day, for 500 total cycles and constantly monitored for fatigue, according to previous procedures (Reference 7). The results are given in Table 1.

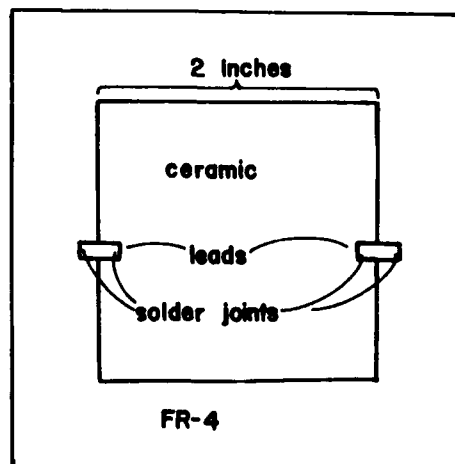


FIGURE 5. Test assemblies used for Table 1.

TABLE 1. Pass/fail Results of Test Assemblies (taken from Figure 5).

Item No.	Test assembly	Predicted result	Observed result
1	10 x 80 mil copper leads, straight	Fail	Fail
2	10 x 80 mil copper leads, bent 90°	Pass	Pass
3	8 x 16 mil silver leads, straight	Pass	Pass
4	10 x 80 mil copper leads, straight, 0.5 x 0.5 inch solder pads	Pass	Pass
5	10 x 80 mil copper leads, bent 90°, butt end	Fail	Fail

Items 1 and 2 of Table 1 represent the situations detailed in Figures 3 and 4. The respective predictions of "fail" and "pass" are observed. Item 3 illustrates the ploy of designing a more compliant lead by reducing the cross sectional area (and to a lesser extent, the elastic modulus). Item 4 shows that increasing the solder joint area indeed decreases the shear stress on the solder joint, suggesting a possible solution to a failing soldered assembly could be extra solder buttresses. Item 5 shows that even with a bent lead, with a butt end for soldering the effective solder area is reduced such that failure is now experienced.

SOLDER FATIGUE CHARACTERIZATION

To prepare samples for characterization, assemblies were prepared as shown in Figure 6. The shear stress far exceeds 500 pounds/square inch as the samples are thermally cycled from -30 to +100° C, 10 cycles/day (Reference 7), and fatigue rapidly sets in. Figures 7-14 describe this phenomenon for 60/40 tin/lead solder. As fatigue advances, the original fillet (Figure 7) begins to craze (Figure 8), then pits and cracks (Figure 9) and then completely fails (Figure 10). A superficial examination suggests the failure is at the pin (see cross section in Figure 11), but closer examination (Figure 12) establishes the failure is through the solder. The mechanism for this failure is domain enlargement, as previously observed (Reference 3c). An intermediate stage of fatigue, corresponding to Figure 8, is shown in Figure 13. An enlargement of the surface crazing is shown in Figure 14.

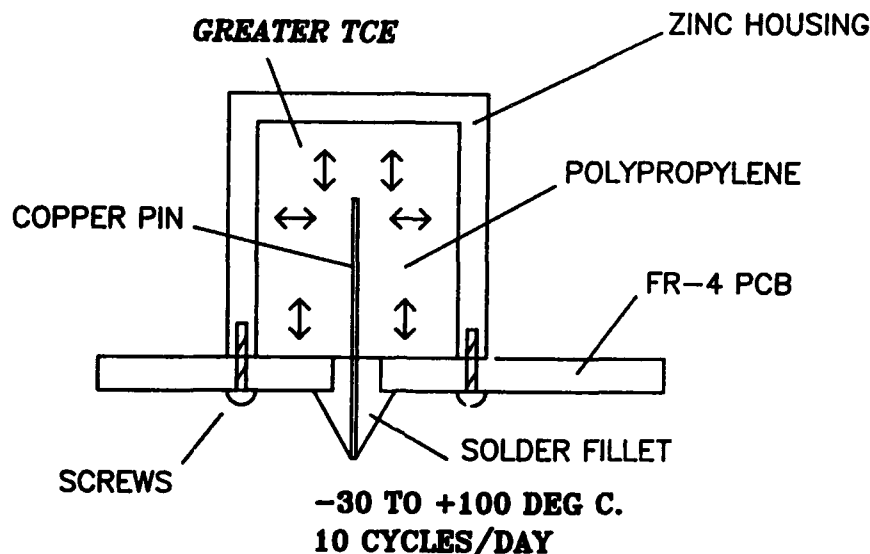


FIGURE 6. Assemblies to prepare samples for solder characterization. Thermal cycling of this assembly produces excess stress on the solder fillet and causes rapid fatigue.

Other solders were also studied, using these test assemblies. Figure 15 shows a stress-cycle plot for all solders, and demonstrates the soft solders perform worse than tin/lead, and the hard solders better. Surface crazing appears differently for these solders: Figures 16-17 display surfaces of 95/5 tin/silver and 50/50 indium/lead. Cross sections generally show no change in domain enlargement for solders other than tin/lead (see Figures 18-19), although for 62/36/2 tin/lead/silver, in addition to the usual domain enlargement observed for tin/lead, the silver-enriched domains also aggregate (Figures 20-21).

The plots of Figure 15 demonstrate that the hard solders originally perform better, and failure of the solder is much more difficult (see Figures 22-23) than with the soft solders (Figure 24). Nevertheless, another failure mechanism arises with the hard solders, as evidenced by the change in the slopes of Figure 15. This mechanism involves the failure of the intermetallic -- Figure 25 shows the fracturing of the intermetallic in 95/5 tin/silver, which compares with the intact intermetallic region of 60/40 solder (Figure 26).

The conclusion is that in a poorly designed system which allows minimum compliancy in the assembly and which demands a great deal of compliancy in the solder joint itself, a change to a different solder

may not be of much help. Thus, as one tests either a "more compliant" solder with high creep (exemplified by indium/lead), or a "hard solder" with high tensile strength and low creep (exemplified by 95/5 tin/silver), in either case the rate of fatigue may be similar (50/50 tin/indium, of course, with both low tensile strength and high creep, is in a class by itself). Some advantage is gained with hard solders, but the onset of a different fatigue mechanism may cause catastrophic failure with only a small increase in the solder joint lifetime.

REFERENCES

1. M. Cohen, "Progress and Prospects in Metallurgical Research," in Advancing Materials Research, National Academy Press, Washington, D.C., 1987, p 51.
2. D. A. Fazekas, Proceedings, 11th Annual Electronics Manufacturing Seminar, February 18020, 1987, Naval Weapons Center, China Lake, CA, p 75; ibid, W. M. Wolverton et al., p 339.
3. Principal articles might include: (a) R. N. Wild, IBM Reports No. 73Z000421 and 74Z000481; H. D. Solomon, Proceedings, 36th Electronics Components Conference, p 622; (b) M. C. Shine, L. R. Fox and J. W. Sofia, Brazing and Soldering, Mp/ 9, 11 (1985); (c) L. R. Lichtenberg, Proceedings ISHM, 1984, p 65.
4. Exemplary might be E. Suhir, Proceedings ISHM, 1985, p 383. Also see W. Engelmaier, "Functional Cycling and Surface Mounting Attachment Reliability," Surface Mount Technology, Monograph Series 6984-02, ISHM, 1984, 87-115; H. D. Solomon, IEEE Trans. Components, Hybrids, and Manuf. Technol., Vol CHMT-9, 1986, 622-635.
5. (a) Principles for mechanical analysis performed in this account were taken from Joseph E. Shigley, Mechanical Engineering Design, 3rd ed., McGraw-Hill, New York, N.Y., 1977; and F. L. Singer, Strength of Materials, Harper & Row, New York, N.Y., 1962. (b) For mechanical properties of solder, an excellent compilation is available in J. H. Lau and D. W. Rice, Solid State Tech., 1985, Oct., 91-104.
6. Values for creep rupture suggest this value of 500 pounds/square inch: see Reference 5b; also, G. Becker, 7th Annual Soldering Technology Seminar, Naval Weapons Center, China Lake, CA, Feb. 27, 1983. In any case, tensile or shear strengths of solder are only a magnitude greater.
7. J. L. Marshall and S. R. Walter, Int. J. Hybrid Microelec., 10, 11 (1987).

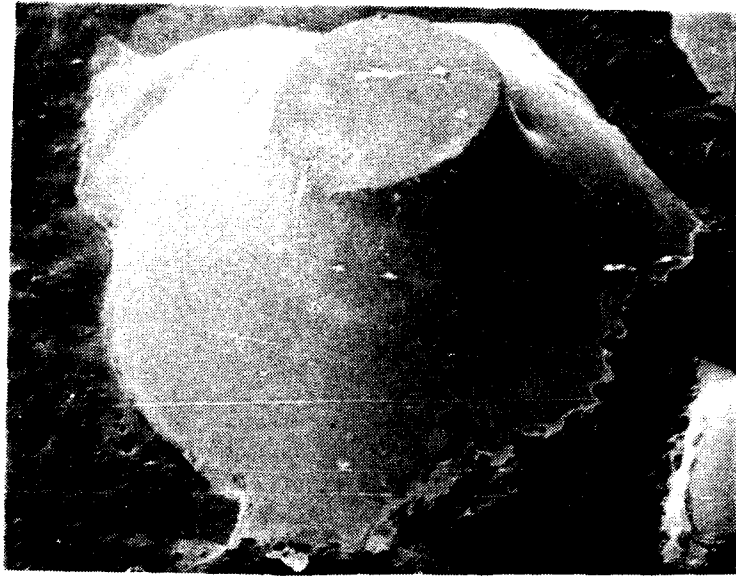


FIGURE 7. Fillet before fatiguing.

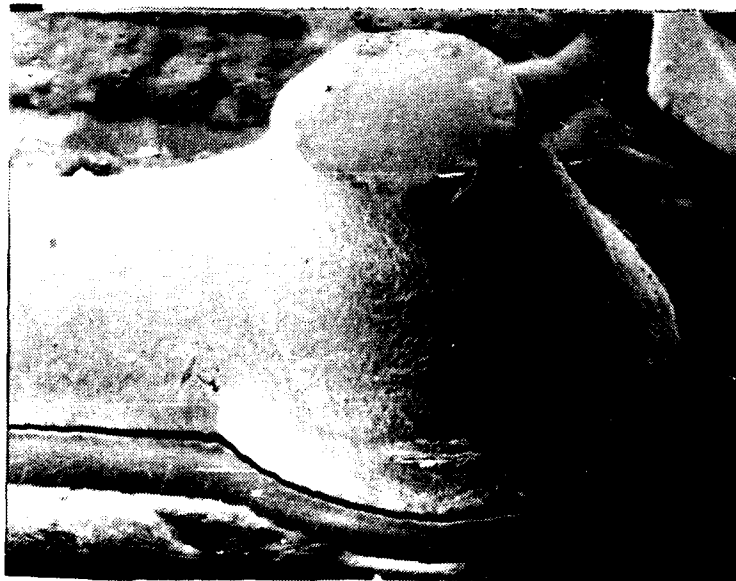


FIGURE 8. Fillet after slight amount of fatiguing.

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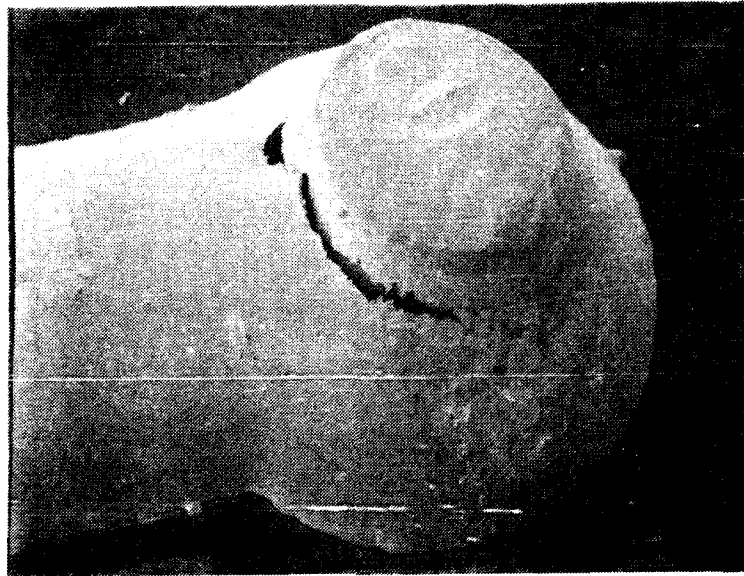


FIGURE 9. Fillet after substantial fatiguing.



FIGURE 10. Fillet after complete failure.

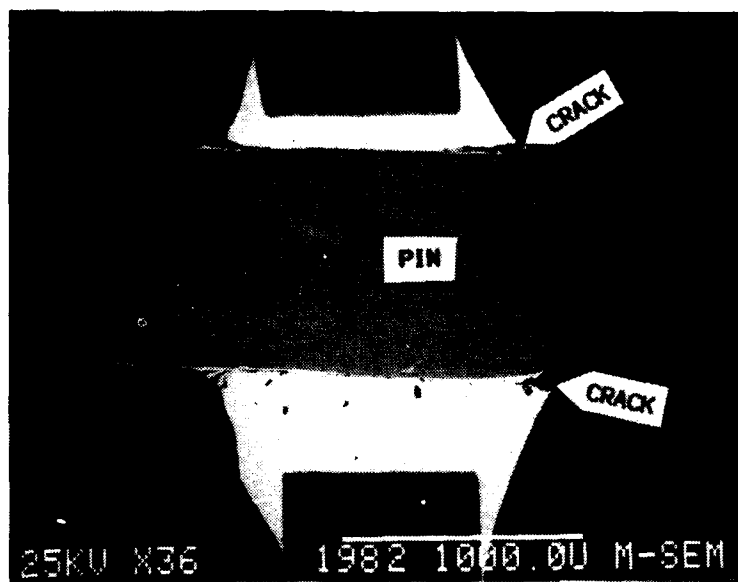


FIGURE 11. Cross section of failed fillet.

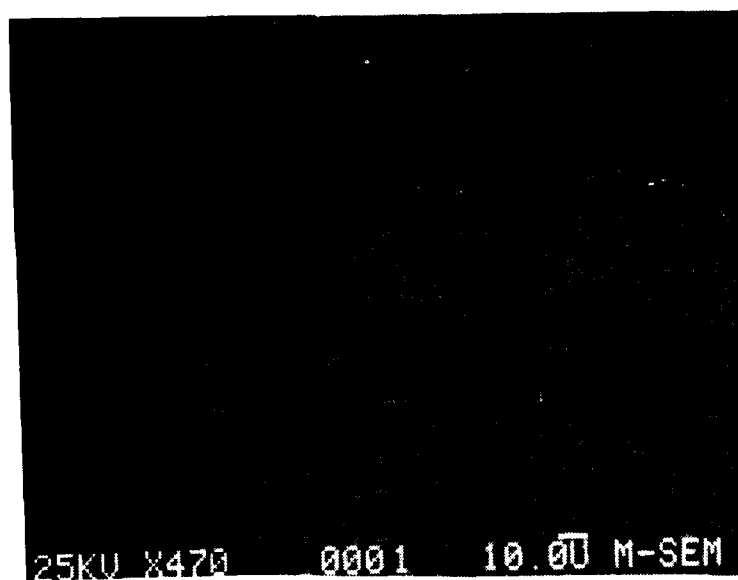


FIGURE 12. Expansion of Figure 11. Failure is through solder.

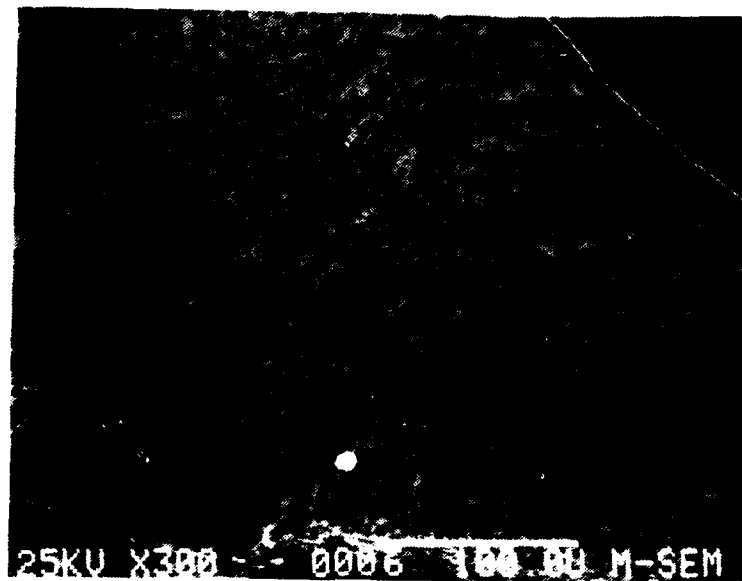


FIGURE 13. Cross section of fillet from Figure 8. Fatigue phenomenon is starting in center of figure, top to bottom.

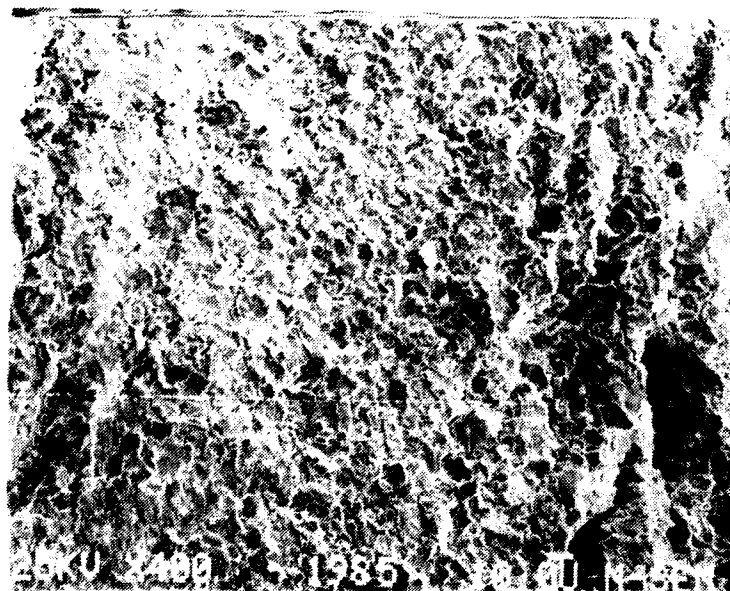


FIGURE 14. Surface of fillet from Figure 8.

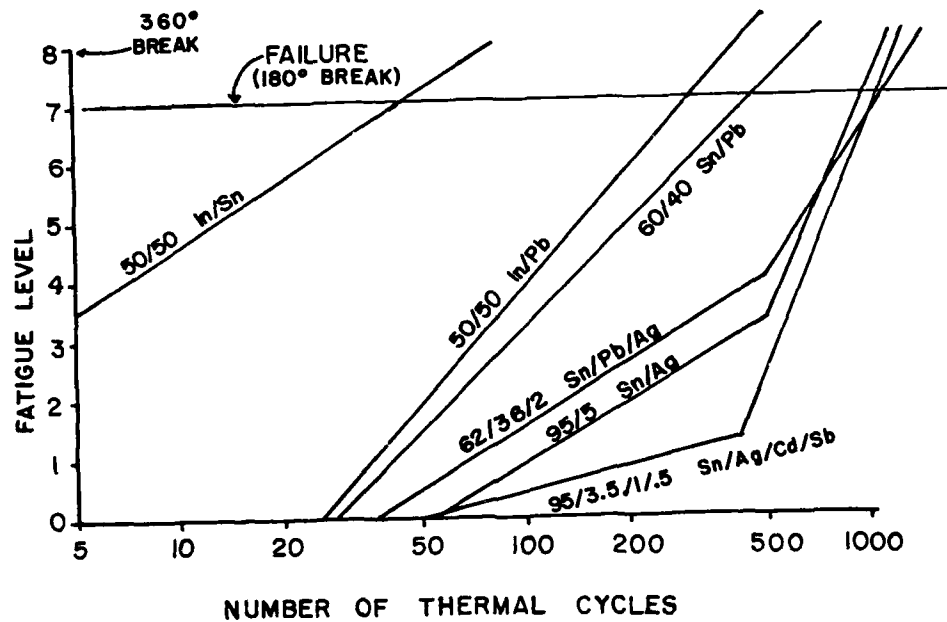


FIGURE 15. Stress-cycle plot of various solders, using assemblies in Figure 6. Solders may have widely different initial fatigue rates, but failure can nevertheless occur after similar exposure times to stress-cycling.



FIGURE 16. Surface of fatiguing 95/5 tin/silver.

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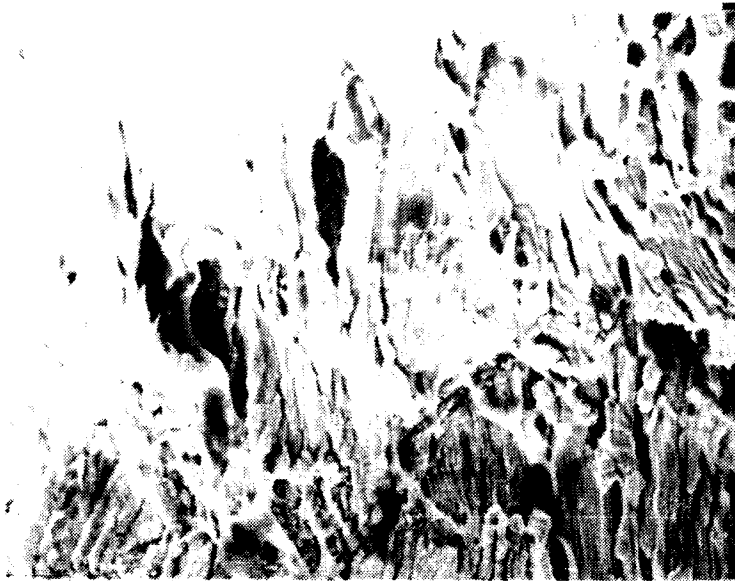


FIGURE 17. Surface of fatiguing 50/50 indium/lead.

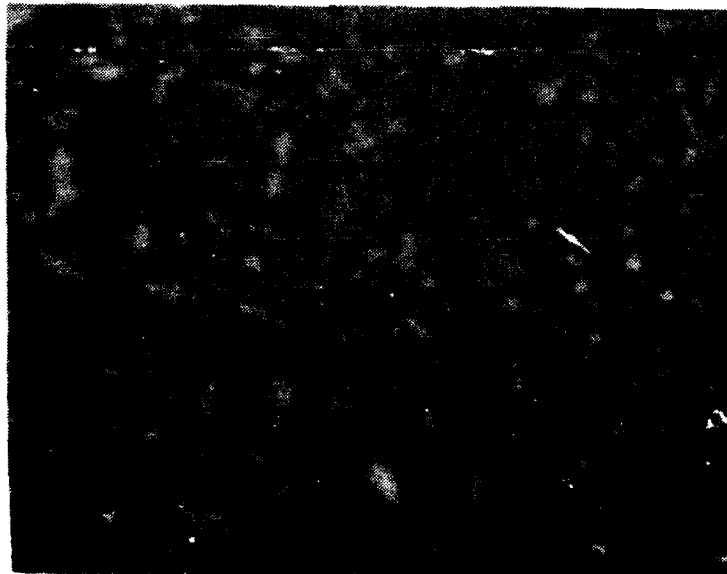


FIGURE 18. Cross section of fatigued 95/5 tin/silver. No domain enlargement has occurred.

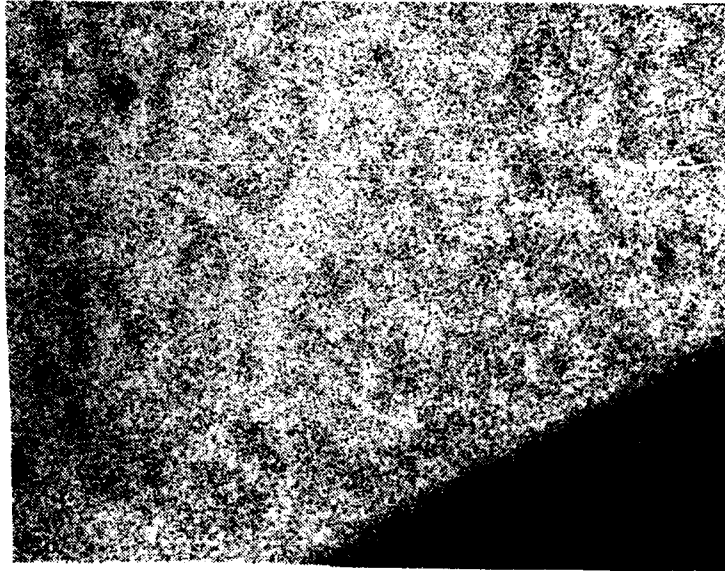


FIGURE 19. Dot map of cross section of fatigued 50/50 tin/indium. Indium-rich and -poor domains remain the same size.

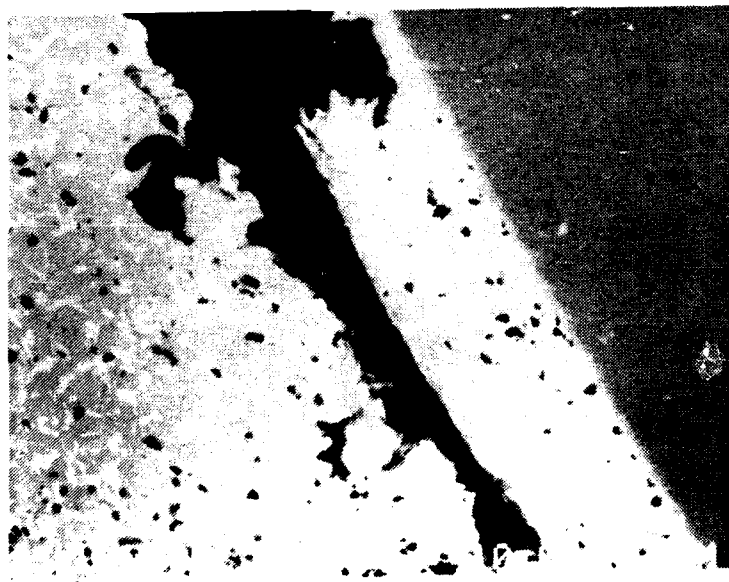


FIGURE 20. Cross section of failed 62/36/2 tin/lead/silver solder.

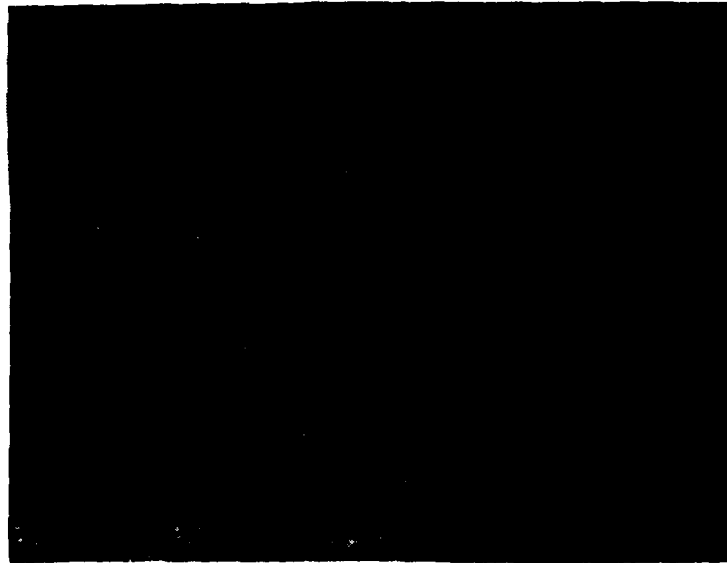


FIGURE 21. Silver dot map corresponding to Figure 20. The silver aggregates during fatigue.

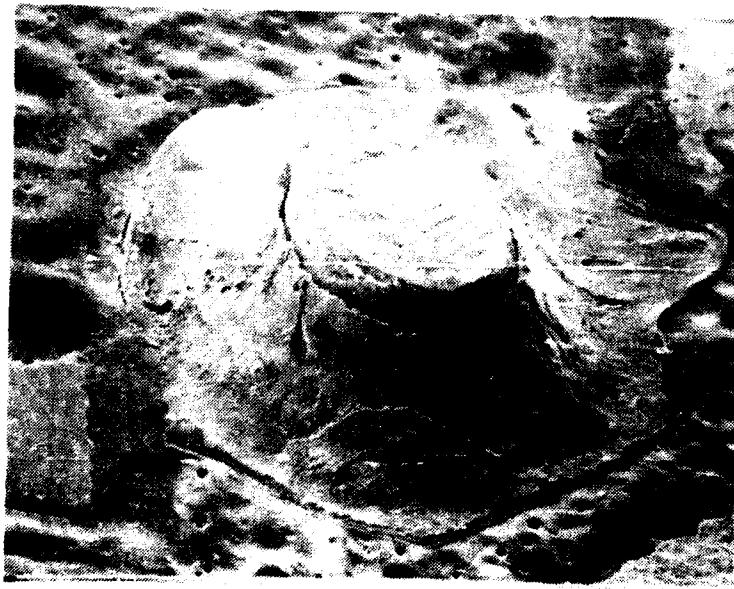


FIGURE 22. Fillet of 95/5 tin/silver, after catastrophic failure.

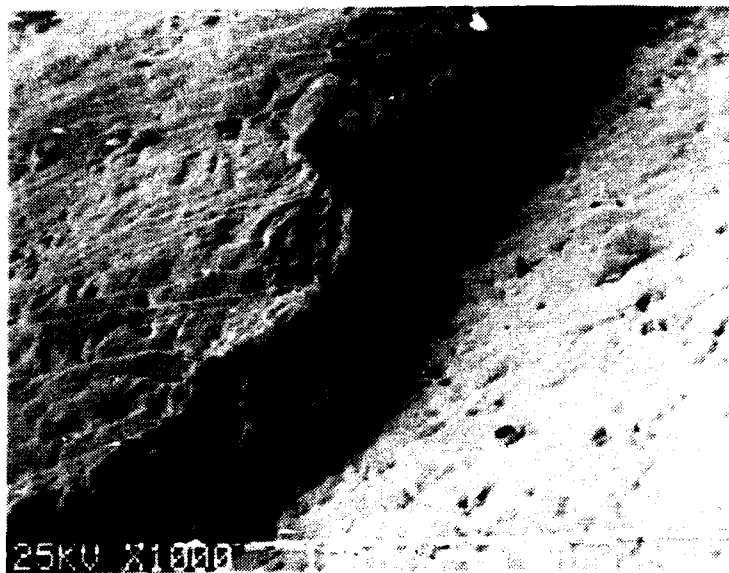


FIGURE 23. Expansion of base of fillet of Figure 22. The brittleness of the solder is evident.



Figure 24. Failed fillet of 50/50 tin/indium.



FIGURE 25. Fracturing at intermetallic in 95/5 tin/silver.

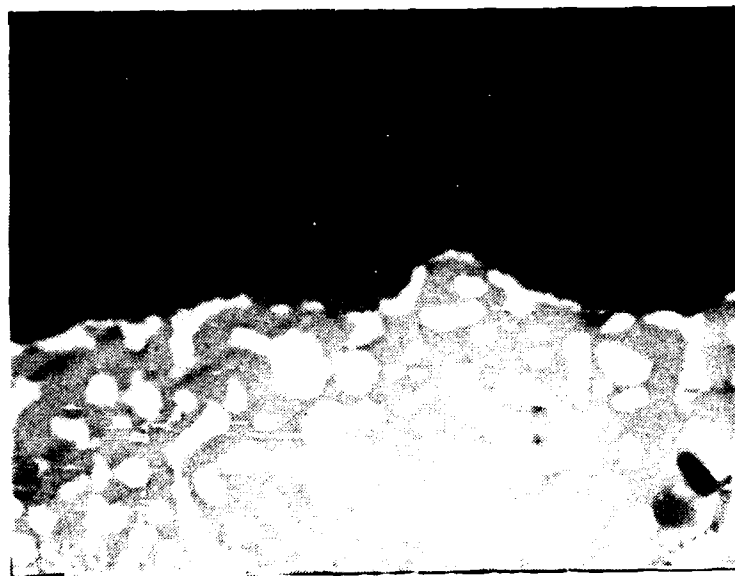


FIGURE 26. Intact intermetallic of 60/40 tin/lead.

Dr. James L. Marshall, professor of Chemistry and Materials Science at the University of North Texas, has written over 60 publications, including a basic reference book in analytical chemistry. He is a member of the American Chemical Society and of ISHM and President of the North Texas Materials Characterization Society, a local affiliate of the Materials Research Society. He also has 6 years' experience in industry. He received his BS degree in Chemistry from Indiana University in 1962 and his Ph.D. in Chemistry from Ohio State University in 1965, and held a postdoctoral fellowship at the University of Colorado in 1966-67.

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WS-6536E & DOD-STD-2000
THE STATUS OF SOLDERING REQUIREMENTS IN THE DEPARTMENT OF DEFENSE

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ABSTRACT

The adoption of WS-6536 as the Navy-wide soldering standard closely followed by the fruition of the multi-year project to develop a DOD-wide soldering standard has resulted in some confusion as to the inter-relationship of the two and considerable concern as to the impacts of implementation of DOD-STD-2000.

This paper discusses the present status of these documents, plans for their use, actions to deal with multi-Service implementation problems and future plans in the area of soldering requirements, including the new Tri-Service process control initiative.

We will briefly discuss the history and structure of DOD-STD-2000, the efforts of the DOD-STD-2000 Ad Hoc Implementation Working Group, how the Services are coordinating on training requirements, facilities and certifications, and future plans for changes and expansion of DOD-STD-2000.

The status of and plans for WS-6536, the results of the industry "top ten" project and new Navy soldering initiatives will also be discussed including plans to phase out WS-6536 in favor of DOD-STD-2000.

Lastly we will discuss the new Tri-Service initiative to provide a process control alternative to the present 100% inspection requirement.

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12/10/87

WS-6536E

DOD-STD-2000

AND

STATUS OF REQUIREMENTS

FOR

SOLDERING OF ELECTRONIC EQUIPMENT

IN THE



DEPARTMENT OF DEFENSE

SUMMARY

DOD-STD-2000

- * BACKGROUND
- * STRUCTURE OF DOD-STD-2000 DOCUMENTS
- * STATUS OF DOD-STD-2000 DOCUMENTS
- * SOLDER TECHNOLOGY STANDARDIZATION WORKING GROUP ACTIVITIES
- * AD HOC DOD-STD-2000 IMPLEMENTATION WORKING GROUP
- * DOD-STD-2000 CERTIFICATION BOARD STATUS
- * FUTURE PLANS FOR DOD-STD-2000

WS-6536 E

- * CURRENT STATUS/PLANS
- * INDUSTRY TOP TEN INITIATIVE STATUS/PLANS
- * CLARIFICATION NETWORK

TRI-SERVICE SOLDERING INITIATIVE

- * CURRENT STATUS
- * FUTURE PLANS

BACKGROUND

- * SOLD STANDARDIZATION AREA CREATED MAY 1978
 - 13 SOLDERING DOCUMENTS CONSOLIDATED INTO ONE FAMILY
- * DOD SOLDERING TECHNOLOGY WORKING GROUP ESTABLISHED JUNE 1980
- * DOD-STD-2000-1 FIRST ISSUED JULY 1982
- * FOUR PART DOD-STD-2000 ISSUED FOR TRIAL MARCH 1985
- * DOD AD HOC IMPLEMENTATION WORKING GROUP ESTABLISHED FEB 1986
- * DOD-COMPONENTS JOINT IMPLEMENTATION MOU SIGNED MARCH 1987
- * REFINED VERSIONS OF ALL FOUR DOD-STD-2000 BASIC DOCUMENTS
FINISHED OCT 1987

STRUCTURE OF DOD-STD-2000 REQUIREMENTS DOCUMENTS

* WHY A FOUR PART DOCUMENT ?

DOD-STD-2000-1 CONTAINS REQUIREMENTS FOR PROCESS CONTROLS
WHICH REDUCE OVERALL COSTS
REPLACED 11 OTHER SPECIFICATIONS

DOD-STD-2000-2 COMPONENT MOUNTING AND DESIGN REQUIREMENTS TO
IMPROVE SOLDER PROCESS EFFICIENCY
INCLUDES REQUIREMENTS NOW IN 5 SPECIFICATIONS

DOD-STD-2000-3 INCLUDES PICTORIAL DESCRIPTIONS OF ACCEPT CRITERIA
ENCOURAGES USE OF COMMERCIAL PRACTICES & STANDARDS
CONSOLIDATES INFORMATION NOW IN 7 DOCUMENTS

DOD-STD-2000-4 LARGELY AND UPDATED VERSION OF MIL-STD-454 REQ'T
5 FOR GENERAL PURPOSE USE, CONTAINS MINIMUM
SOLDERING REQUIREMENTS

STATUS OF DOD-STD-2000 DOCUMENTS

DOD-STD-2000-1 REVISION B AND CHANGE NOTICE 1 ISSUED 10 DEC 86
DOD-STD-2000-2 REVISION A ISSUED 20 NOV 86
DOD-STD-2000-3 REVISION A ISSUED 30 APR 87
DOD-STD-2000-4 REVISION A ISSUED 1 OCT 87
DOD-STD-2000-5 CANCELLED/USING INDUSTRY STANDARD IPC-T-50
DOD-STD-2000-6 (SURFACE MOUNT) UNDER DEVELOPMENT
EXPECTED COMPLETION SEPT 88
DOD-HDEK-2000 UNDER DEVELOPMENT
EXPECTED COMPLETION OCT 88

SOLDER TECHNOLOGY STANDARDIZATION WORKING GROUP ACTIVITIES

- * INCLUDES ALL DOD-COMPONENTS AND INDUSTRY REPRESENTATIVES
- * MEETS THREE OR FOUR TIMES ANNUALLY
- * ESTABLISHES COORDINATED TECHNICAL REQUIREMENTS
- * TECHNICAL PERSONNEL QUALIFIED TO ESTABLISH REQUIREMENTS
- * HAVE COMPLETED DOD-STD-2000 BASIC REQUIREMENTS DOCUMENTS
- * WORKING ON SURFACE MOUNTING REQUIREMENTS FOR INCLUSION IN THE BASIC REQUIREMENTS
- * IS RESPONSIBLE TO DEVELOP THE HANDBOOK AND KEEP THE TECHNICAL REQUIREMENTS UPDATED
- * IS PROPOSING NEW PROJECTS TO IMPROVE SOLDERING IN DOD HARDWARE

AD HOC DOD-STD-2000 IMPLEMENTATION WORKING GROUP

* ESTABLISHED BY DR. WADE, OASD(S&L) 27 DECEMBER 1985

* INCLUDES MEMBERS FROM ALL DOD COMPONENTS

NAVY - M. LAVERSA, CHAIRMAN
ARMY - LEO ST. JEAN
AIR FORCE - ED WESTCOTT
DLA - BILL SWAN
OSD DPSO - JOHN TASCHER

* ACTIVITIES TO DATE

- COMPLETED DOD-COMPONENT MEMORANDUM OF UNDERSTANDING
- ESTABLISHED CERTIFICATION BOARD
- APPROVED OPERATING PROCEDURES FOR CERTIFICATION BOARD
- IDENTIFIED TECHNICAL AREAS FOR STSWG ATTENTION
 - NEED FOR COMPARISON MATRIX FOR THE SERIES
 - RESULTING NEED FOR FLUX CONFLICT TO BE RESOLVED
 - NEED FOR CROSS CERTIFICATION OF SUB-CONTRACTORS
 - NEED FOR RESTRUCTURING OF DOD-STD-2000 SERIES FORMAT
- DEVELOPED A STANDARD APPROACH FOR TRANSITION TO DOD-STD-2000
- COORDINATED A CHANGE TO MIL-STD-454 TO PHASE IN DOD-STD-2000

DOD-STD-2000 CERTIFICATION BOARD STATUS

- * CONCEIVED BY THE AD HOC DOD WORKING GROUP
- * CHARTERED BY THE DOD-COMPONENTS MOU ISSUED 27 MARCH 1987
- * INCLUDES MEMBERS FROM EACH OF THE DOD-COMPONENTS
 - AIR FORCE - JAMES WOODFORD, CHAIRMAN
 - ARMY - DON SHOEMAKER
 - DLA - ALDO DOMENICHINI
 - NAVY - MIKE ROBERTSON
- * ACTIVITIES TO DATE
 - DEVELOPED CERTIFICATION BOARD OPERATING PROCEDURES
 - ESTABLISHED CRITERIA FOR CATEGORY "A" EXAMINER CERTIFICATION
 - ESTABLISHED CRITERIA FOR CERTIFICATION OF SOLDERING SCHOOLS
 - ESTABLISHED PROCEDURES FOR CERTIFICATION OF SOLDERING SCHOOLS
 - DEVELOPED TRANSITIONAL RECERTIFICATION PROGRAM
- * STILL TO BE ACCOMPLISHED
 - CERTIFICATION OF SCHOOLS
 - TRANSITIONAL CERTIFICATION IMPLEMENTATION
 - DEVELOPMENT OF CONTINUING CERTIFICATION PROGRAM

FUTURE PLANS

- * REQUEST STSWG TO RESTRUCTURE DOD-STD-2000 SERIES INTO TASK ORIENTED FORMAT TO FACILITATE TAILORED APPLICATION
- * INITIATE REVISION OF OTHER SPECIFICATIONS AND STANDARDS WHICH IMPACT ABILITY TO ASSEMBLE AND SOLDER ELECTRONIC EQUIPMENT
- * ASSIST IN DEVELOPMENT OF PROCESS CONTROL OPTIONS FOR DOD-STD-2000 AS PROPOSED BY THE 22 SEPT 87 TRI-SERVICE LETTER TO INDUSTRY
- * PROPOSE ALTERNATIVE SOLUTIONS TO THE PROBLEMS OF COST AND AVAILABILITY OF TRAINING FOR DOD-STD-2000
- * PROPOSE ESTABLISHMENT OF A PERMANENT DOD-STD-2000 POLICY BOARD TO REPLACE THE AD HOC WORKING GROUP

WS-6536 E * CURRENT STATUS/PLANS

- * SCN 2 HAS BEEN ISSUED
- * SCN 3 ISSUED TO CORRECT SOME TYPOGRAPHICAL ERRORS
- * STILL BEING USED FOR MOST CONTRACTS - EQUIVALENT TO DOD-STD-2000
- * "OFFICIAL" REPLACEMENT POLICY TO BE ISSUED SOON
- * TO BE INACTIVATED FOR NEW DESIGNS BY SPRING 1988 AND REPLACED
BY DOD-STD-2000-1, 2 & 3

WS-6536 E * INDUSTRY TOP TEN INITIATIVE STATUS/PLANS

- * SCN 2 CONTAINED MOST OF THE CHANGES NEEDED TO CONCLUDE THE PROJECT
- * FIVE MAJOR OPEN AREAS WERE DISCUSSED AT THE "TOP TEN" MEETING ON 9 NOV 1987
 - SOLDER IN THE BEND RADIUS - DATA REVIEW COMPLETED/TEST PLAN BEING DEVELOPED
 - GENERIC TRAINING PROGRAM - ESD AND TEST QUESTIONS ISSUES TO BE RESOLVED BY 31 JAN 88
 - MRB - WILL REVOKE MRB REQUIREMENTS TO ELIMINATE SUB-CONTRACTOR PROBLEMS
 - ORGANIC ACID FLUXES FOR COMPONENT PRE-TINNING - ONE PROCESS "APPROVED" MEETING TO BE HELD TO SET UP APPROVAL PROCEDURES
 - THE "OTHER 37" ISSUES - NO FURTHER ACTION, TO BE HANDLED UNDER DOD-STD-2000
- * DOD-STD-2000 "TOP TEN" TYPE PROJECT TO BE ESTABLISHED

WS-6536 E * CLARIFICATION NETWORK

- * INITIAL QUESTIONS SUBMITTED BY INDUSTRY HAVE BEEN ANSWERED (EXCEPT FOR TWO)
 - * THE REMAINING TWO QUESTIONS TO BE COMPLETED BY 22 DEC 87
 - * NETWORK IS NOW ON LINE
- QUESTIONS - 1 (800) 327-4996
- ANSWERS (CCN) - (202) 746-2645

TRI-SERVICE SOLDERING INITIATIVE * CURRENT STATUS

- * TRI-SERVICE LETTER SENT TO INDUSTRY 22 SEPT 87
- * DOD-STD-2000-1, 2 & 3 BASED PROGRAM PREFERRED
- * TO DATE OVER 30 RESPONSES HAVE BEEN RECEIVED
- * FEW ACTUAL PROPOSALS HAVE BEEN RECEIVED SO FAR
BUT MANY ARE IN PREPARATION
- * INDUSTRY WORKING GROUP - "TOP TEN" GROUP
PROPOSED PROJECT TO DEVELOP APPROACH

TRI-SERVICE SOLDERING INITIATIVE * FUTURE PLANS

- * TRI-SERVICE PLANNING SESSION BEING SCHEDULED IN JANUARY
- * PROPOSAL SCREENING PLAN BEING DEVELOPED
- * "TOP TEN" GROUP WILL BE ASKED TO ASSIST IN DEVELOPING A GENERALIZED APPROACH
- * ACTUAL IMPLEMENTATION TO BEGIN SPRING 1988

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Artificial
Intelligence in the Manufacturing
Environment:
Expert Systems in the WaveSolder
Process

Prepared
and
Written
by

Matthew R. Fulton & Joseph A. Gotsens

Abstract

This paper deals specifically with the use of an expert system in an automated wave soldering process. The system is briefly outlined after an introduction of the topic and a summary of the project's background. An outline of the system's flow as well as figures outlining and depicting screens in the diagnosis mode are also provided. Work was performed at Honeywell Inc., Tampa, Florida.

Introduction

Artificial Intelligence -- the phrase can conjure up some pretty fantastic images of a future life controlled entirely of super computers and robots. In fact, those images will not mirror reality for years to come (if at all). The reality of the situation is that today there are many opportunities to put already accomplished in the field of artificial intelligence to good use throughout the manufacturing industry. For example, one of the bi-products of artificial intelligence (which will simply be defined here as a computer capable of making decisions that parallel logical human thought processes and which should have the ability to make inferential decisions) is the sub-area of expert systems. An expert system is one in which a computer exerts control over a process that would normally or otherwise be controlled by a human being. Even at this moment, there are expert systems functioning in automated processes in American industry. The topic of this technical brief is one such application -- the use of an expert system in a wave soldering process.

Background

This project developed due to the mutual interest of Honeywell Defense Communications and Production Division (Tampa, Florida) and the University of Florida Database Systems Research and Development Center (Gainesville, Florida). Sponsored by the Navy Manufacturing Technology Program through the National Bureau of Standards (grant number 60NANB4D0017) and by the Florida High Technology and Industry Council (grant number UPN85100316), this project was started in the spring of 1987. The University of Florida provided the database and research oriented support, while Honeywell supplied the knowledge and engineering expertise related to the automated wave soldering process to be incorporated into the expert system.

As the project developed, University of Florida utilized a commercially available expert system shell into which the appropriate data, information, and rules were adapted. The knowledge engineering effort identified the need for novice and expert expert systems with the former helping the user to identify even the most basic characteristics of solder defects as well as the rules necessary to make process corrections, and with the latter supplying the rules and associated data necessary only to tweak the process for its most optimum performance.

After a thorough evaluation of the University of Florida shell, Honeywell turned to its own internal resources. The shift became necessary after it was obvious the commercial shell did not possess the necessary hookups needed to utilize it with the current Honeywell statistical process control programs or enough memory to handle even all the rules for two circuit card assembly styles.

Honeywell currently manufactures some three hundred different circuit card assemblies in its automated wave soldering process. The memory problem became a real issue when large sections of the rules base were lost on two occasions.

As Honeywell's interest was in the area of process control and the elimination of the redundant effort performed day-to-day by its process control engineers (80% of the situations which are encountered in this process can be handled by a rules based expert system), the significance of real-time interfaces with the actual process were highlighted. Using the current statistical process control database and the current process cutoff of five defects per one thousand possible solder connections normalized per circuit card assembly style, Honeywell quality assurance and audits group personnel began writing their deductive expert system in the same database language the statistical program utilized. That link eliminated the hookup problems previously encountered with the commercial shell. It also allowed for real-time interface with the process.

The System

The system consists of two personal computers, a computer program with a statistical mode, database, and diagnosis mode. The system, as currently designed, will function as follows:

Step 1-- Operator/Inspector inputs defect data from product as it is sampled in-process into the statistical mode called KU Chart

Step 2-- Data is calculated by the statistical program which provides an accept/reject decision based on the normalized process parameters.

Note: If product is defined as A or R-, then it will continue processing. Product rejected as R+ will have processing discontinued and the expert system will send the operator/inspector into the diagnosis mode.

The diagnosis mode is the heart of the expert system. After a main menu screen, the operator inputs type of assembly and board style configuration. The analysis requires the operator/inspector to identify the defect contributing most significantly to the reject status. Once identified, the system steps the operator/inspector through three corrective actions per defect type, pausing between each to receive data to analyze whether product is now acceptable. If acceptable, then the system bombs out and allows processing. If still reject, then the next corrective action is identified and attempted (this is true after choice 1 & 2). After corrective action 3, the system alerts the operator/inspector to bring the appropriate process engineers into the loop. The engineer

must then determine whether to process product or keep the process in a shutdown mode. A series of figures are attached (Figures 1 through 13) which sequentially show the system screens. Note that not all screens are shown and this is representative of the system at the time the brief was being prepared. There are modifications in process at this time.

Future Plans

There are several changes in progress. Several screens are being modified to eliminate some of the redundancy from the program itself. In addition, the titles of the corrective actions are being modified to reflect the decision tree identified in Figure 14 which was added at the last moment. In the far distant future, the authors envision a more sophisticated system which would eliminate the need for an operator/inspector to identify defects and input data. As the technology is developed, those two functions could be performed by either an electronic eye or lasers. The final change would be the link of the computer microprocessor in the wave soldering machine to the expert system with the result that the system could perform process corrections without human interference unless no satisfactory results could be obtained within the specified parameters and an engineer was required for restart authority.

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Figure 1.
Main Menu Screen for System

***** Main Menu *****

- (D) Database
- (I) Input Data
- (Q) Quit

Enter Choice:

Command

(C:) DMP

Rec: 26/26

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Figure 2.
Data Input Screen

K Factor: 1000

Date: 12/15/87 Part Number: A3041438

Defects in Sample: 60 Sample Size: 4

Opportunity Factor: 1217

Comments:

Lot Number(s):

Command (C:) DMP Rec:1/27

(B):Save-Exit; (D):Del.-Exit; (E):Edit; Disposition is R+

Figure 3
KU Chart Accept/Reject Screen

PWA WAVE SOLDER ACCEPTANCE CRITERIA - LAST DISPOSITION -

Part Number: A3041438 Program: DMP
=====

Type of Chart: KU Chart

UCL = 8.04
Mean = 5.00
LCL = 1.96

Sample Defects/1000 = 12.33

Disposition: R

Press Any Key To Continue...

Command

(C:) DMP

Rec: 28/28

Disposition is R+

Figure 4.
Diagnosis Menu Screen 1

-Diagnosis Menu-
=====

Select Type of Board: (1) Multilayer (2) Double Sided (3) Quit (cr)

Command

(C:) DMP

Rec: 28/28

Figure 5.
Diagnosis Menu Screen 2

-Diagnosis Menu-
=====

Select Type of Board: (1) Multilayer (2) Double Sided (3) Quit (cr) 2

Current Part Number: A3041438 Program: DMP

Type of Joint: (1) PTH (2) NPTH (3) Quit (cr)

Command

(C:) DMP

Rec: 28/28

Figure 6.
Diagnosis Menu Defect Identification
Screen 3

PTH Double Sided PWA

Select from items below:

- (1) Solder Sufficiency Defects (2) Lead Defects (3) Fillet Defects
- (4) Quit

Enter Choice: 1

Command (C:) DMP Rec: 28/28

Figure 7.
Diagnosis Menu Corrective Action Choice 1

Part Number: A3041438 Program: DMP

Action: Excess Solder; Slow Conveyor Speed. Trial 1

Make Process Adjustment; then Press any key to continue

Command (C:) DMP Rec: 28/28

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Figure 8.
KU Chart Data Input Screen After Choice (C.A. 1)

Part Number: A3041438 Program: DMP

K Factor: 1000

Date: 12/15/87 Part Number: A3041438

Defects in Sample: 58 Sample Size: 4

Opportunity Factor: 1217

Comments:

Lot Number(s):

Command (C:) DMP Rec: 1/28

(R):Save-Exit; (D):Del.-Exit; (E):Edit; Disposition is R+

Figure 9.
KU Chart Accept/Reject Screen After Choice (C.A. 1)

PWA WAVE SOLDER ACCEPTANCE CRITERIA _ LAST DISPOSITION

Part Number: A30141438 Program : DMP

Type of Chart: KU Chart

UCL = 8.04

Mean = 5.00

LCL = 1.96

Sample of Defects/1000 =11.91

Disposition: R

Press any key to continue

Command (C:) DMP Rec:29/29

Disposition is R+

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Figure 10.
Diagnosis Menu Corrective Action Screen Choice 2

Action: Excess Solder; Adjust Wave Height. Trial 2
Make Process adjustment; then Press any key to continue...

Command (C:) DMP Rec: 29/29

Figure 11.
KU Chart Data Input Screen After Choice (C.A. 2)

K Factor: 1000
Date: 12/15/87 Part Number: A3041438
Defects in Sample: 30 Sample Size: 4
Opportunity Factor: 1217

Comments:

Lot Number(s):

Command (C:) DMP Rec: 1/29
(B):Save-Exit; (D):Del.-Exit; (E):Edit;

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Figure 12.
KU Chart Accept/Reject Screen After Choice (C.A. 2)

PWA WAVE SOLDER ACCEPTANCE CRITERIA - LAST DISPOSITION -

Part Number: A3041438 Program: DMP
=====

Type of Chart: KU Chart

UCL = 8.04
Mean = 5.00
LCL = 1.96

Sample Defects/1000 = 6.16

Disposition: A

Press any key to continue...

Command (C:) DMP Rec: 30/30

Figure 13.
Diagnosis Menu Screen After Choice (C.A. 2)

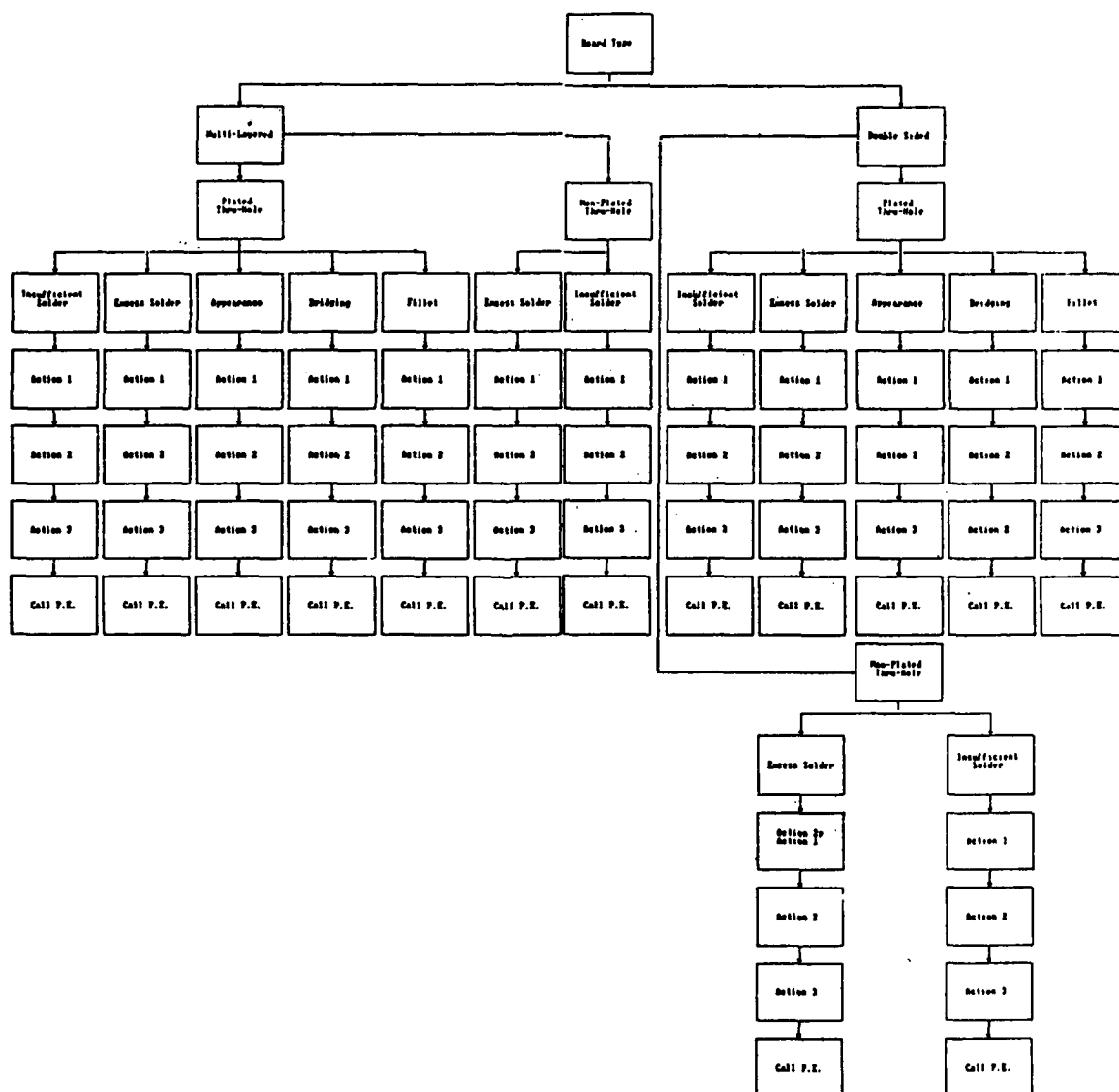
Disposition was A

Action was: Excess Solder; Adjust Wave Height. Trial 2

Did wave height adjustment solve the problem y/n Y

Figure 14.
Diagnosis Mode Tree

FOR HAVE SOLDER PROCESS CONTING



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PROJECT PLANNING AND INSTALLATION OF INTEGRATED SURFACE MOUNT PRODUCTION CAPACITY

by

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ABSTRACT

This paper will concentrate on a new procedure for the documentation of Strategic Net Yield for surface mount production line equipment. The approach presented herein differs significantly from traditional methods for evaluating the throughput of production equipment.

The nature of surface mount technology demands close evaluation of equipment performance and capabilities long before the production line is established. To achieve optimum performance — and maximum yields — with SMT, the user must consider a number of criteria that have not necessarily been critical to the through-hole process.

On a surface mount production line, the pick and place assembler is the key variable when attempting to predict potential yield and throughput, and therefore the discussion will be focused on this keystone unit.

The paper will illustrate the relative importance of speed, accuracy, flexibility, reliability and other factors pertinent to strategic net yield. This will be achieved through the use of a numerical model in which values for each of the aforementioned factors can be manipulated.

Finally, the paper will look at the capacity planning steps necessary to establish an integrated surface mount production line.

A NEW LOOK AT PRODUCTIVITY

OVERVIEW

Changes in manufacturing processes require changes in evaluative methods. As a growing number of manufacturers — in defense and other disciplines — have begun to consider surface mount technology to meet the demand for increasingly smaller, faster and less expensive products, it has become obvious that traditional approaches to the evaluation of equipment performance and capabilities are inadequate. Due to tremendous differences between the two, what seemed to be true and reasonable assumptions for through-hole manufacturing simply do not hold for surface mount.

Analysis of Strategic Net Yields provides a new, more effective model for evaluating the true capacity of high-volume surface mount production lines.

BACKGROUND

Through-Hole Assembly

Through-hole assembly was the predominant electronic manufacturing technology in the 1970s. Inherently robust, its operational tolerances are much less critical than those of surface mount and, in general, these tolerances are an order of magnitude more forgiving. Their impact simplifies all aspects of the process, from board fabrication to touch-up. (Refer to Table 1.) During the insertion process, leads need not be dead center — even if a lead hits the rim, its tendency is to deflect, and successful insertion is achieved more often than not. Through-hole's clinched leads make material handling, parts storage and effective wave soldering inherently easy. Assembly errors are easily visually detected and can be corrected manually at a reasonable cost. Over the years, the through-hole assembly process evolved into a pattern of "insert, visually detect errors and correct manually." The expected defect percentage rate was low, as some manual detection and correction was considered reasonable. In the acquisition equation, extremely low defect rates without operator intervention were not considered critical.

The widespread result has been that many through-hole lines have been producing financially acceptable yields, but have not been performing to the physical limits of the technology. This non-optimization of process has led buyers to utilize speed and cost, i.e. cents per insertion, as key measurements when considering production line equipment for increased capacity. The view of process net yield was not necessary.

Working in this environment, many production engineers never had the need to examine the production process closely. What errors were detected at different stages of the process were repaired relatively easily, and so the system seemed to work well. A process error rate of 1-2% seemed low, and product was being built. Unfortunately, many are now finding that the transition to SMT is unsatisfactory — because they harbor several misconceptions born of several decades of working with through-hole technology.

When faced with the "career opportunity" to implement SMT in the '80s, these production engineers find themselves inadequately prepared from a technological standpoint and biased with regard to acceptable process performance. Since the pain of a poor introduction and start-up is common, it is possible to conclude that the traditional method of planning, evaluation and preparation based almost exclusively on speed and acquisition cost contains some inherent deficiency. Further complicating the situation is the fact that many of these through-hole-biased production engineers often have no experience in the surface mount process nor with statistical process control.

Surface Mount Technology

In a very short time, surface mount technology has revolutionized electronics manufacturing by making it possible to produce superior boards from the viewpoint of cost, size and performance. Currently, an estimated 30% of the industry is using surface mount to some extent in the manufacturing process. For the rest, the switch is not a matter of "if," but "when and how." Yet too many who have adopted this manufacturing process have been disappointed by the results. Reports of first pass yields as low as 7% have been received from the field.

TABLE 1. Through-Hole and SMT: A Comparison

<u>Through-Hole</u>	<u>SMT</u>
<ul style="list-style-type: none"> • Board fabrication tolerances loose • Lead into holes self-correcting • Errors in each process easily visually detected • Clinched leads make parts handling and storage easy • Hand assembly is typical <ul style="list-style-type: none"> a) Use hole to align part b) Clinch over to hold part c) Part jostling not critical • Wave solder of wire in barrel potentially very effective and robust • Touch-up is commonplace <ul style="list-style-type: none"> a) Quick and easy with leaded parts b) Many trained operators c) Allows clean-up of other process errors d) Acceptable approach from management viewpoint e) Equipment is inexpensive 	<ul style="list-style-type: none"> • Tight board fabrication tolerances • Fine lines and spaces • Assembly not self-correcting • Reflow improves high-yield process, but cannot fix out-of-control process • Visual inspection more difficult; often requires magnification • Many part values not marked • Boards must be reflowed soon after assembly to prevent paste over-drying and movement of parts • Deceleration conveyors necessary for smooth transitions and minimal parts movement • Hand assembly is difficult <ul style="list-style-type: none"> a) No alignment features b) No holding features c) Parts can be moved d) Paste can be smeared e) Handling of completed board prone to jostle components • Wave solder is difficult <ul style="list-style-type: none"> a) Requires special wave shapes still under development b) Components prone to thermal shock damage c) "Opens" due to layout d) "Shorts" due to tight spacing • Touch-up is undesirable <ul style="list-style-type: none"> a) Parts are small and close together b) Trained labor less available c) Visual detection of some joints is difficult (J-lead) d) Time-consuming and expensive e) Rate of repair usually biggest management shock after equipment is in place f) Specialized equipment necessary

Surface mount, by nature, is not a very forgiving technology. Tolerances are critical and becoming more so as more finely pitched components become readily available. Today 50-mil pitch components are the norm, and 31- and 25-mil components are being seen frequently. SMT's allowable error band is a mere fraction of acceptable through-hole performance. Typical process error bands of 0.004 to 0.008 — acceptable with 100 mil center line through-hole technology — can absorb SMT's processing window completely.

The differences between surface mount and through-hole are apparent at nearly every step in the process. (Refer to Table 1.) Component placement, board handling and transport, wave soldering and touch-up processes on a surface mount line are all much less robust than those steps on a through-hole line. Not only is accurate placement more difficult with small, finely leaded surface mount components, but movement after placement becomes a concern. The sheer size difference between through-hole and SMT components makes the equipment different, visual inspection difficult and rework of errors time consuming and expensive.

In light of these considerations, process line performance, and its evaluation prior to procurement, becomes significantly more critical. In particular, experience has shown that the pick and place assembler has the greatest leverage in controlling this performance. It is, therefore, especially important to select the best unit for the job.

Statistical Process Control

Introduced in 1931 by Walter Shewhart, Ph.D., in his book, *Economic Control of Quality Manufacturing Production*, the concept of Statistical Process Control was soon embraced by the chemical processing industry as a vehicle for maintaining high quality standards throughout their production processes. Only recently have those in the electronics industry come to see the method's viability. SPC's newfound acceptance is particularly appropriate in the light of the growing interest in surface mount, for this method of quality control lends itself well to SMT manufacturing environments.

As opposed to traditional quality control methods, Statistical Process Control dictates that the manufacturing process itself be monitored. Corrections and adjustments are made to the process and the equipment, rather than to the finished product. The required mindset is one of defect prevention rather than detection and correction.

SPC involves process capability studies to determine what performance levels can be expected of the equipment. Error rates are then tracked and corrected before they reach unacceptable levels. To do this successfully requires a complete and thorough understanding of the process — often down to the most basic physics. An ability to find the root of any problems in order to prevent further defects is also necessary. The proven result is a dramatic increase in net yields.

SPC also has significant value in the determination of process performance expectations. While through-hole traditionalists speak of error rates in terms of 1-2%, SPC proponents speak in parts per million. Process performance under 100 ppm, with a target of zero becomes a reasonable expectation — and one that is far beyond the expectation both engineers and managers not experienced in SPC.

The Pick And Place Assembler

In the surface mount production line, the pick and place assembler has the greatest impact on line performance. It is the only piece of equipment in the entire line that individually handles every single component in the assembly. This increases the probability that an assembler could cause an error by several orders of magnitude. For example, a stencil printer operating at 100 ppm will have a 100 ppm probability of being the cause of an error — because it performs a single operation. In contrast, consider an assembler also operating at 100 ppm and populating a board with 150 components. It performs 150 operations and has a probability of error of 14,888 ppm. Statistics show that the probability of error increases geometrically rather than in a linear manner with each additional operation.

The high number of operations it must handle makes the assembler the key determinant of capacity for the production line. Depending on board size, population density and placement rate, the assembler may be a number of times slower than the next slowest unit on the line. Naturally there is a desire to increase assembler speed. However, such an increase can prove detrimental to final net yield figures if the increase in speed occurs with even a small decrease in placement reliability.

Unlike other surface mount equipment, the pick and place assembler offers little process variable control. Screen printers, reflow ovens and cleaners have parameters — such as snap-off height, reflow temperature profile or spray pressure — that can be adjusted to optimize process performance. The assembler's performance, on the other hand, is primarily a function of its design and features. The inherent process capability provided by this piece of machinery is "designed-in" rather than "adjusted-in." Therefore, the only real opportunity to control proper performance is during the procurement cycle. This makes selection of the optimum assembler for the job absolutely essential in order to maximize net yields.

It must be re-emphasized at this juncture that, for many, the through-hole experience has not provided the necessary expectations, or the technological approaches, for installing high-yield SMT production lines that will operate with optimal cost figures. The following discussion is intended to aid low-risk entry into SMT with minimal leadtimes and rapid start-up.

STRATEGIC NET YIELDS

A new method used to evaluate high-volume surface mount production lines takes a strategic approach to increasing net yields. When properly implemented, this approach provides for greater capacity, higher quality and lower unit costs.

It is no longer enough to specify that an assembler populate X boards/hour with $\pm Y\%$ accuracy. Applied to the pick and place assembler, the concept of Strategic Net Yields requires that the manufacturer examine the actual cost to produce an acceptable board, considering such factors as reliability, flexibility, accuracy/repeatability and production speed, as well as their relative weight. By making certain assumptions, it is possible to develop a numerical model that can be used to judge the merits of various assemblers.

As indicated previously, thorough evaluation prior to acquisition is key to selection of equipment with the desired inherent capabilities. None of the following factors is adjustable — they are all functions of equipment design. Strategic Net Yield allows the process line planner to evaluate key pick and place operational factors and obtain more realistic estimates of expected performance. Performance is clearly defined as total cost per board rather than as speed or accuracy alone.

Reliability And Flexibility

Two factors that have a strong impact on strategic net yields are reliability and flexibility. Both affect the actual production time available during a given manufacturing period — and ultimately, the cost to complete each board.

Reliability, in this discussion, refers to that production time lost to equipment failure or routine maintenance. It has a clear impact on yields, as a fast machine that requires extensive downtime is, in effect, slower than a machine that produces fewer boards per cycle, but that offers more available production time. An actual figure for the reliability of a particular piece of equipment is often difficult to determine based on data provided by the supplier. Also, published Mean Time Between Failure numbers, on the whole, tend to be in error. Users who can provide real data from practical experience are the best source of information on the reliability of any given assembler in continuous use. Names of these can usually be obtained from the manufacturer.

In surface mount, flexibility also becomes a factor. Changeover requires time for reprogramming, moving component feeders or changing components, which detracts from actual available net production time. If the assembler is unable to place complex parts, manual placement must be factored into the strategic net yield equation as well. The difficulty and cost of manual placement, as indicated earlier, tends to make flexibility (or the lack thereof, as the case may be) the pick and place assembler's Achilles Heel.

Accuracy And Repeatability

According to consultant Philip Crosby, author of *Quality Is Free*, the cost of rework typically runs an average of 20% of sales. Through-hole assembly allows for correction at various stages in the process. However, surface mount leaves little tolerance for placement error. The nature of the technology requires that manufacturers maintain high-performance, low-defect-rate processes. The ability to place a component in the target location is a determinant of machine performance. First Pass Yield — the acceptance rate of boards at First Test after assembly — becomes an absolutely critical measurement, and accuracy of placement and repeatability are critical determinants of First Pass Yield.

Ironically, this is the area of widest variability. SMT engineers report First Pass Yields as low as 7% and higher than 99%. Obviously this figure plays a major role in determining the final cost per board. Incremental increases in First Pass Yield percentages can force assembly costs down dramatically.

Production Speed And Equipment Cost

In traditional methods of evaluating through-hole assemblers, speed and equipment costs were the major contributing factors. As we have indicated, through-hole process variables tend to be robust and easily corrected by operators. Most companies fail to realize how much repair is taking place. In SMT, by contrast, other factors overshadow speed and cost. Speed is the deciding factor only when all other factors are equal. And acquisition costs can be overshadowed by more important production factors such as reliability, accuracy and flexibility.

Any number of figures are available relative to the speed of any given assembler, and most are irrelevant in light of Strategic Net Yield. Ultimately, the number of acceptable boards produced in a given manufacturing period matters far more than components placed per hour or cycles per hour — even if those figures were entirely accurate and based on actual operation, which most are not.

SNY: A NUMERICAL MODEL

Developing Input Data

Tables 2 and 3, respectively, indicate the input variables and formulas for performing strategic net yield calculations, while Table 4 represents a typical application. In actual use, the line planner would input data from the various machines under evaluation, adjusting variables as appropriate. By running numerous scenarios, it is possible to evaluate the effects of various line conditions. Due to the sheer number of input variables involved, this method — known as sensitivity analysis — allows effective prediction of line performance.

Key Measure

The Strategic Net Yield model results in four key measures which, when used with differing scenarios, allow easy comparison of 15 diverse input variables.

Total assembly cost. The first measure is total assembly cost. All things considered, the total cost per month is a measure of the size of the production operation.

Assembly cost per board. Assembly cost per board is the dollar value being carried on a board-by-board basis. Obviously, the more boards produced (i.e., the higher the yield), the lower the per-board cost.

Effective yield. The effective yield is the ratio of good boards produced on the first try to the total possible number of boards that could be produced with perfect processes and 100% available equipment. While first pass yield measures the rate at which boards are accepted, effective yield also takes into consideration the time during which the machinery is not productive. In gross terms, effective yield represents the acceptance rate on a period basis, while first pass yield represents an instantaneous basis.

TABLE 2. Strategic Net Yield Variables

1. Scheduled production hours per month.
2. Number of operators required
3. Number of production changeovers per month
4. Direct material cost
5. Burdened labor cost per hour
6. Rework minutes per unit
7. % of rework scrapped (one of an assortment of methods available to estimate scrap costs)
8. Seconds per manual placement
9. Components per board
10. Pick and place machine rate in components per hour (including board handling)
11. Reliability (downtime per month for required maintenance or repair)
12. Flexibility (minutes per product changeover)
13. Flexibility (% manual placement required)
14. First pass yield (including all defect classes either machine- and process-sourced or component-sourced)
15. Equipment cost

TABLE 3. Strategic Net Yield Formulas

- A. Determine available production hours by subtracting maintenance time and total changeover time (which is the number of changeovers multiplied by the changeover time) from scheduled time.
- B. Determine the quantity of boards produced in that period based on the machine rates.
- C. The number of good boards is equal to the total number of boards produced times the first pass yield.
- D. Based on the first pass yield, determine the number of boards that will require rework.
- E. The number of boards scrapped is the percentage of rework scrapped times the number of boards reworked.
- F. Based on total quantity of boards produced, subtract those scrapped to determine the total quantity built per month.
- G. Scrap cost is the number of boards scrapped at the direct material cost.
- H. Assembly cost is the number of operators at the burdened rate.
- I. Rework cost is the rework minutes per unit multiplied by the labor rate times the number of units.
- J. Maintenance cost is the labor rate multiplied by downtime in hours.
- K. The manual placement cost is the labor rate multiplied by the time per manual replacement, the number of components per board manually placed and the number of total boards. The number of components manually placed is the number of total components per board times the percentage of manual assembly required.
- L. Equipment costs are essentially either the lease rate or the capital equipment depreciation rate. In this example, it is assumed that the lease cost is \$22.50 per thousand dollars of equipment cost.
- M. Add all costs to determine the monthly assembly cost.
- N. Divide the total costs by the total boards produced to obtain the cost per board.
- O. Effective yield is determined by dividing the number of good boards produced on the first try (Formula C) by the number of boards that could be produced. To determine the latter, multiply the scheduled hours by machine speed in components per hour, and divide by the number of components per board.
- P. The Capital Content is the monthly equipment cost divided by the monthly assembly cost.

TABLE 4. A Strategic Net Yield Analysis

Inputs

1. Scheduled production hours	176
2. Operators required	1
3. Changeovers per month	20
4. Material cost per board	\$280
5. Labor cost per hour	\$50
6. Rework minutes per board	21
7. % of rework scrapped	1
8. Seconds per manual placement	40
9. Components per board	150
10. Components placed per hour	3,500
11. Reliability: hours down per month	2
12. Flexibility: minutes per changeover	10
13. Flexibility: % manual placement	1
14. First pass yield %	85
15. Equipment cost	\$175,000

Formulas

A. Net hours available	170.67
B. Total board production	3,982
C. less: good boards	3,385
D. Boards requiring rework	597
E. less: scrap	6
F. Total boards produced	3,976

Cost of assembly

G. Scrap	1,672.53
H. Labor assembly	8,800.00
I. rework	10,453.33
J. maintenance	100.00
K. manual	3,318.52
L. Lease — \$22.50/\$1k	<u>3,937.50</u>

Key measures

M. Monthly assembly cost	28,281.89
N. Assembly cost per board	\$7.11
O. Effective yield	0.82
P. Capital content	0.14

Capital Content. The Capital Content is the measure of the dollar content in monthly assembly costs. It represents the percentage of the total monthly dollars due to equipment costs. For two equally performing process lines, a higher ratio is calculated for more costly equipment.

Determining SMT Line Capacity

Table 5 is a capacity analysis spreadsheet based on a 6-inch by 8-inch board with 150 components. When board size and number of components per board are known, the line planner can evaluate relative process rates. While it may be difficult to predict actual performance in advance, it is reasonable to make certain assumptions.

For an initial approximation, the line should be balanced with the pick and place assembler operating at least 20% slower than the other units. This line balance approach simplifies simulation of the line, as it eliminates interactive bottlenecks. As mentioned previously, the assembler is significantly slower than the other units on the line, so the above assumption should not present a difficulty.

Second, using rough capacity requirements for the line, input the board-per-hour rating from the assembler as the production output. Based on the manufacturer's throughput rate, it is possible to estimate approximately how many assemblers will be necessary to meet the required production output.

Third, the assembler should be balanced so that board handling time (5-10 seconds of non-productive placement time) should be limited to 5% of the total cycle. Carefully weigh the number of machines required, cost, placement rate and transport time, then plug the data back into the strategic net yield numerical model. The cycle should be repeated iteratively until diminishing returns indicate a line layout.

CONCLUSIONS

A new assembly technology requires a new approach to equipment and process evaluation. Experience with through-hole assembly has fostered many misconceptions and misunderstandings regarding the surface mount assembly process.

Statistical process control is proving itself an effective method of maintaining high SMT quality standards. However, this approach may require changes in production and management orientation, particularly in regard to equipment acquisition and process implementation. Such strategic factors as equipment flexibility, accuracy, reliability as well as speed and cost must be considered when the pick and place assembler, a critical unit, is being evaluated. This can be done through the use of a Strategic Net Yield model, which results in four key measures that can be used for comparison of varying scenarios. A surface-mount capacity planning worksheet can be used to determine the number of assemblers necessary to meet production projections.

While the equations above can help evaluate pick and place assemblers, no standard formulas exist for designing a surface mount assembly line. All introductory seminars speak broadly of the basic methods for choosing surface mount equipment and processes,

but each application and each environment is different. In all probability, a certain amount of customization will be necessary to achieve optimal performance. In addition to the relative importance of all the SNY factors discussed above, individual methods of process control, material quality control, inventory control, maintenance, production management, investment strategy and technical expertise all must be considered in the line development strategy.

TABLE 5. SMT Line Capacity Planning

Board width 6"
Board length 8"
Number of components 150

Screen Printer			Sec/bd	Bd/min	Bd/hr	
			10	6.00	360	
			15	4.00	240	
			20	3.00	180	
			25	2.40	144	
			30	2.00	120	
			35	1.71	103	
		40	1.50	90		
Pick and Place	Comp/hr	Min/bd	Sec/bd	Bd/min	Bd/hr	
	1500	6.00	360	0.17	10.00	
	2000	4.50	270	0.22	13.33	
	2500	3.60	216	0.28	16.67	
	3000	3.00	180	0.33	20.00	
	3500	2.56	154	0.39	23.33	
	5000	1.80	108	0.56	33.33	
	10000	0.90	54	1.11	66.67	
	13500	0.67	40	1.50	90.00	
Reflow	Inch/min	Ft/min	Min/bd	Sec/bd	Bd/min	Bd/hr
	10	0.83	1.60	96.00	0.63	38
	15	1.25	1.07	64.00	0.94	56
	20	1.67	0.80	48.00	1.25	75
	25	2.08	0.64	38.40	1.56	94
	30	2.50	0.53	32.00	1.88	113
	35	2.92	0.46	27.43	2.19	131
	40	3.33	0.40	24.00	2.50	150
	45	3.75	0.36	21.33	2.81	169

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**SURFACE MOUNT ASSEMBLY AT
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ABSTRACT

Recent product developments by GTE-CSD, a prime contractor of Military Communication Systems, has required the use of many leaded and leadless surface mount devices (SMD's). These SMD's are used to achieve overall system performance within size, weight and power constraints. The assembly of these components on dense printed circuit boards requires an automated Surface Mount Technology assembly process.

GTE-CSD has been developing the design and manufacture of Surface Mount assemblies for several years. During this time several systems utilizing surface mount assemblies have been manufactured, tested and shipped to customers.

This paper is broken into two sections which describe:

- 1.) GTE-CSD's initial development and implementation of the SMT assembly process and;
- 2.) Actions taken, as a result of product evolution and experience gained, to optimize the design and manufacture of surface mount assemblies.

INTRODUCTION

There continues to be an increasing need for higher density of electronic circuitry in systems and smaller equipment for government and defense applications. This need has driven manufacturers of electronic systems to use Surface Mount Technology (SMT).

Surface Mount Technology may be generally defined as a method of electronic packaging and assembly. This implies that there are two constituents which go hand-in-hand. One is the electronic components themselves (e.g., chip resistors, chip capacitors, flatpacks, LCC's, PLCC's, etc.). The other is the process used to assemble these components to the circuit.

This paper discusses some of GTE-CSD's experiences in the initial development and implementation of the SMT assembly process, incremental enhancements as a result of product evolution and experience, and potential new processes and equipment to be used in the future.

DEVELOPMENT

During the development of SMT, there were two prime considerations. These were: 1) Design, and 2) Manufacture. Because one can never truly separate product and process, it is imperative that the design and manufacture of a surface mount assembly be thought of as a continuous function, rather than discrete tasks.

Design for Manufacturing

When considering the manufacturability or producibility of a surface mount assembly three factors come into play: 1.) Limitations in the production equipment, 2.) Component and Substrate Selection, and 3.) footprint layout.

Limitations of the Production Equipment. It is important for designers to consider the inherent limitations in today's production equipment. These considerations range from the obvious (e.g., size constraints) to precision and accuracy of printers and placement machines.

Printed wiring boards can be designed and densely populated with a spacing of .015 inches between components. However, the tight spacing requirements between components can adversely affect screen printing. Poor printing can lead to solder bridges or shorts. When designing a PWB the inherent accuracy and precision of placement equipment must be considered. For example, many of today's pick and place machines cannot accurately and precisely place flatpacks with .025 inch centers. In many cases poor production yields may be avoided with carefully planned process capability studies. The results of these studies should be used as a guide to the designer or as an indicator to upgrade the production processes.

Component and Substrate Selection. Designers should be sensitive to the affects of the soldering and cleaning processes on the materials and components selected. In general, the materials and components should be able to withstand five vapor phase soldering cycles (419 degrees F for 45 seconds) and several solvent cleaning cycles without showing signs of component failure, and material failure such as delamination, hazing and marking retention problems.

Component solderability should also be considered. Passives (e.g., chip capacitors, chip resistors) should be specified with a barrier metal (usually nickel) separating the termination metal from the solder coat (see figure 1). Furthermore, if the passive components are to be tape-and-reeled for pick and place, the solderable coat should be plated rather than tin/lead dipped (the solder may form a "glob" on one end of the component and not fit into the pocket of the tape-and-reel). To further ensure solderability, gold plating should be dissolved from the leads/terminations of any components. This is done by pre-tinning the lead or termination. Failure to do so can lead to the

formation of Au-Pb and Au-Sn inter-metallic compounds resulting in brittle solder joints.

Finally, the issue of how to handle the thermal coefficient of expansion (TCE) mismatch problem arises. The three most common package styles are leadless chip carrier (LCC), J-leaded carrier and gull wing carrier (flatpack, cerquad). The style package that will ultimately prevail is not clear. Each offers unique advantages. Leadless chip carriers offer the greatest density (X, Y and Z) and thermal dissipation; however, standard glass/epoxy substrates must be constrained to meet rigid thermal cycling requirements.

J-lead carriers can be packaged to achieve the same density as LCC's (in fact, using the same foot prints); however, thermal dissipation through the board is more difficult due to the larger gap beneath the component body. Higher component height also means greater card or module pitch lowering overall volumetric efficiency.

Gull wing packages enhance thermal dissipation and their lower profile reduces card pitch; but real estate is increased accordingly. Figure 2 shows a comparison of the three package styles with respect to several manufacturing parameters.

Surface Mount Assembly Process

The surface mount assembly process involves solder paste deposition, board population, pre-bake, reflow, cleaning and inspection. The various assembly processes may be characterized as follows:

- o Type I: SMC's only
Single or double sided assembly of SMC's
- o Type II: Mixed Technology
Single sided assembly of all types of SMC's and through hole components
- o Type III: Mixed Technology with under-side attachment
Double sided assembly with small SMC's (chip caps, resistors) mounted on the un

derside of conventional through-hole assemblies or Type II assemblies.

These process flows are depicted in figure 3.

Solder paste selection and the SMT operations are described in the following paragraphs.

Solder Paste. Solder pastes are composed of a solder alloy suspended in a flux binder. The alloy and flux used in the SMT process are very similar to those used in through-hole assembly processes. However, a major difference does exist in the purpose of the solder. In SMT assembly the solder joint is acting as an electrical and mechanical connection, whereas in through-hole assembly the solder joint is acting solely as an electrical connection. For this reason it is important that a high quality solder paste be used.

Several factors effect the overall usability of solder paste. These include:

- o Viscosity

The viscosity of a solder paste is measured and recorded daily. The viscosity is measured using a Brookfield RVTD viscometer with a helipath stand and a TF spindle at a speed of 5 RPM. Solder paste viscosity is controlled between 400,000-600,000 cps for successful stencil printing. Experimentation has shown that viscosity tends to increase with exposure time (due to solvent evaporation). The effect of temperature on viscosity is very dramatic. Tests show a decrease in viscosity of 12,000-15,000 cps/degrees F. This can lead to solder slumping if not controlled. Control is attained by assembling in a temperature controlled environment.

- o Metal Purity

When a Sn/Pb solder paste is manufactured certain trace elemental impurities may be formed. The impurities, if in sufficient quantities, can cause solderability problems. These quantities are shown in Table 1 (from Fed. Spec. QQ-S-571E). Some examples of solderability problems caused by impurities include solder grittiness caused by

excessive copper and iron, poor wetting and grittiness caused by oxide promoting elements such as aluminum, zinc and cadmium, and poor wetting from elements such as bismuth and arsenic. A qualitative trace element analysis of the metal should be performed by atomic absorption spectroscopy.

o Oxide Content

Several elements from Table 1 have been shown to promote oxide on the Sn/Pb metal particles. Solder paste also oxidizes when it is exposed to air. Excessive oxide content tends to inhibit solder coalescence during reflow which results in the formation of solder balls and poor wetting. During reflow, oxides are removed (by reduction processes) from the metal surfaces by the flux in the solder paste. The greater the oxide content the more active the flux needs to be. However, using higher activated fluxes can create cleaning problems in later stages of the SMT process. Therefore, the paste is monitored (using a solder ball test) for oxide content rather than trying to compensate with highly activated fluxes.

The "solder ball test" is a simple test, but gives an accurate representation of a paste's usability. A fixed amount of paste is screened onto a non-wettable surface and reflowed in a bell jar. A good paste will coalesce into a single solder ball with a minimal flux spread. An oxidized paste will exhibit many solder balls and a large flux spread which, during reflow of an assembly, can cause opens, bridges and components to "pop" off the pads. An oxidized solder paste should be discarded immediately.

It should be noted that problems with solder balls and solder wetting are not always due to a poor quality paste. Process variables including print quality, component placement and heating rates will also affect solder ball formation. However, when the problem is with the paste, oxidation is usually the problem.

- o Particle Shape and Size

The shape and size of the metal particles used in the solder paste can affect the solderability of the paste. Large, spherical particles tend to minimize the surface area of the metal, less surface areas means less chance of oxidation. It has also been our experience that large, spherically shaped metal particles tend to produce the best reflow results due to the decreased halo effect commonly found when using a paste with many smaller, irregularly (tear-drop, rod) shaped particles (called "fines").

- o Flux Activity

Thus far we have concentrated on the metal particles in the solder paste. The flux in the solder paste plays a critical role in chemically cleaning the metallized surfaces to promote even wetting and reliable solder joints. The flux also protects, to a certain extent, the metal particles from oxidation.

The flux system used in solder pastes vary in strength and activity. However, for military applications an R or RMA flux version is used. This flux system consists of solids (water white rosin), solvents (non-chlorinated), activators and other materials (wetting agents, stabilizers, viscosity modifiers).

Per QQ-S-571E, the flux is evaluated for composition and corrosiveness. The flux is extracted with isopropyl alcohol followed by resistivity tests, chloride and bromide tests and the copper mirror test. The resistivity test provides a measure of the ionic activity of the flux system. The chloride and bromide tests indicate the presence of these two ions; and the copper mirror test indicates the corrosiveness of the flux system at room temperature on bare copper. However, because most boards are pre-tinned results of the copper mirror test are limited in their usefulness. These flux tests are done on a lot sampling basis.

These parameters, along with other user specific functional parameters (e.g., ability to be

dot dispensed, screen printability, tack time, etc.), should be evaluated when qualifying a solder paste. Furthermore, these parameters should be monitored and controlled with some regularity to maintain high production yields.

Printing. Screen or stencil printing involves depositing solder paste onto the foot prints of the PWB. This is accomplished using a stencil (or mesh silkscreen in some cases) and a printer. Basically, two factors determine the quality of solder paste deposition. These are print registration and deposition thickness. Print registration is primarily a function of aligning the apertures of the stencil to the pads of the printed circuit board. Alignment is easier with a stencil because of it's "cookie-cut" nature.

Stencils are fabricated from the PWB artwork (pads only) and are visually and mechanically checked at incoming inspection. Aside from obvious registration and aperture (1:1 with pad) requirements, the stencil thickness and presence of a double sided chemical etch are verified. These latter two are quite important in determining the total volume of wet solder paste that will be deposited on the footprints of the board. Stencil thickness is measured using a micrometer. For our assemblies a thickness of 0.008" +/- 0.0005" yields optimum solder joint configuration. The thickness of the solder paste deposition will vary depending on the pad layout, pad sizes and types of components used. A double sided chemical etch as opposed to a single sided chemical etch is shown in figure4.

Along with the quality of the stencil (or screen), other parameters in the printing process must be controlled with respect to one another. These include:

- o Squeegee down pressure - enough to wipe the stencil clean.
- o Squeegee hardness - 80 durometer
- o Print Speed - Decrease viscosity during travel
- o Print Edge - 45 degree angle

Each of these parameters, if not controlled, can alter the height of the solder paste deposition. For example, if an excessive squeegee down pressure is used with a soft squeegee, the squeegee tends to take the shape of the stencil aperture during the print and "scoop" the solder paste off the pad, thus leaving a void on the footprint.

Pick and Place. There are two methods of programming a pick and place machine:
1) manual programming with a teach pendant and 2) downloading information directly from a design data base.

As one would expect manual programming via a teach pendant presents some major concerns not encountered with automatic programming.

Because manual programming is a labor intensive and repetitive task, it tends to be time consuming and inaccurate. Manual programming also provides limited editing capabilities. And finally, the pick and place machine is unavailable for production while the program is being generated. For these reasons we have elected to automatically generate pattern programs, operating instructions, and set-up instructions by a communications link between the Design data base and pick and place via a personal computer.

Aside from extracting component location information from the data base, placement parameters are also programmed and monitored. These parameters include placement pressure, pick-up tool selection, feeder type and location and tweezer centering mode.

Finally, one must also consider the types of components, size of components, and packaging configuration (e.g., tape and reel, bulk, etc.) of the components to be presented to the pick and place machine. The pick and place machine must be flexible enough (or fast enough) to meet the user's needs.

Pre-Bake. Once the board is populated, the assembly is pre-baked in a convection oven at 150

degrees F for 20 minutes. This evaporates the volatile solvents in the solder paste, thus minimizing the chance of solder balls due to "micro-eruptions".

This drying of the solder paste also facilitates board handling. After the pick and place operation the component is held in place only by the tackiness of the wet solder paste. The force required to move the component is minimal. After pre-bake, however, the force needed to move a component is significantly increased.

Vapor Phase Soldering. Vapor phase or condensation soldering is one of the many methods of reflowing surface mount assemblies. The in-line vapor phase soldering system consists of a closed stainless steel vapor chamber with long, narrow throats extending from each side. Heater elements, located at the bottom of the chamber, heat the "Fluorinert" fluid in the sump to a boil (419 degrees F). This produces a saturated vapor having the same temperature as that of the boiling liquid. As the cool board passes through the chamber, the vapor condenses and transfers its latent heat of vaporization, thus providing the means of reflow.

Some of the critical process parameters which may be controlled include:

- o Conveyor speed
- o Inlet/outlet temperature
- o Vapor/liquid temperature
- o Power consumed by heating elements
- o Ventilation

These are machine countrollable parameters which affect solder joint quality, machine maintenance and safety.

The vapor phase soldering process has been used successfully on surface mount assemblies with several types of leadless and leaded components (0.040" pitch). However, it should be recognized that each of the previous operations and the board design will affect the final quality of the assembly. For example, the pad sizes and layouts must be configured for automated surface mount

assembly (e.g., plated through holes should not be in the component mounting pad, they should be "necked down" per Figure 5). Bent leads or lead that are not coplanar to ± 0.0002 " can cause opens. Assembly operations such as the quality of the print, component placement accuracy, and pre-bake will affect the quality of the final product.

Cleaning. Cleaning surface mount assemblies or any other electronic assembly is a critical process step. Flux residues or ionic contamination left on printed circuit boards can lead to manufacturing and long term reliability problems by causing mealing in conformal coat, corrosion of the substrate material, and electrical degradation. Because of the increased density of electronic component and decreased clearances between the component and substrate (for LCC's, typically 3-4 mils), successful cleaning of surface mount assemblies is difficult at best. It has been our experience that turbulence or agitation for varying periods of time in the boiling and distillate sumps is the most effective way of cleaning SMA's. Maintenance and control of the cleaning process is concentrated in two areas: 1.) equipment control and 2.) Maintaining the integrity of the solvent.

Experiments conducted at GTE show that verifying cleanliness of assemblies with LCC's continues to be a difficult task. Traditional techniques such as the omegameter or ionograph tend to yield beta errors (i.e., the omegameter indicates the assembly is clean, however, when a component is removed flux residue remains). Other methods, such as surface insulation resistance measurements, are difficult to use in production. The need to verify cleanliness in real time, continues to be a concern which will require further development.

IMPLEMENTATION

Training

After developing design criteria and the SMT process via experimentation, and the assembly of thousands of test boards, the production process had to be implemented into GTE's manufacturing mainstream. This required the integration of all functions within the Operations Organization. A true team effort is required from manufacturing, production control, purchasing, cost control, and manufacturing and design engineering. This team effort must be supported by management who will provide the resources for training and the tolerance while the organization comes down the experience curve.

Communication is critical when trying to transfer a technology from a development phase to production. This seems implicit, but in a large organization it is often easier said than done. It is essential that all functions know their role in the implementation of SMT. They should also be well aware of the operating differences between SMT and through-hole technology.

To facilitate technology transfer, two technicians from the Manufacturing floor were made part of the development team. This afforded them the opportunity to actually be involved in the "hands-on" development of the process, hence providing that feeling of "ownership" to those that would actually be the critical bridge in transferring and sustaining the technology. The manufacturing technicians were primarily responsible for training the production operators, trouble-shooting day to day problems, and equipment maintenance and repair. It should be emphasized that training and education be an on-going, continual process.

Action could not stop at production personnel. A project engineer was responsible for integrating and coordinating many of the other involved functions. Some examples include:

- o Manufacturability/producibility (pad design, component selection, material selection) is critical. Poor pad layout can lead to skewing, tombstoning and a host of other problems. Improper specification of components can lead to solderability or coplanarity problems. Manufacturing engineering must be "in bed" with design engineering.
- o Production control and purchasing must ensure that passive components are purchased in a tape and reel packaging configuration.
- o When kitting material for the floor, stockroom personnel should not cut the reels (for example, cutting 10 chip caps off a reel for a board).

The examples are numerous and in many cases user specific.

Other Applications

Product evolution and the changing technology have necessitated certain incremental innovations to the surface mount assembly process. To meet these needs a machine to dispense dots of solder paste and a portable, in-house configured vision system are now part of the process.

The dot placement machine uses a positive displacement force to dispense dots of solder paste (Note; a new solder paste had to be qualified for the dispensing application -smaller particle size & lower viscosity). The dot placement machine is used on modules (e.g., SEM's modules) where the circuit cards are pre-bonded to a frame. This makes stencil printing impossible. Another application for the dot placement machine has been cards with sockets inserted. The sockets had to be soldered to the backside of the board. Tight spacing and heavy groundplanes made wave soldering impossible.

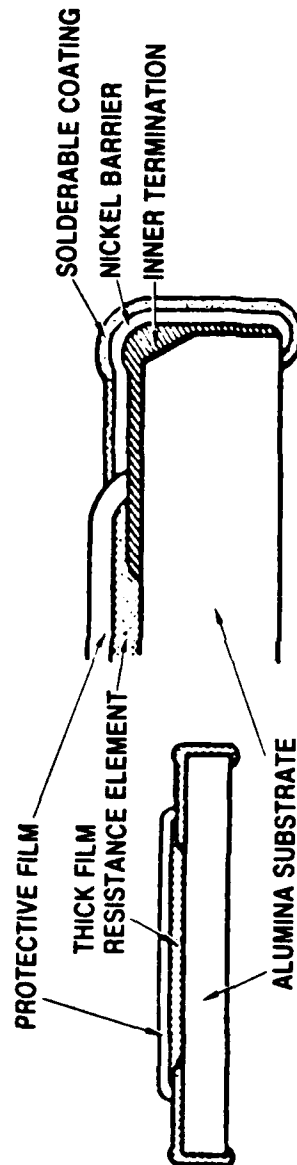
To solder these cards, solder paste was dispensed onto the tip of the sockets. The cards were pre-baked and vapor phase reflowed. A marked improvement in quality resulted.

As the densities increased visual inspection for missing components, wrong components, components in the wrong place, etc., becomes quite difficult. An in-house configured vision system has been put in place to provide a real-time "inspection". Boards are "inspected" after the pick and place operation and prior to reflow. This eliminates costly rework (due to placement errors) after reflow. Furthermore, the vision system acts as a process control tool. Data on missing components, misplaced components, and wrong components may be fed back to the operator, who can then take action to solve the problem.

SMT is still a relatively new technology. Many improvements have been made, and many more will be made. Future processes and equipment will have to be developed to reflect user's and customer's needs, as well as the ever changing technology.

Passive Components

- Chip resistors



- Chip capacitors

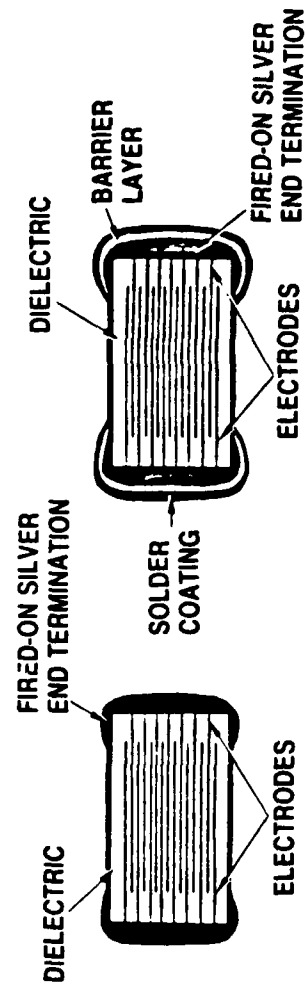


FIGURE 1 COMPONENT CONSTRUCTION

PACKAGE COMPARISON

	J- LEADS	GULL WINGS	LCC
COMPLIANCY	CONCERN DURING MFG (PASTE IN CURVE)	NOT AN ISSUE	VERY POOR
COMPONENT PREP	PURCHASE FROM SUPPLIER	COMPONENT PREP. REQUIRED	PRE-TIN
REAL ESTATE	LESS SPACE REQ'D	MORE SPACE REQ'D	SAME AS J- LEAD
HANDLING	COPLANARITY A CONCERN. DIFFICLT TO REFORM LEADS	COPLANARITY A GREATER CONCERN. LESS DIFFICULT TO REFORM LEAD	NO CONCERN
FEEDING FROM PNP	VIBRATORY/SLOPE FEEDRS- NO PROBLM	NEW FEEDERS WOULD BE REQUIRED	VIBRATORY/ SLOPE FEEDRS- NO PROBLM
CLEANING	GOOD CLEANABILITY	CLEANING A BIT MORE DIFFICULT (EASIER THAN LCC'S)	VERY POOR
INSPECTION/ TOUCH-UP	DIFFICLT TO INSPCT AND TOUCH-UP	EASY TO INSPCT AND TOUCH-UP	VERY DIFFICULT
DESIGN RULES	SAME AS LCC'S	NEW PAD DESIGN RULES NECESSARY	KNOWN
PNP	EASY TO CENTER ON PNP TOOL HEAD	DIFFICULT TO CENTER ON PNP TOOL HEAD	NO CONCERN
VPS - VOIDS	VOIDS/ OPENS DUE TO EXCESSIVE WICKING DURING VPS	NO KNOWN VOIDING PROBLM DURING VPS	PREVALENT
VPS - SELF- CENTERING	WON'T SELF-CENTER DURING VPS	WON'T SELF-CENTER DURING VPS	SELF- CENTERS
THERMAL DISSAPTN	NOT GOOD	GOOD	GOOD

FIGURE 2 PACKAGE COMPARISON

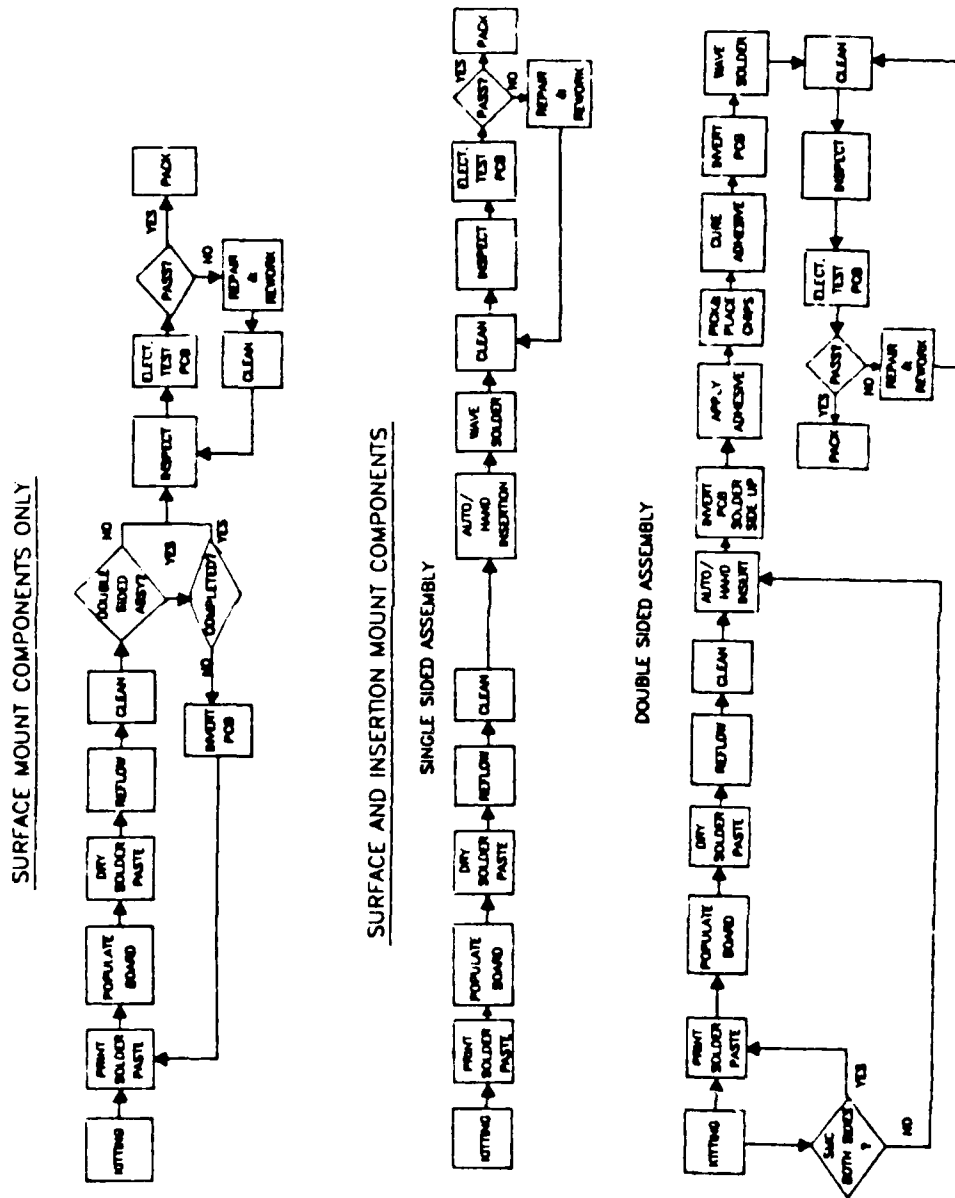


FIGURE 3 PROCESS FLOWS

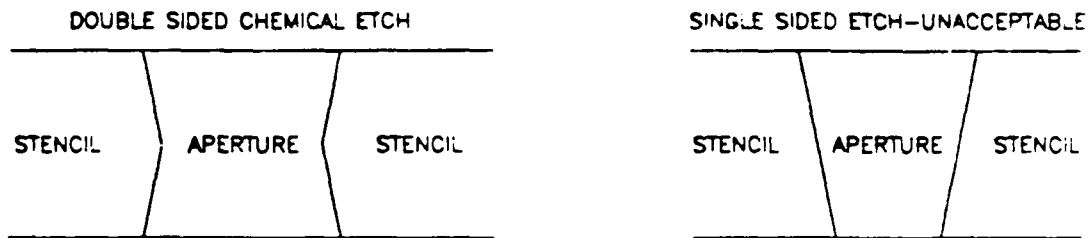


FIGURE 4 DOUBLE VS. SINGLE SIDED ETCH

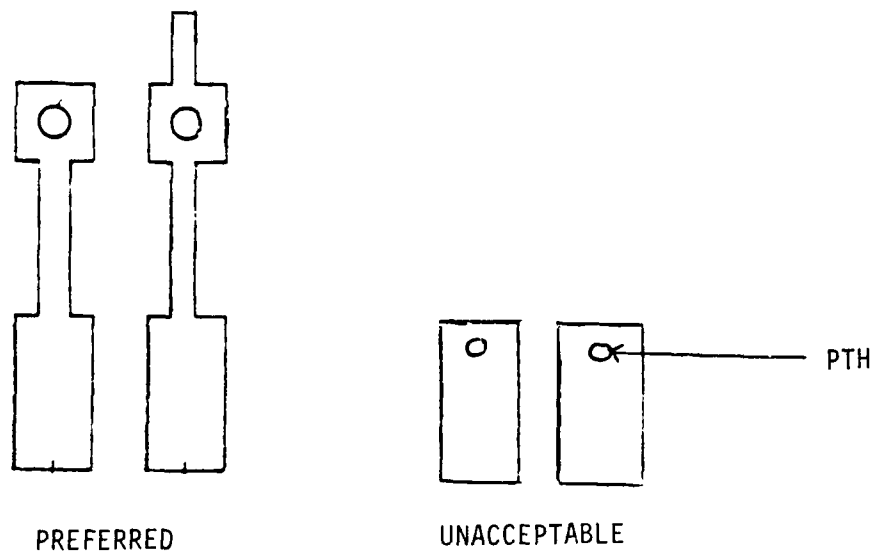


FIGURE 5 NECK DOWN PAD

Elements	Symbol	Percent of Total
Tin	Sn	62.5 to 63.5
Antimony	Sb	0.30 to 0.40
Bismuth	Bi	0.05
Aluminum	Al	0.002
Arsenic	As	0.01
Cadmium	Cd	0.001
Copper	Cu	0.04
Gold	Au	0.01
Iron	Fe	0.01
Phosphorus	P	0.01
Silver	Ag	0.01
Sulphur	S	0.005
Zinc	Zn	0.001
Lead	Pb	Remainder
Nickel	Ni	0.002
Total of All Others		0.05

TABLE 1. Trace Elemental Impurities

NWC TP 6896
EMPF TP 0003

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LESSONS LEARNED DURING A YEAR OF PRODUCTION SOLDERABILITY TESTING WITH A WETTING BALANCE

by

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ABSTRACT

The paper is divided into three sections. In section one the design and operation of a wetting balance is described. In section two lessons learned during the transition of the balance to a production environment are discussed. These lessons bear on the reliability and repeatability of the test results. A comparison of test results from the wetting balance and the dip and look test is presented. In section three changes to the test method specification and the assembly specification are suggested, to make the test method better reflect the mass soldering process requirements and allow the test method to be more widely used.

INTRODUCTION

In October of 1986, Collins Defense Communications (CDC) began using a computer integrated wetting balance for solderability testing at receiving inspection. The use of the balance was approved on a limited basis (which will be described later) for one production program.

This paper will describe briefly the system that was designed and built, and the test results to date, before getting into the two main sections of the paper. First several lessons which were learned with regard to obtaining consistent and reliable test results from the balance will be discussed. Second, several suggestions for changes in the assembly specifications (WS-6536 and DOD 2000) to allow use of the wetting balance, and in the test method specification (MIL-STD-883 Method 2022) to make the test more meaningful, will be described.

BACKGROUND

The first question which must be answered is, "Why bother with the wetting balance in the first place?" The equipment is more expensive than the simple solder pot required for the MIL-STD-202, Method 208 (dip and look) test, and the test method is not currently called out as an

alternative solderability test in the applicable assembly specifications (WS 6536 and DOD 2000).

ADVANTAGES OF THE WETTING BALANCE TEST

The answer is that the wetting balance, when integrated with a microcomputer, has several major advantages over the dip and look test. The first advantage is in speed of testing. The dip and look test requires that, after dipping in molten solder, a one inch length of each lead be examined at 10x. The inspector must then judge whether or not the defects found on the lead cover more than 5% of the surface. With the wetting balance the evaluation of the test data, and the pass/fail decision can be automated and can be done in a fraction of a second. The second major advantage deals with consistency of test results. It is difficult for an inspector to maintain consistency in evaluating the lead coverage over long periods of time. The wetting balance pass/fail decision is based on numeric values which make consistent evaluation so simple that it can be done by a machine.

Another advantage of the wetting balance test is that it is a dynamic test which gives information about the entire wetting process rather than just showing what the state of wetting is after five seconds. Thus, it is a much better reflection of the actual mass soldering process than is the dip and look test. Also, the wetting balance data, when stored in a microcomputer, is easily available as input to a statistical vendor quality system which, in the long term, can be used to weed out, or assist, vendors with chronic solderability problems.

SYSTEM DESCRIPTION

A brief description of the wetting balance system design and operation is presented in this and the following section. For those interested in a more detailed description of the system an information packet is available from the author. The packet includes hardware specifications for all system components, full operating procedure, blueprint of the interface, operation flowchart, operating program on a 5 1/4" diskette, and a full listing of the program. The information is not designed to give one a pat answer to implementing a wetting balance, but rather to suggest a method and give what the author feels is the right direction to head in implementing the system.

The wetting balance system designed and built at CDC was comprised of the following major physical components.

1. GEC Mark 6 Meniscograph
2. IBM PC-XT
3. Tecmar Labmaster I/O board for PC
4. Interface (designed and built in-house)

The reasons for integrating a computer in the wetting balance were to get consistent, fast pass/fail decisions, automate the data collection and analysis process, allow the setup parameters for all components tested to be stored on-line, and to assist in statistical analysis of the test data collected over long periods of time. The computer reads the following signals from the Meniscograph control unit.

1. Temperature of solder pot
2. Switch close/open to indicate start/end of test cycle
3. Vertical force on component (LVDT output scaled to 10 mv/mn)

A brief description of the basic operation of the system follows: it is similar to that described in references 1 and 2. The part identifier and lot identifier are entered at the keyboard and the set up parameters (speed, depth, and dwell) are displayed on the CRT. When the setup is complete and the solder pot temperature is checked, the operator presses the start button on the control console to run the first test. When the test is complete, the force vs. time trace is displayed on the CRT along with the measured values for the pass fail parameters and a pass or fail message for the sample. When all the samples for a given lot have been tested, a one line summary for the lot is printed and the system is ready to be set up for the next lot.

Figure 1 is an example of what would be displayed on the CRT after a test. The screen can be hard copied if there is a reason to examine any particular trace in more detail. The data from each test, including the entire force vs. time trace, is stored on a diskette so it can be re-examined, if necessary, at a later date.

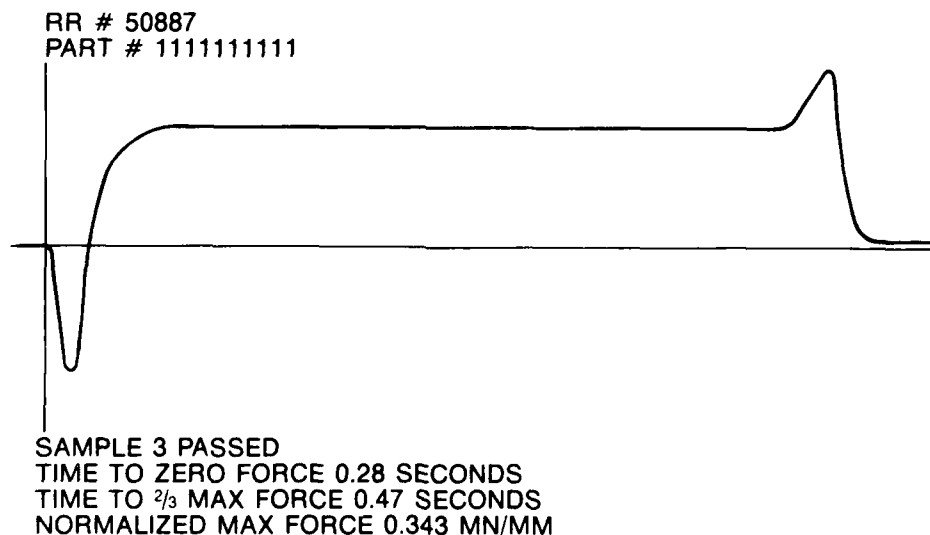


FIGURE 1. Typical computer output of wetting balance trace. Lot number, part number, and critical force and time values are displayed along with trace.

TEST RESULTS TO DATE

The use of the wetting balance was implemented on a deviation basis with the understanding that it would be used for acceptance of solderability, but would not be used to reject parts. Under the current wording of the applicable specifications, rejection can only be made when the parts fail to conform to the requirements of MIL-STD-202, Method 208. Therefore, all lots which passed the wetting balance test were accepted and inducted into stock. Those that failed were retested with the dip and look test, and those that failed the dip and look were rejected. Those that passed the dip and look were accepted and inducted into stock. This is admittedly not the ideal situation but in order to get some production experience with the wetting balance these conditions were considered to be acceptable on a temporary basis. The ultimate goal was to replace the dip and look test entirely with the wetting balance for both accepting and rejecting parts. It now appears that reaching this goal will be a little more complex than anticipated.

For the first six months of operation the lot reject rate from the wetting balance was consistently in the 50 to 60% range. For the same time period the dip and look reject rate for lots which had already failed the wetting balance was about 5%. The reject rate for parts which could not be tested on the wetting balance and thus received dip and look testing only was also about 5%. This indicates that the original premise (i.e. that the wetting balance test is more difficult to pass than the dip and look test) was correct. In fact, it appears that the wetting balance test is even more stringent than was originally thought.

A recheck of the reject rates six months later (October 1987) showed the reject rate from the wetting balance to have dropped significantly, to the 40 to 50% range. The dip and look reject rate appeared to have dropped slightly to about 4% but this may have been an aberration due to the much smaller sample size in the recheck.

The drop in rejects from the wetting balance is attributed to the fact that during the same time period CDC procurement practice was changing. The change involved an aggressive posture toward procuring parts which had been hot solder dipped by the vendor.

TEST RELIABILITY AND REPEATABILITY ISSUES

The following sections describe problems that were encountered during the day-to-day operation of the wetting balance in a shop floor environment, and suggestions for solutions to the problems.

ENVIRONMENTAL FACTORS

It was discovered upon moving the system from a lab environment to the factory that the electrical "noise" on the power line would intermittently cause the balance to start or stop a test cycle without being told to do so. Figure 2 is a trace of a test which was prematurely started by a voltage spike on the power line. This problem is solved by putting an isolation transformer in the line ahead of the wetting balance. Also, both the computer and the meniscograph must take their power from the isolator and must have a common ground.

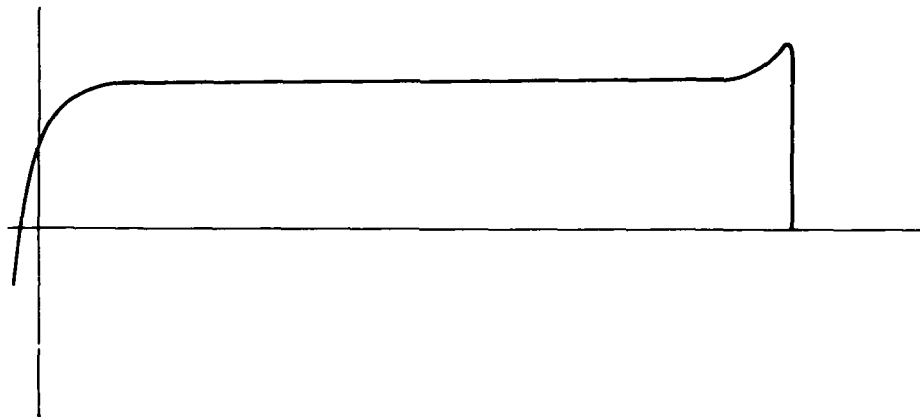


FIGURE 2. Test cycle which was triggered early by voltage spike on power line. Trace is shifted to the left and initial part of trace was lost.

Low frequency vibration can cause false pass/fail decisions. The force sensor on the meniscograph is sensitive enough to react to vibration caused by a passing forklift truck, or to plant equipment such as air compressors starting or stopping. Figure 3 shows the effect of vibration on the force/time trace. This, too, was a problem caused by the change from a lab to a factory environment. The solution is a vibration isolation table on which the test head is mounted.

TEST PROCEDURE

Several items in the test procedure are critical to obtaining consistent results. The first item is that in order to know whether results are consistent over a period of weeks, months, or years, it is necessary to establish some kind of a daily calibration procedure. The procedure established at CDC is to test ten samples of a previously characterized and relatively stable type of bus wire each day before production testing begins. If the test results do not fall within preset limits something in the system has changed and the change must be identified and fixed before production testing can begin. This procedure can also be used to ensure that test results from different machines are in agreement.

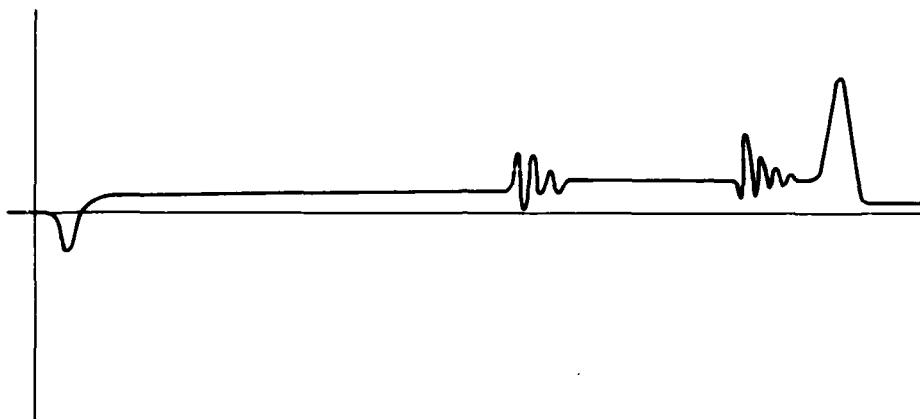


FIGURE 3. Trace showing the effect of vibration transmitted through the floor. Two vibration "events" are displayed.

Flux type is also critical to repeatability of test results. Of course, the flux must be rosin based, type R, per MIL-P-14256 but beyond this, solids content (References 3 and 4) and the type of solvent in the flux can affect the test results. The solids content affects the viscosity of the flux (i.e. how much remains on the lead) and how much oxide the flux will be able to remove. This is because the active component in the flux is the rosin and the solids content is a measure of how much rosin is present. The solvent used to formulate the flux affects how quickly the flux dries on the lead, and this has an indirect effect on how quickly wetting commences. We have determined that a type R flux with a solids content of 30 to 40% and an isopropyl alcohol solvent will give a consistent result. This type of flux is readily available.

Since the balance actually measures the apparent weight of the specimen it is important to get the same amount of flux on the component lead for each test. The lead must be dipped to approximately the same depth for each test and the drop of flux which normally adheres to the end of the lead when it is withdrawn from the flux must also be removed. The flux droplet will usually separate from the lead in the solder pot and go skating off over the surface of the molten solder. This causes the balance to read a decrease in the apparent weight of the specimen which is translated as a reduction in the wetting force. Figure 4 is an example of this phenomenon. The flux drop can be removed by touching the end of the fluxed lead to an absorbent surface (paper towel or cheesecloth) after removal from the flux.

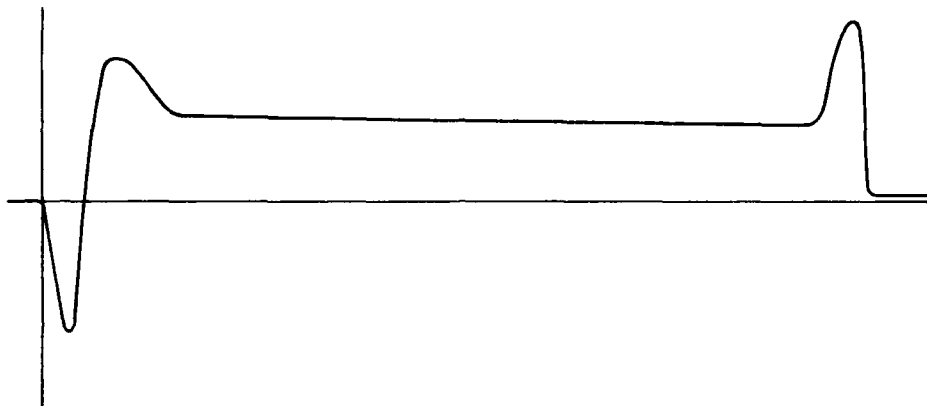


FIGURE 4. Drop in wetting force caused by flux droplet separating from lead and "skating" away on surface of molten solder.

The time between the application of the flux and the start of the test is also important: the dryness of the flux on the lead affects how fast wetting will commence. The IEC specification (Reference 5) for the wetting balance test recommends that, after fluxing, the part be hung on the fixture over the solder pot for 30 seconds to allow the flux coating to dry. This should give consistent results but will also have an adverse impact on throughput since the test cycle time is on the order of 15 seconds if the flux is not dried. The procedure used at CDC is to mount the component on the fixture first, then flux the lead, remove the adhering drop, place it on the balance hook, and commence the test as rapidly as possible. The typical delay between removal from the flux and contact with the molten solder is about 5 seconds.

One final note on the test procedure. The top of the pot should be cleaned with a skimmer just prior to each test. The material that the skimmer is made from must be stiff enough to push beneath the surface of the molten solder, so that it can push the dross to the side of the pot, and be stable enough at the test temperature that it will not contaminate the solder. Two good candidate materials are stainless steel and Teflon. We have found at various times such diverse materials as punch cards, paper towels, and pieces of PWB's being used as skimmers.

Another problem has been encountered which relates to the type of device being tested. The system signals the start of a test by sensing when the lead touches the molten solder. This requires electrical continuity from the holder through the component and the lead(s) being tested. The sensing circuit does not apply a large voltage to the component and will continue to work even at relatively high resistance levels. For situations where the resistance through the component is too high, an auxiliary probe is provided which must be set at the same height as the lead(s) being tested. We have discovered two types of components, tantalum capacitors and

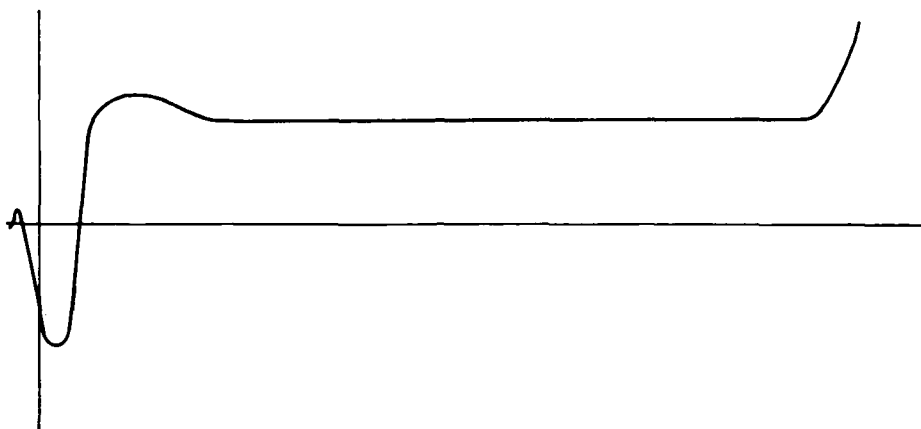


FIGURE 5. Test cycle in which contact of lead to pot was sensed by computer later than it actually occurred. Trace is shifted to the left.

resistor networks, which for unknown reasons cause the sensing circuit to sense contact with the solder pot after it actually occurs. Figure 5 is an example of this problem. The problem is intermittent and does not occur for all values of either component. This causes the computer to use the wrong data point as the starting point of the test for the pass/fail calculation, and can cause false passes. The solution is to isolate the part electrically from the holder and use the auxiliary contact probe. There may also be other component types which could cause this problem.

SPECIFICATION ISSUES

The specification issues will be discussed in the following sections. They are grouped by the specification that they apply to.

TEST METHOD SPECIFICATION (MIL-STD-883 Method 2022)

There are two situations in which parts that will not perform well in the mass soldering process will pass the test criteria in this specification. The first is shown in Figure 6. The maximum wetting force achieved by the component under test was barely above zero. There is a good possibility that there will not be an adequate fillet on this lead on the top side of the board after mass soldering. Therefore, a minimum normalized wetting force value at some specified time needs to be added to the specification. The second situation, which is shown in Figure 7, is one where a lead wetted in an acceptable fashion initially and then underwent severe dewet

during the latter part of the test. This can occur when a solderable material which is soluble in molten solder (such as silver or gold) is plated over a base metal which is not wettable. Therefore, a minimum force value at the end of the test period needs to be added to the specification.

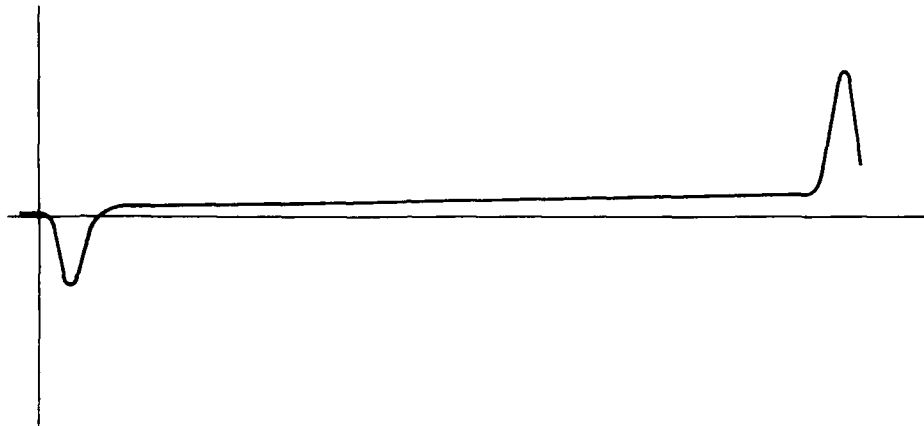


FIGURE 6. Trace of component which passed current specification requirements. Note extremely low wetting force.

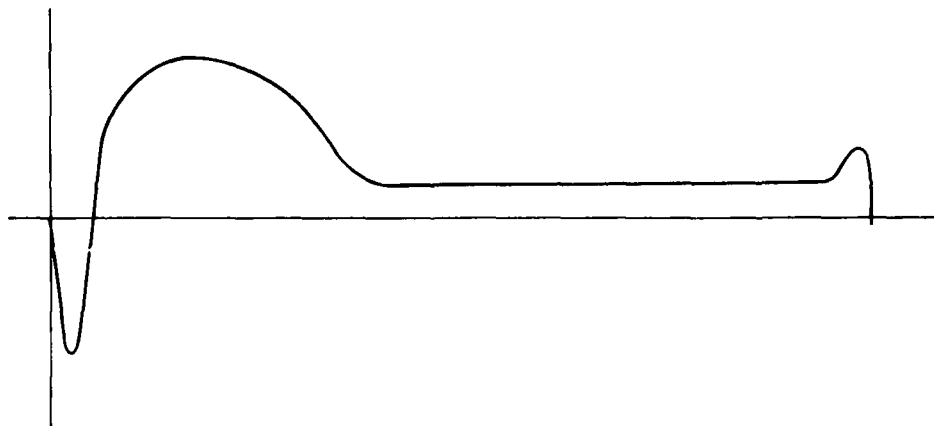


FIGURE 7. Force curve showing initial good wetting followed by dewetting as solderable plating was dissolved from lead exposing underlying unsolderable base metal.

Conversely there are times when a part which will perform adequately in the mass soldering process will fail the test criteria. The specification requirements need to be looked at in terms of what will actually happen to the components in the mass soldering process. The higher temperatures, both for the solder bath and the components themselves, used in the mass soldering process will increase the speed of wetting considerably (References 3 and 6). The more active fluxes used in mass soldering will magnify this effect even further. Therefore, the test requirements for wetting times do not necessarily need to fall within the realm of the minimum times used in the mass soldering process. The rejection rates which were described earlier as well as in References 2 and 7 indicate that the test criteria are far too stringent. Also, the requirement for time to reach 2/3 of maximum force is ambiguous and does not have a significant relationship to the mass soldering process.

RECOMMENDATIONS

The following recommendations are intended to make the test method better able to detect parts which will not solder adequately, as well as allow a greater percentage of parts which will perform well in mass soldering to pass the test. The changes will provide a pass/fail gate which is more representative of the mass soldering process than that contained in MIL-STD-202 Method 208.

1. Change the time to cross the zero force axis from 0.59 seconds maximum to 1.0 seconds maximum.
2. Remove the requirement for achieving 2/3 of maximum force in one second or less.
3. Add a requirement that the wetting force be a minimum of 200 millinewtons/mm at 2.5 seconds.
4. Add a requirement that the wetting force be a minimum of 200 millinewtons/mm at 4.5 seconds.

ASSEMBLY SPECIFICATIONS (WS 6536 and DOD 2000)

Currently this specification requires solderability testing by MIL-STD-202, Method 208. The experience gained with the wetting balance at CDC to date has been on a deviation basis. In order for other companies in the industry to start using the wetting balance it will be necessary for its use to be allowed by the assembly specification. The ultimate goal is to supplant the dip and look test completely with the wetting balance for reasons discussed previously.

RECOMMENDATIONS

1. Allow the use of MIL-STD-883 Method 2022 as an alternate to MIL-STD-202 Method 208.

This recommendation is considered to be a necessary interim step to allow the industry as a whole to gain production experience with the wetting balance.

SUMMARY

A year of production testing with the wetting balance has shown it to be a consistent, reliable tool for determining solderability of component leads. Test results have shown the pass/fail criteria of MIL-STD-883, Method 2022 (the wetting balance test) to be much more stringent than those of MIL-STD-202, Method 208 (the dip and look test). In fact, the criteria are more stringent than necessary to provide solderable parts and in some respects are not germane to the mass soldering process. These results are in concurrence with previous work (References 2 and 7). The changes outlined will make the specification better able to fail parts which will not solder adequately, as well as accept a greater percentage of parts which will solder adequately.

REFERENCES

1. J.A. DeVore *Wetting Balance Solderability Testing*, General Electric Co., Electronics Laboratory, Syracuse, New York.
2. J.G. Davy and R. Skold, "Computer Aided Solderability Testing for Receiving Inspection", IEPS Fourth Annual International Electronics Packaging Conference, 1984.
3. J.A. DeVore, "The Use of Wetting Balance Data to Predict Soldering Materials Performance and Soldering Process Parameters," Eleventh Annual Electronics Manufacturing Seminar Proceedings, Naval Weapons Center, China Lake, CA, 18-20 February 1987.
4. Private conversations
5. "Solderability Testing By the Wetting Balance Method," IEC 682-54, International Electro-technical Commission, 1985.
6. J.T. Bolton, *The Meniscograph as a Quality Control Tool — A Case Study in Solderability Testing*, Australian Tin Information Centre, 1982.
7. R.N. Wild "Some Component Lead Soldering Issues, Phase 2," Ninth Annual Soldering Technology Seminar, Naval Weapons Center, China Lake, CA, 19 February 1985.
8. "Wetting Balance Solderability," MIL-STD-883C Method 2022.2, 29 May 1987.
9. "Solderability Tests for Component Leads and Finishes," IPC-S805, Institute for Interconnecting and Packaging Electronic Circuits, January 1985.
10. "Solderability," MIL-STD-202F Method 208F, 11 April 1986.

11. I.A. Gunter, "Solderability Testing of State-Of-The-Art Electronic Components and Substrates," GEC Journal of Research, Vol. 4 No. 4, 1986.
12. B.M. Allen, "The Kinetics of Soldering," Welding and Metal Fabrication, January/February 1982.
13. D. Mackay, *The Meniscograph Method of Solderability Testing*, The General Electric Co. Ltd., Central Research Laboratories Hirst Research Centre, Wembley, England.
14. R.J. Klein Wassink, "Measurement of the Surface Tension of Molten Solder in the Presence of Some Rosin Fluxes," Brazing and Soldering, Spring 1987.

NWC TP 6896
EMPF TP 0003

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AUTOMATION AND CLEANING: A NEW OPPORTUNITY FOR SMT

by

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ABSTRACT

The use of surface mount technology (SMT) in US electronics is still relatively new. SMT presents many opportunities and also challenges. For high reliability surface mount assemblies (SMAs) cleaning is essential. One of the challenges in SMT is to make sure they are cleaned properly. Design factors such as component type(s), component standoff, pitch, density, etc. are certainly important since they determine what parameter settings must be used on the machine performing the cleaning. The chief equipment parameter of in-line cleaning defluxers for conventional, through-hole assemblies is, of course, the conveyor speed. In addition to conveyor speed, such equipment parameters as spray pressures, volume of solvent, the number and proximity of spray bars, and the impingement angle are important for cleaning SMAs, especially SMAs having tight standoff components such as leadless chip carriers (LCCs). State-of-the-art processing of SMAs must take into account these additional parameters to achieve effective cleaning.

In addition, the steady trend in US manufacturing towards computer integrated manufacturing (CIM) makes it desirable to have a cleaning process monitored and adjusted by computer control. Such a process can now be incorporated into a flexible manufacturing cell (FMC), an outcome which greatly benefits productivity and increased throughput. This paper describes experiments performed to define the process window for achieving surface mount cleanliness and the necessary analysis whereby an automated cleaning system capable of being incorporated into an FMC can be built. Indeed, it is already being built. In addition, various methods for testing for cleanliness are also discussed.

1. INTRODUCTION

The rapid growth of surface mount technology in the US electronics industry poses both new opportunities and also new challenges. The many opportunities of SMT have long been widely touted. Such advantages as increasing the functionality per board area, decreasing of the number of layers in a multilayer printed wiring board (PWB), and decreasing the signal path length are advantages that design engineers are now recognizing when they utilize SMT. And on the manufacturing side, SMT is generally more amenable to automated manufacturing techniques. Benefits for the packaging engineer accrue also, for SMT is probably the most viable way of packaging high pin count integrated circuits (ICs) as found in VLSICs and VHSICs.

Accompanying these benefits, however, are the challenges that SMT presents. Many of the manufacturing problems that SMT has brought into the manufacturing arena are now being dealt with satisfactorily. Manufacturing engineers in printed wiring assembly have had to master reflow soldering techniques such as vapor phase and infrared reflow, and they have had to learn to work with such new materials as reflow liquids and solder pastes. Another challenge that SMT presents centers on solder joint integrity and long-term reliability. Reliability issues are, of course, very important even with conventional printed wiring assemblies (PWAs), but SMT introduces new unknowns.

Companies using SMT normally make or expect to make a highly reliable product that is expected to have excellent performance characteristics over the life of the product. To achieve this end cleaning the soldered assemblies is a must.

Surface mount assemblies have associated with them several cleaning challenges not normally associated with PWAs having conventional through-hole components (THCs). Among these are:

- o Reduced standoff
- o Reduced pitch
- o Solder paste residue removal

- o Board geometry
- o Component density
- o Board configuration under the surface mount component (SMC).

Each of the above points has been developed in much more detail in a previous paper by the author.¹ It suffices to say at this point that each of these makes cleaning SMAs more difficult than PWAs with conventional THCs.

2. AUTOMATION

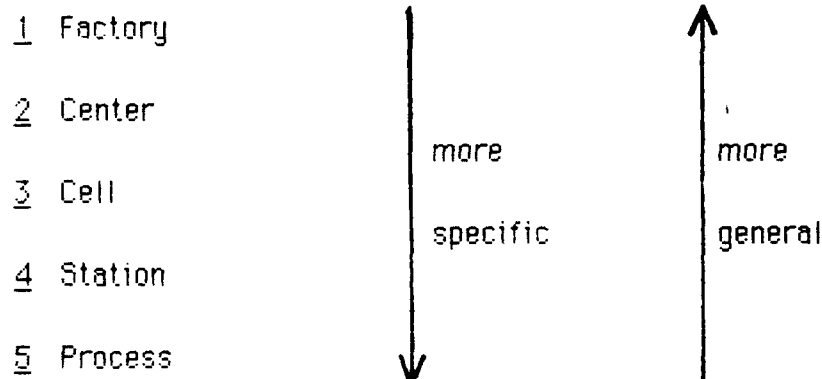
Both within and outside of the electronics industry, a new development has been taking place that is rapidly transforming manufacturing. This is the trend towards increasing automation. Such acronyms as CAD, CAM, and CIM have been widely bandied about, but the reality is there. The increasing introduction of computers on the manufacturing floor has been proceeding at a steady pace. This trend has been especially noticeable in the metal working industry; indeed, many pieces of routine machinery now incorporate a microprocessor or programmable logic controller (PLC) as an integral part of the machine. Such machines are being incorporated into groups of machines integrated around a central host computer. These groups of machines under computer control are sometimes referred to as flexible manufacturing cells. Such FMCs are receiving wide attention.²

Such a flexible manufacturing cell can be developed for SMT assembly operations. Indeed, the use of the computer to coordinate and control manufacturing operations had been foreseen several decades ago.^{3,4,5} The application of the computer to discrete parts manufacturing has led to the precise control of the various operations that a workpiece experiences during a given process and to the problem of workpiece storage and transportation between different work stations.

The computer is the central element of a data-processing system. Therefore, its usefulness lies in its manipulation of data involved at all levels of manufacturing. The most basic level involves the control of tools in executing their

function upon the material and the movement of the material
from one piece of machinery to another (emphasis mine).⁶

It is clear that manufacturing consists of several different levels. Using a terminology widely used for manufacturing, there are five distinct levels.⁷ These are:



That is, a given factory contains so many centers, each center contains so many cells, each cell so many stations, and each station performs a particular process. See Figure 1. By a process is meant the utilization of energy (chemical, mechanical, thermal, etc.) to transform the workpiece into a new, more desirable state. Economically speaking, a process performed on a workpiece increases its economic utility and hence its economic worth. The mere physical movement and/or orientation in space of the workpiece is an operation performed on the workpiece but is not a process because it does not increase its economic worth. Also, inspection of the workpiece is an operation but not a process since again there is no corresponding increase in economic worth. It is clear that a workpiece passing through a station may have several operations performed on it such as physical movement to the station and within the station, orientation, inspection, etc., but only one process is performed per work station. It must be moved to another station to be subjected to another process.

To determine how best to proceed with automation, a systems analysis approach is desirable. It is necessary to consider the station in which a given process takes place as the starting point of systems analysis. This analysis enables one to discern the necessary entities in a FMC regarding the workpiece flow. These are the entities:

- 1 Workpiece--the material unit upon which the process occurs, in this case an SMA.
- 2 Station intertransport mechanism--the means whereby the workpiece is transported to the station. In a fully automated system, this would be some sort of conveyor system or a robot.
- 3 Storage-in module--a buffer area in which workpieces can be stored temporarily prior to being checked into the station for processing.
- 4 Check-in mechanism--the means whereby the workpiece is verified as being at the proper station at the proper time, such as a bar code reader. Such a mechanism would communicate with the cell controller which would then download instructions to the station controller to adjust all necessary process parameters for that particular workpiece.
- 5 Station intratransport mechanism--the means whereby the workpiece is transported from the check-in point through the machine so that the process can take place on it. In many cases this will be some sort of conveyor system.
- 6 Station process mechanism(s)--the means whereby the machine acts upon the workpiece to perform the process upon it.
- 7 Check-out mechanism--the means whereby the workpiece is verified as having had the proper process conducted on it.
- 8 Storage-out module--a buffer area in which workpieces can be stored temporarily before being transported to the next station.

In addition, there must be a station controller and a cell controller. The station controller has control authority over all the machine parts required

to perform the process, that is, the process parameters are subject to the station controller and can be changed by direct order from the station controller. In addition, the station controller monitors the process in a real-time mode to ensure that the parameters are maintained within an acceptable range. It must also control the rate and flow of the workpieces through the machine proper. The station controller, then, is responsible for setting and maintaining entities 5 and 6--the station intratransport mechanism and the process mechanism(s). The other entities are normally under the control of the cell controller.

Those operations whereby the workpiece arrives at and departs from the station, buffer input and output zones for workpieces prior to and after processing, and the check-in and check-out mechanisms are under the jurisdiction of the cell controller. Indeed, the check-in mechanism must inform the cell controller that a particular workpiece is ready for machine processing. The cell controller must then inform the station controller what parameter values are to be used for the particular workpiece undergoing check-in. In addition, two-way communication must be effectuated between the station controller and the cell controller. Any report generation is done by the cell controller, and it must have access to all relevant information at the station level. In a working FMC, the cell controller is a computer powerful enough to control several stations. It is necessary now to consider the process window whereby SMAs can be cleaned and then to return to the concept of a cleaning machine under computer control.

3. PROCESS PARAMETERS FOR SMAs

To demonstrate convincingly that SMAs can be cleaned using a fluorocarbon solvent, a series of SMAs were cleaned and tested for cleanliness. The processing steps used were:

- o Apply solder paste (60/40 RMA paste screened on
using a 0.010" metal stencil)
- o Mount SMCs (LCCs)
- o Preheat (175°F for 30 min.)

- o Reflow (vapor phase reflow: 0.5 min. reflow/1.0 min. dwell)
- o Clean using fluorocarbon solvent in automated in-line defluxer
- o Check for cleanliness.

All SMAs used were processed on production equipment at Allied-Signal's Applications Laboratory.

The chief SMA design parameters affecting cleaning are:

- o Component standoff, d
- o Component pitch, p
- o Number of I/O terminations of component
(\approx component area), n
- o Board configuration under components
- o Component spacing (distance of components from each other), d'
- o Number of components populating the assembly, n' .

In addition to the design parameters of the SMA affecting cleaning, there are also a number of process parameters that are significant in the cleaning operation. These are:

- o Conveyor speed, S
- o Pressure at the nozzle orifice, P
- o Number of high-pressure nozzles, N

- o Distance of nozzle spray bars from each other in spray manifold, δ .
- o Solvent used
- o Volume of solvent, V
- o Impingement angle, α
- o Distance of substrate to nozzles, D .

The sole cleanliness criterion used initially was: no visible residues of any sort at 10x magnification after components were removed. However, because it is very difficult, if not impossible, to compare the cleanability of different pastes and also to compare different cleaning protocols using this criterion, more quantitative methods are being sought. One method that has been used to great advantage is high performance liquid chromatography (HPLC) and another is coulometry. The latter method is used to determine total carbon residue, but since the residues left on the SMA after cleaning are organic in nature, this method is acceptable for LCCs. A third method being explored is differential refractometry.

In Figure 2 is depicted a partially populated test board; Figure 3 shows a fully populated test assembly (SMA Type 1: all LCCs). The populated test assembly or one not quite fully populated was the one used in the work.

In the experiment conducted on the test assemblies (SMAs), the chief process parameters in the cleaning operation were:

- o Conveyor speed
- o Pressure
- o Number of high-pressure nozzles
- o Volume of solvent.

The design factors that impacted cleaning the most were:

- o Component standoff
- o Configuration under components.

The component pitch was not varied; however, it is highly likely it too would have a very important effect on cleanability.

For solder paste used in conjunction with LCCs, it proved very difficult to clean effectively if the total standoff was < 5 mils. However, if a standoff of $0.005''$ was achieved, cleaning was greatly improved. Test boards were run where the pressure was varied between 150-200 psi and the conveyor speed and the number of spray headers were varied. In some cases a visual criterion of cleanliness was used. In other cases the LCCs were desoldered and run in a coulometer to measure for total carbon residue. The boards (after desoldering) were checked for ionic contamination using the solvent extract resistivity test. In the case of the coulometer the results are reported in micrograms of carbon or equivalent per square inch ($\mu\text{gC}/\text{in}^2$) and also in terms of $\mu\text{gC}/\text{pad}$. The latter figure was arrived at by finding $\mu\text{gC}/\text{component}$ and dividing this figure by the number of pads per component. Ionic contamination is, of course, expressed in micrograms of sodium chloride or equivalent per square inch ($\mu\text{gNaCl}/\text{in}^2$). See Table 1.

Effective cleaning of SMAs is possible using a fluorocarbon solvent in conjunction with a high pressure spray system. Cleaning was significantly improved if:

- o The conveyor speed was equal to or less than 3 ft/min
- o The pressure on the spray headers was maintained
between 150 to 200 psi
- o The number of spray-headers was at least 8 in a given header
manifold and each header was approximately 3 inches apart

- o The volume of solvent was 20-25 gal/min
- o The component standoff was equal to or greater than 0.005"
- o The configuration under the components was kept simple.

4. FEATURES OF THE AUTOMATED CLEANING MACHINE

In Sections 2 and 3 automation and the process parameters for cleaning SMAs were discussed. In this section a defluxing machine incorporating features for both FMC automation and for effective cleaning of SMAs will be described. Based on the systems analysis performed in Section 2, such a machine will have the following: (1) a storage-in module, (2) a check-in mechanism, (3) a station intratransport mechanism, (4) station process mechanisms, and (5) a storage-out module. In addition, the defluxer has a machine controller, i.e., the station controller, and a subsystem controller, i.e., the cell controller.

The machine controller, the heart of the automated defluxer, controls a variety of functions in the machine. It interfaces with the subsystem controller through an RS-232 port; it also interfaces with the hardware of the cleaning machine, the storage-in module, and the storage-out module. When the subsystem controller receives a message from the check-in mechanism (a bar code reader) identifying the SMA type, the subsystem controller downloads the particular parameter settings needed to clean effectively that type of SMA to the machine controller. The latter, in turn, then gives orders to adjust all necessary machine hardware (the station process mechanisms) for cleaning the SMA. Among the process mechanisms adjusted by the machine controller are:

- o The presence of an SMA in the storage-in and storage-out modules
- o The temperatures of the machine sumps (6 in number)

- o The pump pressures which can vary between 20 to 200 psi in 10 psi increments
- o The impingement angles of the spray nozzles which are adjustable within the range of ± 45 degrees with respect to vertical in 15 degree increments
- o The conveyor speed which is adjustable in 0.1 ft/min increments within the range of 0 to 9.9 ft/min.

The machine itself has other noteworthy features. Its overall dimensions are 31 feet long by 6 feet wide plus space required for a control cabinet to be located separately. It has a total of six sumps. Two of these are liquid seal--one at the machine entrance and one at the machine exit. In addition, there are three recirculating sumps and a vapor generating sump. Each recirculating sump is serviced by two pumps--one to feed the top spray manifold and one to feed the bottom spray manifold. The defluxer has a workpiece counterflow design, which means the workpiece is exposed first to the most contaminated solvent and as it progresses through the machine, experiences ever cleaner solvent. The machine controller, as was pointed out above, controls the pressures of each sump. Each high pressure spray zone is separated by an 18 inch space allowing adjustment of the various parameters within the zone while the pallet with SMA is outside the zone. See Figure 4 for a depiction of the machine.

5. Summary

This new defluxer is designed, then, for integration into a flexible manufacturing cell. In addition, it also has pertinent machine features allowing it to clean effectively a wide variety of SMAs.

TABLE 1. Average Carbon Residue And Ionic Residue After Cleaning

Passes Under High Pressure Nozzle	* $\mu\text{gC}/\text{in}^2$	* $\mu\text{gC}/\text{pad}$	* $\mu\text{gNaCl}/\text{in}^2$
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100	23.6	0.25	1.2
50	92.8	0.98	1.2
25	235.9	2.48	2.4

Conditions: Paste Had No Standoff; Conveyor Speed 10 ft/min (Simulated)

100	17.8	0.19	0.8
50	17.6	0.19	1.9
25	24.8	0.26	1.3

Conditions: Paste Had 0.005" Standoff; Conveyor Speed 10 ft/min (Simulated)

100	25.0	0.26	2.1
50	31.4	0.33	2.0
25	46.7	0.37	2.0

Conditions: Paste Had 0.005" Standoff; Conveyor Speed 20 ft/min (Simulated)

REFERENCES

1. John K. (Kirk) Bonner, "Effective Cleaning of Surface Mount Assemblies," Proc. Expo SMT '87, Oct. (1987).
2. Robin P. Bergstrom, "FMS: The Drive Toward Cells," Mfg. Eng., Aug. (1985), 34-38. Also see Paul Kinnucan, "Flexible Systems Invade the Factory," High Tech., July (1983), 32-43.
3. See Norbert Wiener, The Human Use of Human Beings: Cybernetics and Society (New York: Avon Books, 1967 [paper]), pp. 207, 209-21. Wiener, a mathematical prodigy who received his Ph.D. in mathematics from Harvard at 18, wrote the original hardcover work in 1950. Hence, his remarks regarding the coming automation of the factory must be considered prescient indeed.
4. See Joseph Harrington, Jr., Computer Integrated Manufacturing (Huntington, NY: Robert E. Krieger, 1979 [original 1973]).
5. Daniel B. Dallas, "The Advent of the Automated Factory," Mfg. Eng., Nov. (1980), 66-76.
6. Harrington, op. cit., p. 8.
7. This terminology has been promoted largely by the U.S. Air Force's ICAM (Integrated Computer Aided Manufacturing) Program. See, for example, Integrated Computer Aided Manufacturing (ICAM): Task I--Final Report (Government Printing Office, Nov. 1978).

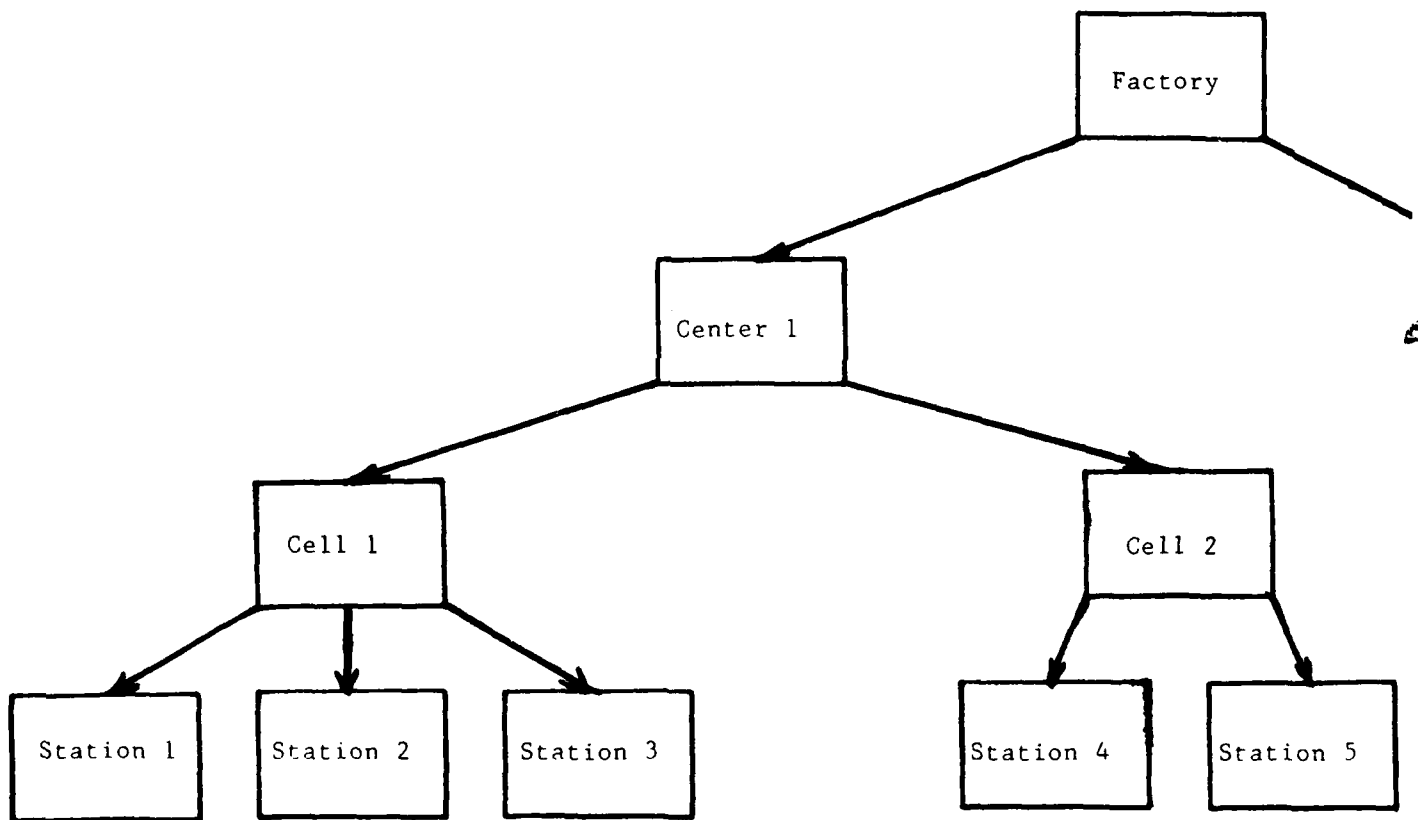


FIGURE 1. Hierarchical Arrangement of Manufacturing.

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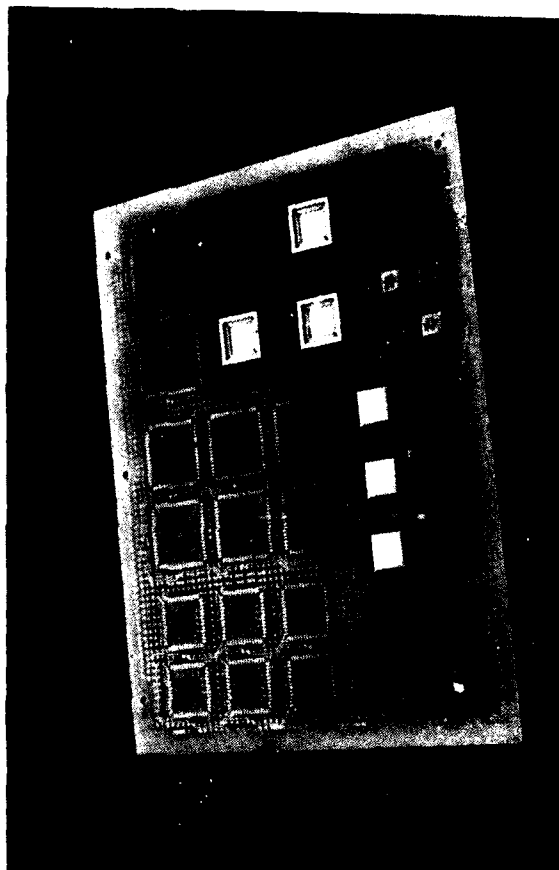


FIGURE 2. Partially Populated Test Board.

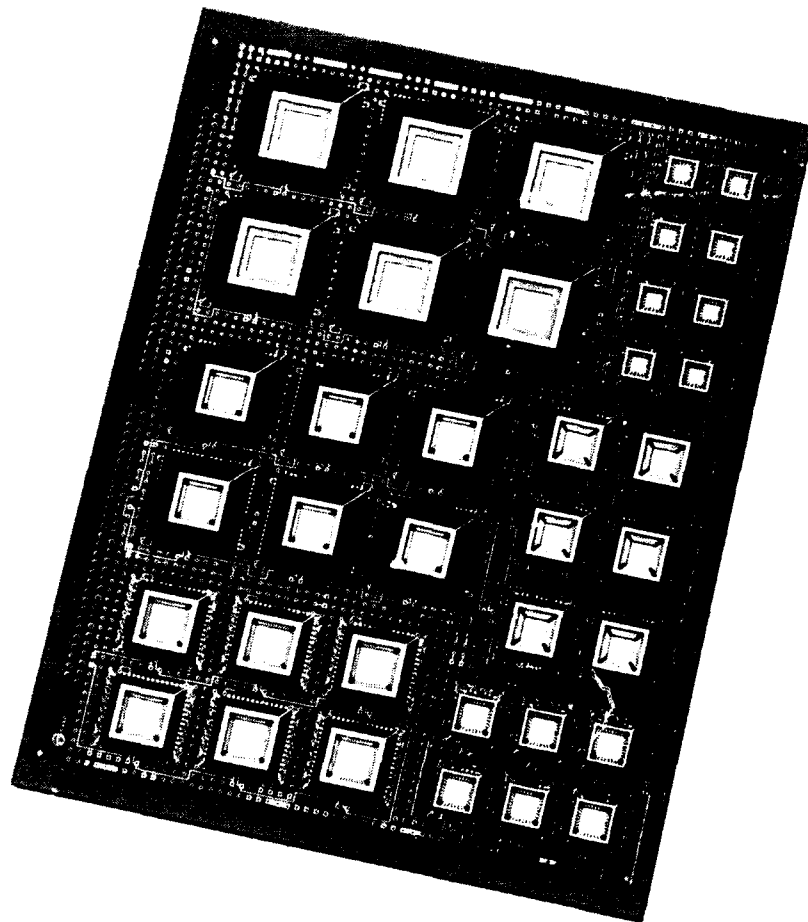


FIGURE 3. Populated SMA (LCCs).

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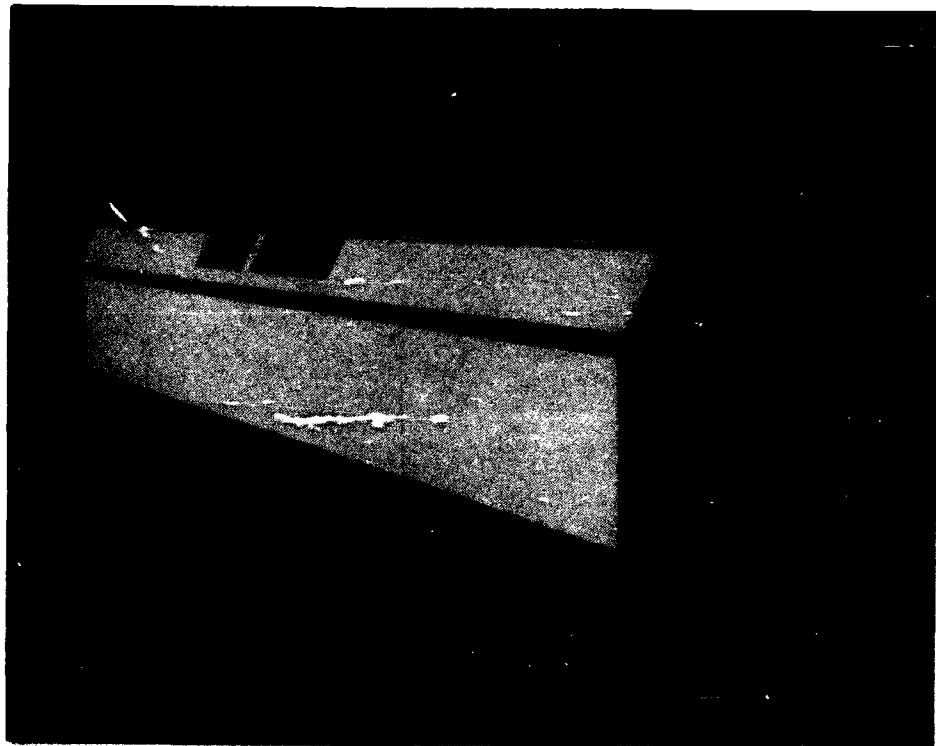


FIGURE 4. Automated In-Line Defluxer for FMC.

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